A 106-dB SNR Hybrid Oversampling Analog-to-Digital Converter for Digital Audio

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***Abstract*—An audio $\Sigma\Delta$ analog-to-digital converter (ADC) with the loop filter implemented by continuous-time (CT) and discrete-time (DT) circuits is presented. A tuning circuit is used to compensate for changes in the *RC* product due to process skew, power supply, temperature and sampling rate variation. To eliminate errors caused by inter-symbol interference (ISI) in the CT feedback DAC, a return-to-zero (RTZ) switching scheme is applied on the error current of the CT integrator. The converter is fabricated in a 0.35-μm CMOS process, and achieves 106-dB dynamic range, $-$99-dB THD + N.**

***Index Terms*—Continuous time $\Sigma\Delta$ modulator, oversampling ADC.**

I. Introduction

THE post-processing of multi-channel audio sources such as DVD audio requires high-performance low-cost codecs for the front-end and back-end signal conversions. The front-end $\Sigma\Delta$ ADCs in these codecs are commonly realized by switched-capacitor circuits. Switched-capacitor implementation offers many conveniences from the system point of view. The matching of on-chip capacitors yields good tracking of modulator coefficients while the discrete-time nature of the circuit allows the modulator transfer functions to scale proportionally with the modulator clock frequency. Another advantage of switched-capacitor circuits is the low sensitivity to modulator clock jitter. This tolerance to clock jitter greatly relaxes the jitter specification of the system clock. As more channels are integrated into the codec, power consumption and heat dissipation become an issue. In such case, techniques such as slew-rate boosting [1] can be used to enhance the operational amplifier (opamp) settling time while maintaining a low quiescent power consumption.

The integration of high-performance ADCs in a high-channel count audio codec has always been a challenge due to on-chip signal-dependent coupling that significantly increases the harmonic distortion in the ADC output. This problem occurs because short-duration on-chip signal-dependent glitches are sampled by the switched-capacitor circuits in the first stage via the reference voltage coupling, substrate coupling, or clock feedthrough mechanisms. The decimation filter engine of the ADC is a major source of such signal-dependent glitches. Techniques such as the use of a four-phase clocking scheme and dummy switches are commonly implemented to reduce the effect of this problem. These techniques yield good results when there are enough supply and ground pins to separate the clock driver circuitry from the signal processing blocks. Another possible means to reduce the effect of coupling is to time the critical moments of the switched-capacitor circuits so that they take place when there is no digital activity. However, in a highly integrated package such as multi-channel codec or DSP with integrated codec, these techniques do not work well. The digital filters or DSP engines, in such cases, operate at a higher rate to process data in a time-interleaved fashion. Phasing the critical moments of the switched-capacitor circuits to avoid sampling of signal-dependent glitches becomes very difficult or may not be feasible at all. Another drawback of the switched-capacitor implementation is the radiated EMI problem caused by the modulator clock feedthrough to the input pins of the ADCs. On-chip buffers can be used to isolate the sampling capacitors from the package pins at the expense of higher power consumption and a larger silicon area. Such buffers can also degrade linearity without very careful design.

A loop filter with combined CT and DT circuits [2] offers an alternative approach to realize a high-performance $\Sigma\Delta$ ADC. This combined loop filter structure offers several important advantages compared to the switched-capacitor-only structure. First, since there is no sampling of the input voltage, signal-dependent clock feedthrough and noise resampling in the first integrator do not exist. Second, any signal-dependent glitches coupled into the first integrator are averaged out over the clock period. This averaging characteristic of the CT integrator greatly reduces the harmonic distortion due to coupling. Third, the input impedance of the first integrator is purely resistive, hence, it does not emit EMI back to the input pins. Last, the intrinsic anti-alias filtering property of the CT first stage offers some high-frequency alias protection for the modulator.

This paper presents an audio $\Sigma\Delta$ ADC with the loop filter consisting of a continuous-time first stage, and a discrete-time second stage. Section II discusses the modulator topology, the problems associated with the front-end CT integrator, and solutions for these problems. Section III discusses the detailed implementation of the various blocks of the converter. Typical performance measurements from the silicon are presented in Section IV, followed by a conclusion.

II. Architecture

The presented ADC is a part of a multi-channel audio codec with the target performance of the ADC having 105-dB SNR and better than $-$95 dB of THD + N. Fig. 1 shows the block diagram of the second-order, 4-bit front-end modulator where

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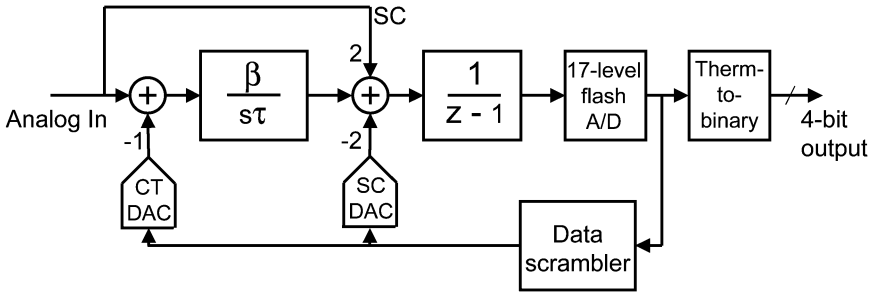

Fig. 1. Block diagram of the modulator.

β represents the normalized gain of the CT integrator. With an oversampling ratio (OSR) of 128 times and a digital output range of 0.75 $\times$ full scale, the theoretical SNR of this modulator is about 117 dB, well below the targeted circuit noise. A data-directed scrambler [3] is used to spectrally shape the error caused by the feedback DAC's unit element mismatch into the out-of-band frequency region. The feed forward SC path from the analog input to the second integrator forces the CT first stage to process only shaped noise. This technique allows a dynamic range scaling of the first stage that results in a significant reduction in the integrating capacitor size compared to the nonfeed forward topology. The trade off is a nonpure resistive input impedance that does not completely eliminate EMI emission. Traditional implementation of the ADC with a CT first stage suffers from several severe problems. Each of the problems will be studied and addressed in detail in Section II.

A. Inter-Symbol Interference

Inter-symbol interference (ISI) error is the result of mismatch in the rise and fall time in the CT feedback DAC output waveform which severely degrades the SNR and THD + N performance of the converter. To reduce this effect, a switch gate drive circuit such as [4] has been proposed. For further improvement in THD performance, the return-to-zero (RTZ) scheme is commonly used. RTZ completely eliminates ISI error at the cost of higher slew rate and wider bandwidth requirements for the amplifier. Moreover, since the first stage has no feedback during the off-period of the DAC, its output voltage exhibits large fluctuations that can cause headroom problems.

Our technique to completely eliminate ISI error applies a RTZ scheme on the difference between the input current and the feedback DAC current of the first stage.[1] Since the amplifier does not have to withstand the large current pulse as in the conventional RTZ case, it does not require a higher slew rate and wider bandwidth. Further, the first integrator does not exhibit large output fluctuations since it either integrates the closed loop error current or remains idle during the RTZ period.

The schematic of the CT first stage is shown in Fig. 2. A pair of RTZ switches S1 and S2 controlled by a timing control loop is added to the summing junctions of the integrator. The timing diagram of the switch control signal, DAC clock and the sampling clock of the second stage is shown in Fig. 3 where MCLK is the modulator clock, P1 is the sampling clock of the second stage and INT_CLK is the control signal for the summing junction

[1]Patent pending.

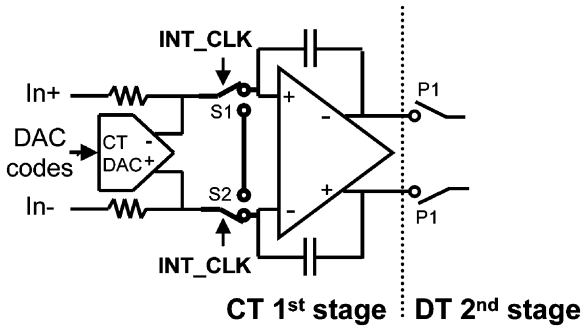

Fig. 2. Schematic of the CT first stage.

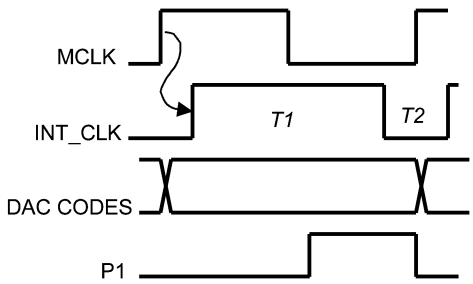

Fig. 3. Timing diagram of the CT first stage.

switches. When the rising edge of the modulator clock arrives, it turns on INT_CLK and starts the integration. After an interval T1, the timing control loop turns off INT_CLK and stops the integration. During the off period T2, the DAC codes are changed, the DAC outputs are short circuited and held at the CM voltage by a buffer amplifier. The DAC has no memory of its previous value and hence is free of ISI error. Since the transient behavior of the DAC output wave is immaterial to the converter performance, the switch gate driver circuit can be simple D-flip flops. The summing junction switches are relatively small since they conduct only the small error current. Further, any nonlinearities of the switches will be suppressed by the high loop gain.

Since the input of the CT integrator is now multiplied by a square wave at the modulator clock frequency, input signals at $f_{\mathbf{mclk}} \pm 20$ kHz are folded down to the audio band. However, in practical applications, the ADC input is band-limited by a preceding anti-alias filter, and hence should have no signal content near the modulator clock frequency range.

B. Input CM Voltage Stabilization

The first stage in Fig. 2 is directly connected to the external source via the input resistors, so that the summing junction

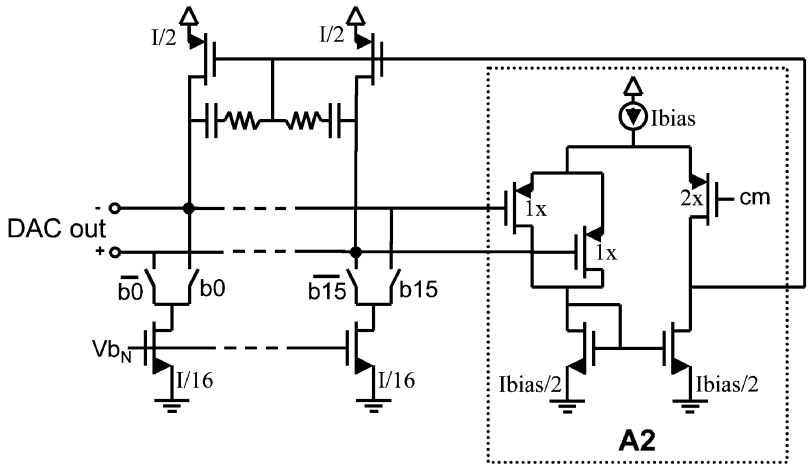

Fig. 4. Common-mode servo-amp and DAC circuit.

voltage of the integrator depends on the external CM voltage. With an AC coupled input signal source, the integrator summing junction voltage is undefined. Further, the DAC CM current is not zero due to the mismatch of the top pMOS devices and current steering nMOS devices. This CM current results in a shift in the operating point at the summing junctions of the integrator that may cause a headroom issue for the thermal noise optimized current sources. Another problem is the CM voltage variation at the summing junctions caused by the input resistor mismatch. Such signal-related CM voltage variation at the summing junctions introduces a second-order harmonic distortion. A pseudo-differential circuit consisting of two single ended amplifiers would avoid the resistor mismatch problem but it does not solve the DAC CM offset problem.

To alleviate all the CM voltage problems mentioned above, a servo amplifier A2 is added to the DAC to regulate the CM voltage at the integrator summing junctions.[2] The combined servo-amp and DAC schematic is shown in Fig. 4. The servo amplifier consists of a simple differential pair with one device split as shown. A2 regulates the CM voltage at the integrator summing junctions by adjusting the bias voltage of the pMOS devices in the DAC. During the RTZ period of the DAC output, A2 and the DAC form a CM buffer amplifier to force the DAC outputs to the CM level. This technique avoids a separate CM buffer for the DAC while providing a continuous CM voltage regulation at the integrator summing junctions. Since the CM regulation loop uses the feedback DAC as the output stage, it does not introduce any additional noise source into the differential signal path. Noise of the servo amp A2 is common-mode and does not degrade the system performance. The CM regulation loop in Fig. 4 forms a two-stage amplifier and thus requires a compensation network for stability. The CT first stage with the input CM voltage regulation circuit is shown in Fig. 5.

C. RC Product and Sampling Rate Variation

A shift in the *RC* product value due to process and temperature variation can significantly affect the modulator noise transfer function (NTF) and lead to degradation in performance of the converter as shown in Fig. 6. When both *R* and *C* are 25% larger than the nominal values, the theoretical SNR degrades to 109 dB. When both *R* and *C* are 25% smaller than the nominal values, the NTF exhibits some peaking and high out-of-band noise gain.

[2]Patent pending.

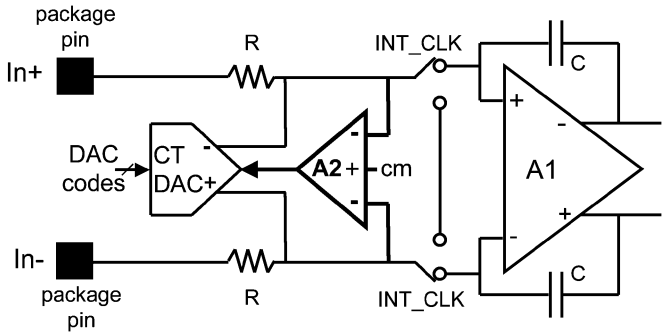

Fig. 5. CT first stage with input CM regulation.

The required output sample rate of the ADC ranges from 8 to 48 kHz, implying a modulator clock frequency range of 1.024 to 6.144 MHz. A modulator designed with one set of *RC* cannot operate with such wide range of clock frequency. On-chip *RC* tuning is therefore necessary to ensure stability and to maintain the modulator performance under all conditions.

A master–slave tuning scheme such as [5] is commonly used in CT circuits that require on-chip *RC* tuning. The drawback of such discrete capacitor tuning strategy is the additional on-chip capacitor required to compensate for low modulator clock frequencies and smaller than nominal *RC* values. For multi-channel ADCs, these additional capacitors can take up a significantly large area. Tuning of *R* is not suitable for high precision converters since the series switches introduce a source of distortion into the modulator. Another drawback of discrete tuning is that it requires a known modulator clock frequency to calibrate the master tuning circuit. This requirement makes it not suitable for audio applications since the master clock frequency can vary widely.

The proposed tuning strategy adjusts both the integrating capacitors and the integration period.[2] It uses the on-chip reference voltage to calibrate the master tuning circuit. To compensate for larger *RC* value due to process skew, or higher modulator clock frequency, the integrating capacitors of the CT first

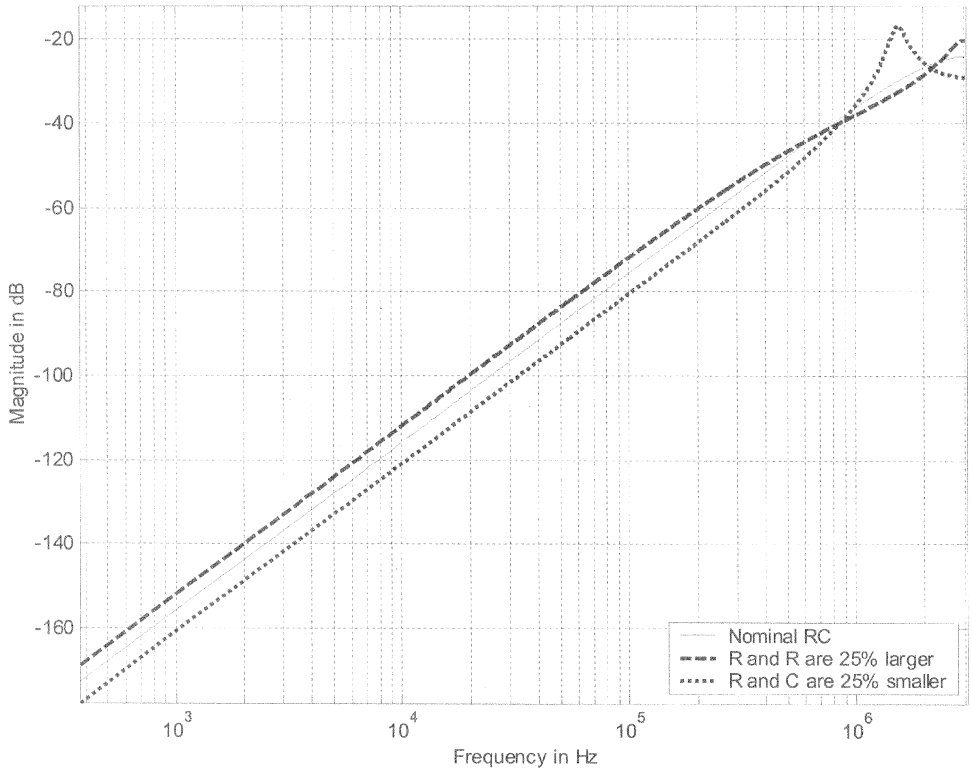

Fig. 6. Effect of *RC* variation on the NTF.

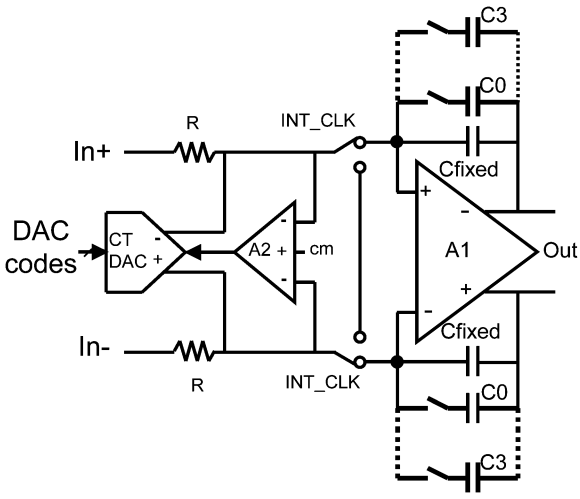

Fig. 7. CT first stage with tunable integrating capacitors.

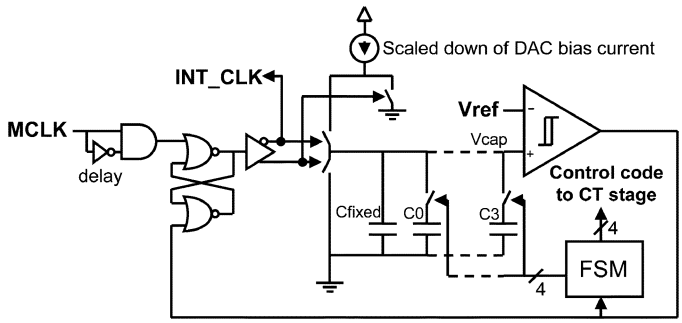

Fig. 8. Schematic of the timing control circuit.

stage are discretely sized down by a finite-state machine. For smaller *RC* value, or lower modulator clock frequency, the integration interval is kept constant. The schematic of the CT first stage with tunable integrating capacitors is shown in Fig. 7 [8]. Each of the integrating capacitors now consists of a fixed capacitor and a 4-bit binary weighted programmable capacitor array.

The timing control loop shown in Fig. 8 produces the control signals for the summing junction switches and the tunable integrating capacitors. It consists of a reset-set (RS) flip-flop, a fixed capacitor, a 4-bit binary weighted programmable capacitor array, a hysteresis comparator, and a finite state machine (FSM). The ratio of the fixed capacitor and the programmable capacitor array in this timing loop is the same as in the CT first stage. The operation of the timing control is as follows. Consider the case of nominal *RC* value shown in Fig. 9(a). When the rising edge of the modulator clock arrives, it starts the integrating clock INT_CLK, and begins to charge up the capacitors in the timing control loop. When this voltage, Vcap, reaches the comparator trip point, the comparator will reset Vcap to zero and turn off the integrating clock. The current source is connected to ground during the nonuse phase to completely discharge the parasitic capacitor and eliminate any glitching at the beginning of the charging phase. The operation then repeats with the next rising edge of the modulator clock. For the case of smaller *RC* product shown in Fig. 9(b), Vcap reaches the comparator trip point earlier, the integration period is then shortened to compensate for larger integrator gain. For the case where the *RC* product is larger, the integrating interval becomes longer as shown in Fig. 9(c). When this interval becomes longer than the clock period as in Fig. 9(d), the FSM will begin cutting down the capacitor size in the tuning circuit. This process continues until the

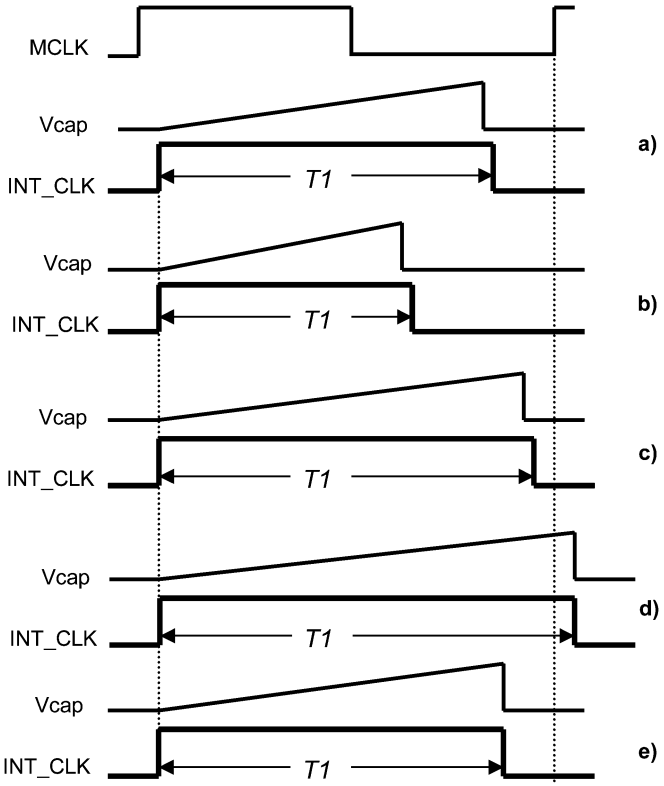

Fig. 9. Tuning for *RC* variation.

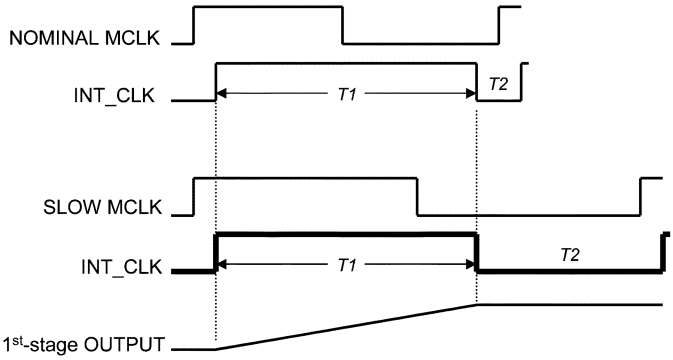

Fig. 10. Tuning for slow modulator clock.

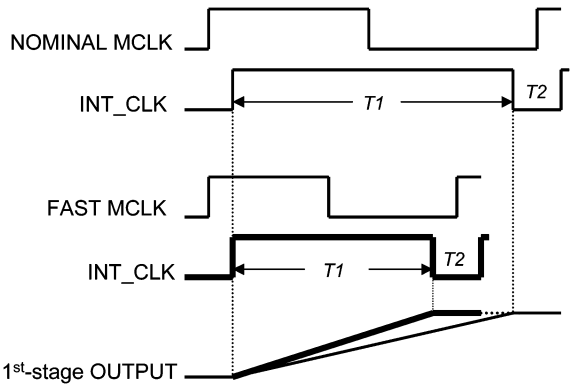

Fig. 11. Tuning for fast modulator clock.

integration interval is shorter than the clock period. When this condition is met as in Fig. 9(e), the tuning is completed and the control code is copied to the CT integrator.

Fig. 10 shows the tuning for slow modulator clock frequency. Since the integration interval T1 is determined only by the timing circuit, longer modulator clock period has no effect on the integration time. The CT integrator stays idles during T2, and hence its effective gain does not change. Fig. 11 shows the tuning for fast modulator clock frequency. Under this condition, the FSM will start cutting down the programmable capacitor in the tuning loop until T1 is shorter than the clock period so that a minimum idle period T2 is maintained. This is necessary so that the DAC codes can be changed without causing ISI error. The corrected control code is then copied to the CT first stage. This tuning technique allows a continuously adjustable output sample rate up to 65 ksample/s.

D. Jitter Sensitivity

The feedback DAC in the first stage is a current-steering type, which is very sensitive to clock jitter. The theoretical SNR limit of the converter due to only the jitter-induced noise of the feedback DAC is expressed in the charge domain as

$$\mathrm{SNR} = 10\log\left(\frac{P_S}{P_N}\right) = 10\log\left(\frac{Q_S^2}{Q_N^2/\mathrm{OSR}}\right)$$

where Q_S is the signal charge and Q_N is the noise charge. In one clock cycle, this expression can be rewritten as

$$\mathrm{SNR} = 10\log\left(\frac{\left(0.75\left(I_{\mathrm{DAC}}/\sqrt{2}\right)T\right)^2}{\sigma_j^2\left(\frac{I_{\mathrm{DAC}}}{16}\right)^2/\mathrm{OSR}}\right)$$

where T is the modulator clock period which equals 162.8 ns, and σ_j is the rms jitter amplitude, assuming a 0.75 output range usage and 4-bit quantizer. For a 110-dB SNR target, the rms jitter requirement of the modulator is about 49 ps. This is a stringent requirement on the system clock compared to a switched-capacitor-only implementation. One approach is to increase the feedback DAC resolution to 6-bit in order to reduce jitter sensitivity in the feedback DAC [6]. However, the area occupied by a 6-bit data scrambler becomes unacceptable. Further, the unit current cell becomes much smaller which increases the mismatch error. Another technique such as the use of pulse-shaped feedback DAC [7] is not suitable for this design since it requires the generation of a highly accurate cosine waveform, which itself is a very challenging task.

It can be seen that the timing control loop basically converts the modulator clock edge jitter into the positional jitter of the integration interval, hence the modulator clock jitter is immaterial to the CT first stage performance. In fact, the jitter problem is shifted to the timing control loop as jitter from this loop will alter the integration interval T1 and degrade the SNR. The design of a low-jitter timing control loop will be presented in Section III.

III. Circuit Design

A. CT First Stage Amplifier

In CT circuits, the value of the waveform at all times is important, as opposed to just the end value in DT circuits. Any slewing in the first stage will severely degrade the THD + N performance of the converter. The amplifier shown in Fig. 12 is chosen for its high output drive capability and low quiescent

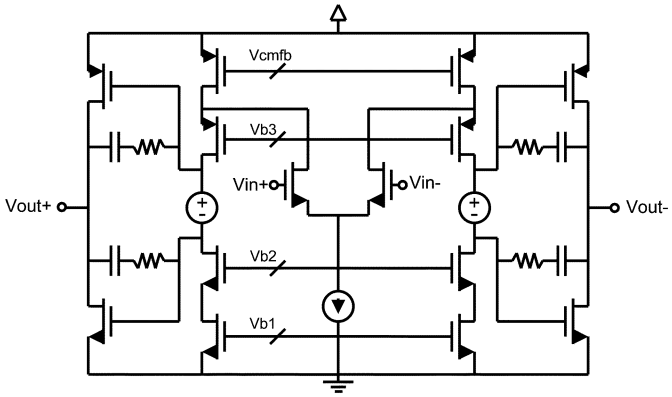

Fig. 12. Schematic of the first-stage amplifier.

power consumption. For simplicity, the CT CMFB circuit is not shown. The internal slew is designed to ensure that the integrator never slews even with the largest sample-to-sample code jump. The high DC gain of the amplifier ensures the quality of the corresponding NTF zero at DC. Any cross-over distortion of the output stage is heavily suppressed by the high gain first stage when referred back to the input.

B. Timing Control Loop

The main challenge in designing the timing control loop is the low-jitter requirement. The design criteria for this circuit are similar to those found in the design of a low-jitter relaxation oscillator. The two main sources of jitter are the current source noise and the comparator noise. Fortunately, the current source uses the same bias circuit as the current steering DAC, and hence, is already optimized for low noise performance. The comparator noise, on the other hand, is the rms noise measured at the trip point and can be optimized by using sufficiently large bias current and input devices. The cycle-to-cycle rms jitter of the loop can then be approximated as

$$\text{jitter}_{\text{rms}} \approx \frac{V_{\text{noise}}}{I/C}$$

where V_{noise} is the root-sum-squared of the current source noise and the comparator noise. I is the magnitude of the current source, and C is the sum of the capacitors in the tuning circuit. The timing control circuit was designed to have 32 ps rms jitter and it is not the limiting factor for the SNR of the converter.

C. The Flash A/D

To reduce the power consumption and silicon area, the flash ADC consists of only nine comparators. One comparator is used to determine the polarity of the input signal to either pass the input through or its inverted waveform to the eight-level flash ADC. Extra logic circuits then combine the sign and magnitude information to form the correct digital output. This technique results in a saving of approximately 40% in area and power consumption of the flash A/D compared to a traditional implementation of 16 comparators.

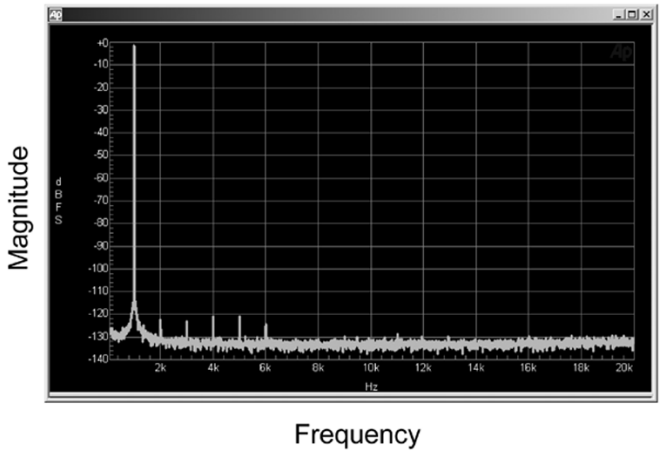

Fig. 13. 8k-FFT plot of a −1-dBFS output tone at 1 kHz.

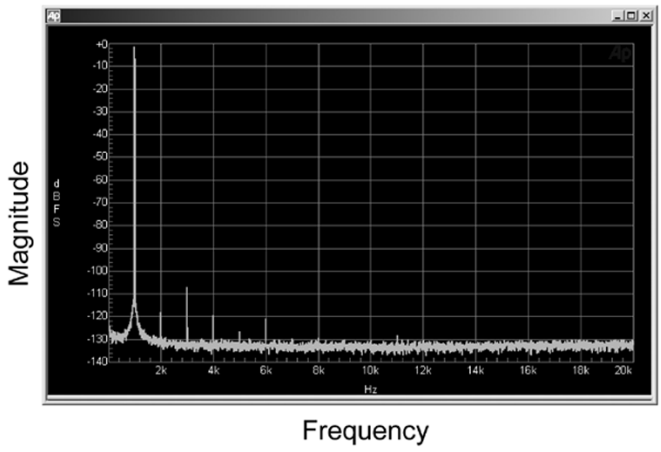

Fig. 14. 8k-FFT plot of a −1-dBFS tone with all converters running.

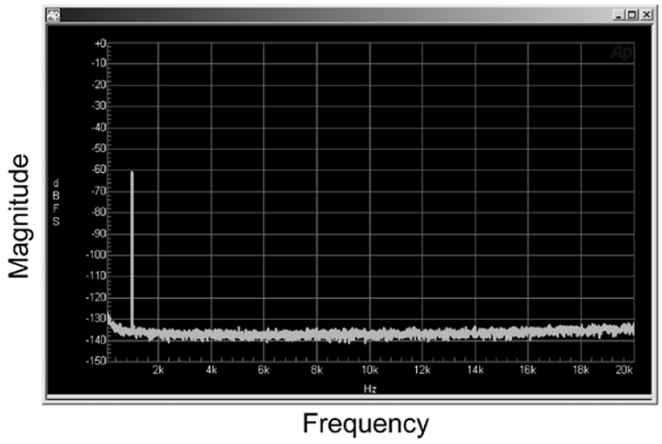

Fig. 15. 8k-FFT plot of a −60-dBFS output tone at 1 kHz.

D. The Decimation Filter

The decimation filter consists of a sinc4 filter followed by two half-band filters and a compensation filter. For the 96-kHz and 192-kHz output sample rate, the data from the modulator is first sampled and held by 2 × and 4 ×, respectively. The entire digital filter engines then runs 2 × and 4 × faster to produce higher output sample rates. This approach maintains the same passband ripple and stopband attenuation specifications at all

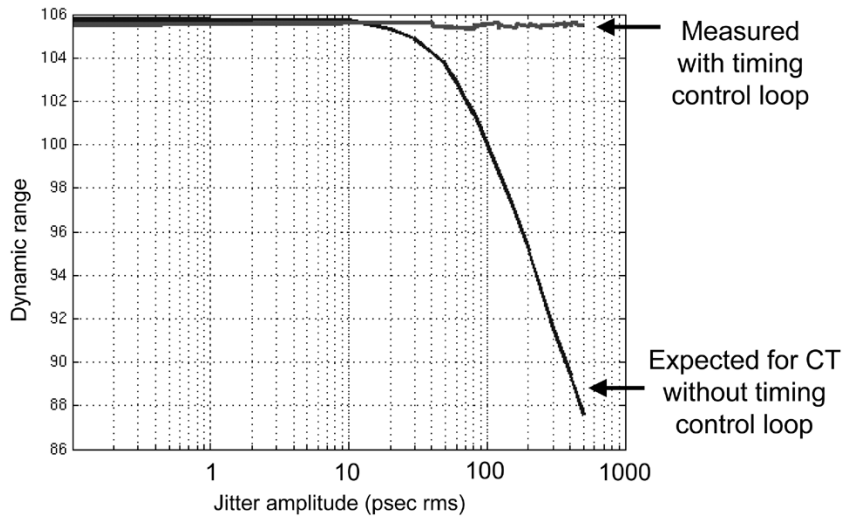

Fig. 16. Dynamic range versus mclk jitter amplitude.

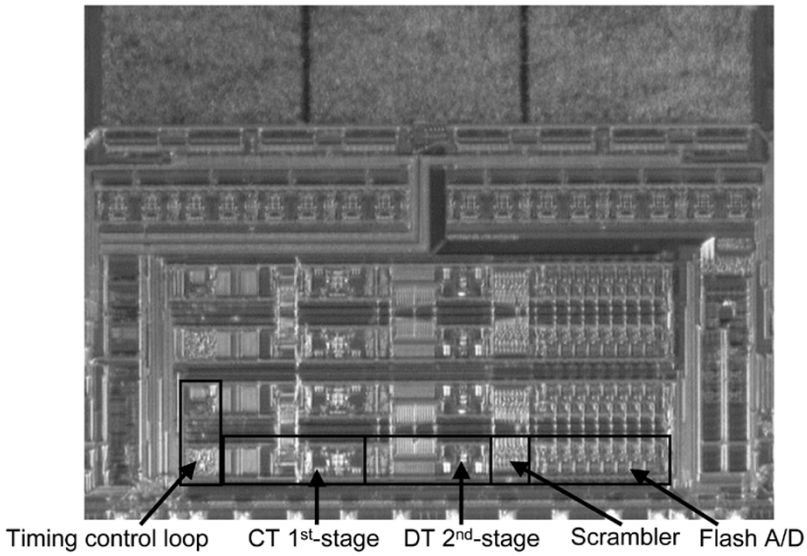

Fig. 17. Die photo.

output sample rates without changing the sequencer and coefficient ROMs. The tradeoff is the higher power consumption at higher output sample rates.

IV. Measurement Results

Fig. 13 shows the 8k-FFT plot of a -1-dB full-scale output tone at 1 kHz captured by Audio Precision. The very low harmonic distortion content indicates the excellent full-scale linearity of the converter. Fig. 14 shows the THD$+N$ measurement when all the converters (ADCs and DACs) on chip are running at full-scale level with the same input tone. This condition represents the worst case THD $+ N$ since all the harmonics from different channels are in phase. The third harmonic component in this case rises to -107 dB, but the overall THD $+ N$ measurement is still very good. Fig. 15 shows the spectral plot of a 1 kHz tone at -60 dBFS, corresponding to the dynamic-range measurement. No dither was used at the input of the quantizer since the modulator has good tonal performance. To see how the ADC performs in the presence of clock jitter, the modulator clock is injected with wide-band jitter up to 500 ps rms.

TABLE I
Performance Summary

SNR, 20Hz – 20kHz	106dB A-weighted
Dynamic range, -60dBFS	106dB A-weighted
THD+N, -1dBFS	-99dB
Full scale input	2Vrms differential
Analog power consumption	~18mW per channel
Analog area	~0.82mm^2 per channel
Input CMRR	-65dB
Digital filter stopband attenuation	-80dB

As shown in Fig. 16, without the timing control loop, the dynamic range would have been degraded to 104 dB with a jitter of 50 ps. With the timing control loop, the dynamic range is virtually unchanged in the presence of clock jitter up to 500 ps rms. Fig. 17 shows the die photograph. Table I summarizes the chip performance.

V. Conclusion

All the limitations of the CT first stage such as ISI error, high sensitivity to clock jitter, variation in the *RC* product, and the modulator clock dependency have been studied and eliminated by the proposed techniques. The ISI error was eliminated by the use of RTZ scheme applied on the error signal of the first stage. The sensitivity to clock jitter was solved by using an on-chip low-jitter timing loop. The same timing control loop also tunes the *RC* product for process skew and change in modulator clock frequency. Input CM dependency is eliminated by the use of a CM regulation circuit. The IC is fabricated in a 0.35-μm CMOS double-poly triple-metal process. The total area per channel including the decimation filter is 1.82 mm^2. Both analog and digital supplies are 3.3 V. The total power consumption per channel including the decimation filter is approximately 32 mW measured at 48-kHz output data rate.

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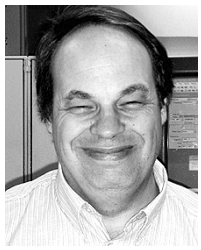

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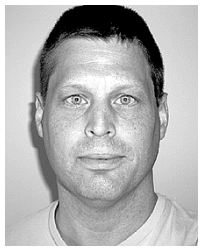

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