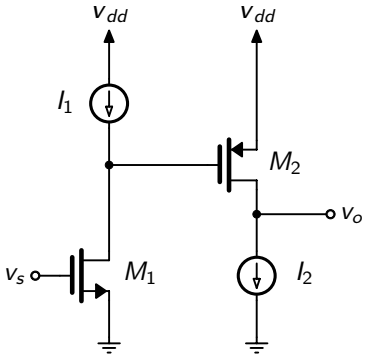
Problem Set 3b - Cascode

Question 1

Given a two-stage common-source amplifier where the biasing current sources I_1 and I_2 have output resistances equal to those of M_1 and M_2 respectively, determine an expression for the voltage gain, v_o/v_s, in terms of g_{m1}, g_{m2}, r_{o1} and r_{o2}.



Answer

$v_o/v_s = (g_{m1}g_{m2}r_{o1}r_{o2})/4$

Question 2

Given transistor M_1 which has $\mu_n C_{ox} = 240\mu\text{A/V}^2$, $\lambda_n' = 50\text{nm/V}$, $V_t = 0.5\text{V}$, $W = 1\mu\text{m}$, and $L = 200\text{nm}$:

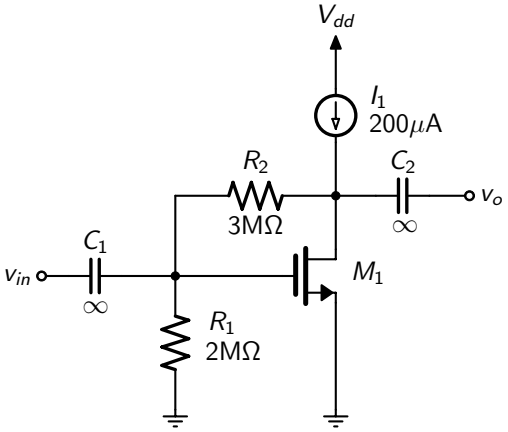
a) Ignoring any DC current in R_2 and assuming $r_o \to \infty$, determine V_{GS}.

b) Determine the DC current in R_2, determine V_{DS}, and justify your neglection of the DC current when calculating V_{GS} in part a).

c) Determine the small-signal voltage gain v_o/v_{in}. (Assume an ideal current source)

d) Assuming the negative swing of the output limits the overall output swing, what is the min output voltage, max output voltage and output peak-to-peak swing?

e) What is the corresponding input amplitude, max and min voltages at the gate?



Answer

a) $V_{GS} = 1.077\text{V}$

b) $V_{DS} = 2.693\text{V}$

c) $v_o/v_{in} = -13.76\text{V/V}$

d) $V_{o,pp} = 3.945\text{V}$; $V_{o,min} = 0.7207\text{V}$; $V_{o,max} = 4.666\text{V}$

e) $V_{G,pp} = 0.2868\text{V}$; $V_{G,min} = 0.934\text{V}$; $V_{G,max} = 1.221\text{V}$

Question 3

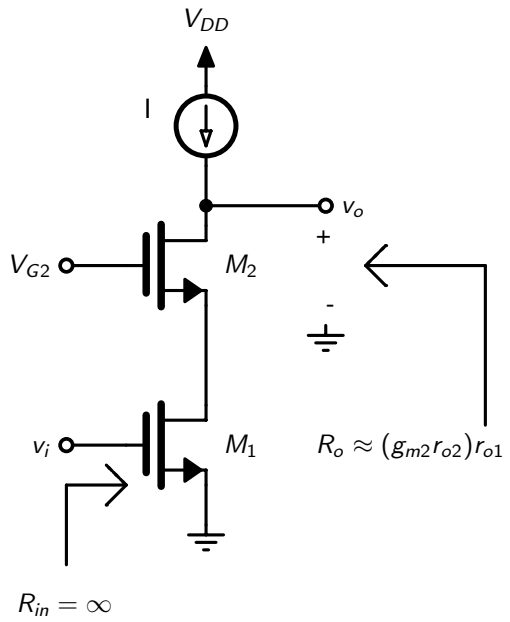
In a MOS cascode amplifier, the cascode transistor is required to raise the output resistance by a factor of 40 over that of a non-cascode amplifier. If the transistor is operated at $V_{ov} = 0.2\text{V}$, what must its λ_n be? If the process technology specifies λ'_n as 50nm/V, what channel length must the transistor have?

Answer

$\lambda_n = 0.25\text{V}^{-1}$; $L = 200\text{nm}$

Question 4

Design the cascode amplifier shown below to obtain $g_{m1} = 1\text{mA/V}$ and $R_o = 400\text{k}\Omega$. Use a $0.18 - \mu m$ technology for which $V_{tn} = 0.5\text{V}$, $\lambda'_n = 200\text{nm/V}$ and $\mu_n C_{ox} = 400\mu\text{A/V}^2$. Determine L, W/L, V_{G1}, V_{G2}, and I. Use identical transistors operated at $V_{ov} = 0.2\text{V}$, and design for the maximum possible negative signal swing at the output. What is the value of the minimum permitted output voltage?



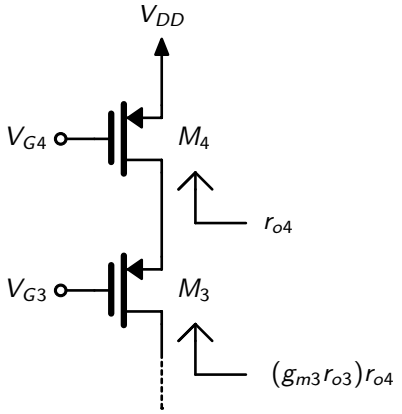
Answer

$L = 400\text{nm}$; $W/L = 12.5$; $V_{G1} = 0.7\text{V}$; $V_{G2} = 0.9\text{V}$; $I = 100\mu\text{A}$; $V_{o,min} = 0.4\text{V}$

Question 5

Design the circuit shown below to provide an output of $I_D = 100\mu\text{A}$. Use $V_{DD} = 3.3\text{V}$, and assume the PMOS transistors to have $\mu_p C_{ox} = 60\mu\text{A/V}^2$, $V_{tp} = -0.8\text{V}$, $L = 250\text{nm}$, and $\lambda'_p = -50\text{nm/V}$. The current source is to have the widest possible signal swing at its output. Design for $V_{ov} = 0.2\text{V}$, and specify the width, W, of

the transistors and of V_{G3} and V_{G4}. What is the highest allowable voltage at the output? What is the value of output impedance, R_o?



Answer

$W = 20.83\mu$m; $V_{G4} = 2.3$V; $V_{G3} = 2.1$V; $V_{o,max} = 2.9$V; $R_o = 2.5$MΩ

Question 6

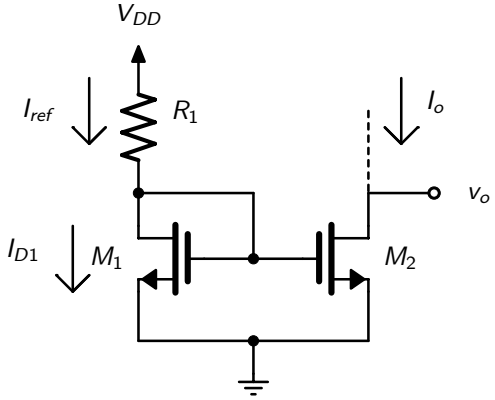
For $V_{DD} = 1.8$V and using $I_{ref} = 100\mu$A, it is required to design the circuit below to obtain an output current whose nominal value is $I_{ref} = 100\mu$A.

a) Find R if M_1 and M_2 are matched with channel lengths of $L = 500$nm, channel widths of $W = 4\mu$m, $V_{tn} = 0.5$V, and $\mu_n C_{ox} = 400\mu\text{A/V}^2$.

b) What is the lowest possible value for V_o?

c) Assuming that for this process technology $\lambda'_n = 50\text{nm/V}$, find the output resistance of the current source.

d) Find the current change in output current resulting from a +0.5V change in V_o



Answer

a) $R = 10.5$kΩ
b) $V_{o,min} = 0.25$V
c) $r_{o3} = 100$kΩ
d) $\Delta I_D = 5\mu$A