A 50-MS/s (35 mW) to 1-kS/s (15 μW) Power Scaleable 10-bit Pipelined ADC Using Rapid Power-On Opamps and Minimal Bias Current Variation

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***Abstract*—A novel rapid power-on operational amplifier and a current modulation technique are used in a 10-bit 1.5-bit/stage pipelined ADC in 0.18-μm CMOS to realize power scalability between 1 kS/s (15 μW) and 50 MS/s (35 mW), while maintaining an SNDR of 54–56 dB for all sampling rates. The current modulated power scaling (CMPS) technique is shown to enhance the power scaleable range of current scaling by 50 times, allowing ADC power to be varied by a factor of 2500 while only varying bias currents by a factor of 50. Furthermore, the nominal power is reduced by 20%–30% by completely powering off the rapid power-on opamps during the sampling phase in the pipeline's sample-and-holds.**

***Index Terms*—ADC, analog-to-digital conversion, CMOS, low power, pipeline, power reduction, power scaleable, reconfigurable, scaleable.**

I. Introduction

A POWER-SCALEABLE ADC is motivated by flexible applications where a single ADC is required to operate at different operating speeds. As ADCs are typically power optimized for only a single operating speed, a power scaleable ADC affords minimal power consumption over a broad range of operating speeds in a single circuit. In addition, a power-scaleable ADC is of great utility in reducing design efforts as a single ADC can be targeted for a variety of applications each with vastly different performance requirements with respect to power and speed. Thus, a power-scaleable ADC can reduce time to market and save costs associated in producing several individually power-optimized ADCs.

The power consumed by CMOS digital circuits explicitly scales with operating speed, f_s, capacitive load, C_L, and power supply $V_{\rm DD}$, according to $f_s C_L V_{\rm DD}^2$ (ignoring leakage currents). However, analog power (the dominant power consumer in ADCs) does not explicitly scale with sampling rate as it is mostly static in nature. Static analog power is a consequence of static bias currents used to bias transistors in the saturation region. Previous publications of high-speed power-scaleable ADCs achieve power scalability by making operational amplifier (opamp) bias currents a function of sampling rate. In [1], opamp bias currents were varied by three orders of magnitude to achieve scaleable power between operating speeds of 20 kHz and 20 MHz in a pipeline/delta-sigma ADC. In [2], opamp bias currents were varied to reduce ADC power between sampling rates of $\sim$3 and 220 MS/s. Although effective for small variations in sampling rate, for large bias current variations (to maximize the power-scaleable range), current mirrors shift from strong to weak inversion resulting in reduced yield, increased sensitivity to noise, and multiple design corners; increasing design and verification time. The architecture of this work [3] was thus motivated by a desire to minimize the amount of bias current scaling required for large variations in power with sampling rate.

The organization of discussion in this paper is as follows. Section II compares the tradeoffs in ADC performance when transistors operate in strong and weak inversion. Section III describes the architecture of this work to realize power scalability. Section IV details the circuit implementation of key circuit blocks in the ADC, where the functionality of a rapid power-on opamp required to attain power scalability at high sampling rates is detailed. Section V presents measurement results of a prototype fabricated in 0.18-μm CMOS, where while maintaining an signal-to-noise-plus-distortion ratio (SNDR) between 54 and 56 dB, the ADC was measured to have a power-scaleable range of 1:2500, while the bias currents were only varied by a factor of 50. Section VI concludes the paper.

II. Strong Versus Weak Inversion

MOS transistors typically operate in strong inversion when $V_{\rm eff} \equiv V_{\rm GS} - V_t$ is greater than 100 to 200 mV, and in weak inversion (subthreshold) when $V_{\rm eff}$ is negative [4]. In ADCs which rely on frequency-dependent biasing, large sampling rate variations shift transistors biased in strong inversion to weak inversion for low sampling rates (thus, low bias currents). For a transistor operating in strong inversion, the rate of change of drain-source current with gate-source voltage is given approximately as

$$\frac{dI_{\rm DS}}{dV_{\rm GS}} \propto V_{\rm eff}$$

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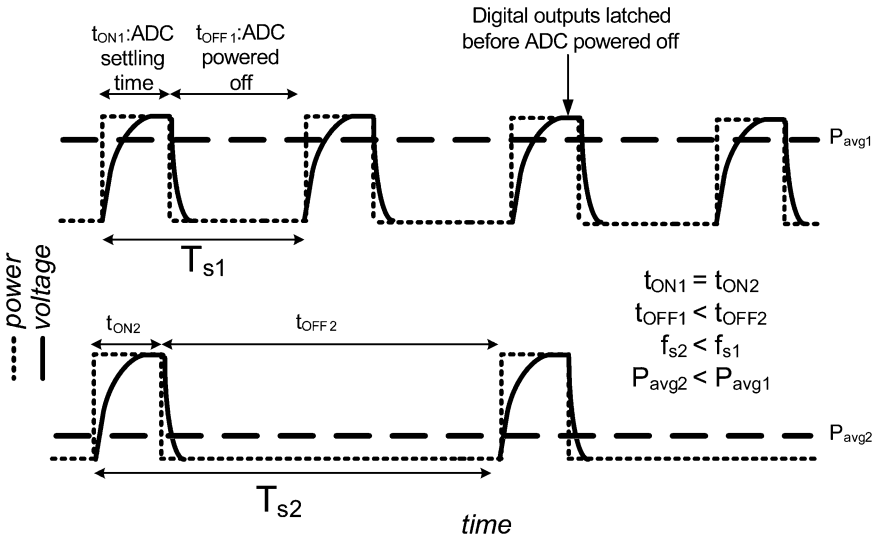

Fig. 1. CMPS with constant bias currents. Dashed power line indicates instantaneous power of analog portion of ADC, and solid voltage line represents effective settling accuracy of the ADC.

and

$$\frac{dI_{\rm DS}}{dV_{\rm GS}} \propto e^{(V_{\rm eff}/nU_T)}$$

in weak inversion (where U_T is the thermal voltage kT/q, and n is a scaling parameter). Due to the exponential dependence of drain-source current with gate-source voltage in weak inversion, small variations of an opamp's current source's gate-source voltage from the nominal bias point due to (e.g.) noise coupling from a nearby digital circuit, or processing-induced threshold mismatch, can cause opamp bias currents to fluctuate significantly (e.g. $>$30% for 3 sigma of total yield [5]). Since opamp bandwidth is a function of bias currents and the settling accuracy of a sample-and-hold is a strong function of opamp bandwidth, weak inversion results in the accuracy of an ADC being highly sensitive to noise and process mismatch. Thus, designs which rely on current mirrors in weak inversion tend to suffer from poor yield [5], and therefore are more costly to design, verify, and test.

III. Power-Scaleable Architecture

A. Current Modulated Power Scaling (CMPS)

In a power-optimized ADC, just enough analog power (set by bias currents) is consumed by the ADC to allow the analog circuits to settle to the desired accuracy. If, as the ADC sampling rate is decreased, the bias currents are kept constant, the time required by analog circuits to settle to the desired accuracy becomes a smaller percentage of the sampling period. Although ADCs are predominantly analog, ADC outputs are digital. Hence, per ADC output only enough power to set the digital outputs to the correct logic levels representing the sampled analog input is required. Thus, if bias currents are fixed as the sampling rate is reduced, the ADC's digital outputs can be latched after the desired settling accuracy is attained, and the analog portion of the ADC powered down shortly thereafter, as shown in Fig. 1, and powered back on when the next input is to be digitized. By powering off the analog portion of the ADC between conversions, the average power of the ADC is given by

$$P_{\rm avg} = P_{\rm ON} t_{\rm ON} f_s + P_{\rm fixed}$$

where $t_{\rm ON}$ is the time the ADC is powered on, $P_{\rm ON}$ is the power consumed by the ADC during $t_{\rm ON}$, $f_s = 1/T_s$, and $P_{\rm fixed}$ is the power consumed by circuits which are not powered off during $t_{\rm OFF}$ ($t_{\rm OFF} = T_s - t_{\rm ON}$). Thus, lower power for lower sampling rates is attained only by changing the time the ADC is powered off, which can be digitally controlled. As $t_{\rm ON}$ (and thus, bias currents) remain fixed for different sampling rates with this current modulated power scaling (CMPS) approach, strong inversion performance can be retained for lower sampling rates. With CMPS, the lowest power consumed by the ADC (thus, power-scaleable range) is limited only by $P_{\rm fixed}$, which is shown in Section IV-H to be relatively small. The highest sampling rate attainable with CMPS is limited by how quickly the ADC can power-on after being in a state of minimal power consumption during $t_{\rm OFF}$—which is the key design challenge of this work. A rapid power-on also minimizes $t_{\rm ON}$.

If, in addition to using CMPS, the bias currents are also scaled, as shown in Fig. 2, CMPS enhances the power-scaleable range of bias current scaling. This is due to the fact that for any current-scaled sampling rate, the ADC can always be powered off between conversions to yield a further reduction in ADC power without further reductions in bias currents. For example, if current scaling is used to vary ADC power by a factor of one to ten, and CMPS allows ADC power to be reduced by a factor of one to 50, application of CMPS to the lowest power attainable with current scaling results in a minimum power of $1/(10 \times 50) = 1/500$th the maximum power. Thus, the CMPS approach necessarily improves on any previous architecture which relies solely on current scaling to achieve power scalability. The lowest power attainable when CMPS is used in conjunction with current scaling is limited practically by how much current scaling can be tolerated by the application in question.

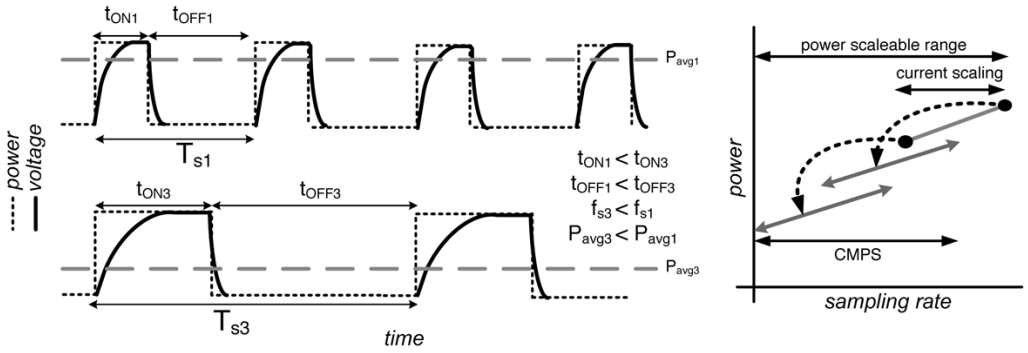

Fig. 2. CMPS used in conjunction with bias current scaling to enhance power-scaleable range.

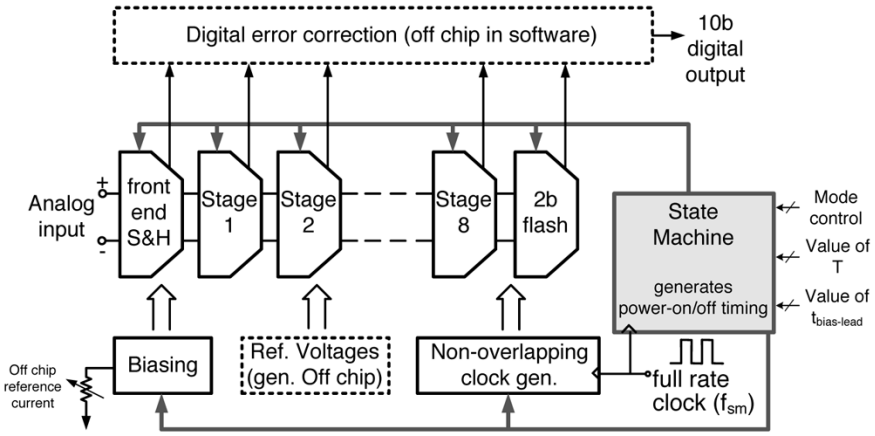

Fig. 3. System level diagram of power-scaleable ADC.

B. Application of CMPS to a 10-bit 1.5-bit/Stage Pipelined Architecture

CMPS can be applied to any Nyquist-rate ADC architecture to realize a scaleable power with sampling rate. In this work, CMPS was applied to a 10-bit 1.5-bit/stage pipelined architecture [6]. A block diagram of the overall power-scaleable pipelined ADC is shown in Fig. 3.

In the CMPS pipeline ADC of this work, after a sampled analog input is digitized, all pipeline stages are powered down. To simplify the clocking of the pipeline stages, only one pipeline stage powers on at a given time when CMPS is applied to the pipeline. As such, the next digital output is available only after the input traverses the entire pipeline, as shown in Fig. 4 (i.e., the ADC operates similar to an algorithmic ADC when CMPS is enabled). Shortly before a given pipeline stage powers off, the subsequent pipeline stage powers on and enters the hold mode. The digital outputs from each pipeline stage are also digitally latched before each pipeline stage powers off. As $t_{\rm ON}$ is given by the conversion latency of the ADC $(t_{\rm lat})$, the maximum sampling rate when CMPS is applied to the pipeline architecture is $1/t_{\rm lat}$. The maximum sampling rate attainable with a pipeline architecture, however, is given by the inverse of the maximum latency through a single pipeline stage $(1/t_{\rm stage\text{-}lat})$, which is larger than $1/t_{\rm lat}$. To achieve scaleable power for sampling rates not allowable with CMPS enabled (i.e., between $1/t_{\rm lat}$ and $1/t_{\rm stage\text{-}lat}$), the ADC of this work was given two modes of power scaling operation, as shown in Fig. 5. In the first mode of operation, CMPS was used to attain power scalability for sampling rates up to $1/t_{\rm lat}$ (corresponding to 5.55 MS/s in this work). In the second mode of operation, CMPS was disabled, and the ADC operated as a conventional pipeline ADC (i.e., *without* powering off the analog portion of the ADC between conversions) so as to attain the maximum sampling rate of $1/t_{\rm stage\text{-}lat}$ (corresponding to 50 MS/s in this work). Power scalability is realized in the second mode of operation by using bias current scaling. Since bias current scaling is required only over a relatively narrow range of sampling rates (between 5.55 and 50 MS/s), operation of transistors in weak inversion can be minimized or avoided through judicious design. External control bits were used to set the mode of operation (i.e., enable/disable CMPS), and a constant current biasing scheme with a tunable external reference current used to set on-chip bias currents.

IV. Circuit Implementation

A. Overview of ADC Implementation

The overall ADC architecture of this work is similar to that of a conventional pipelined ADC, where the main difference is the addition of a state machine block to generate the power-on/off timing of the various subsystems in the pipelined ADC, as shown in Fig. 4. The pipeline sub-blocks shown in Fig. 6 consist of an ADC, DAC, 2 × gain, and sample-and-hold (S/H). The DAC, 2 × gain, and sample-and-hold are lumped into a single circuit referred to as the multiplying digital-to-analog converter

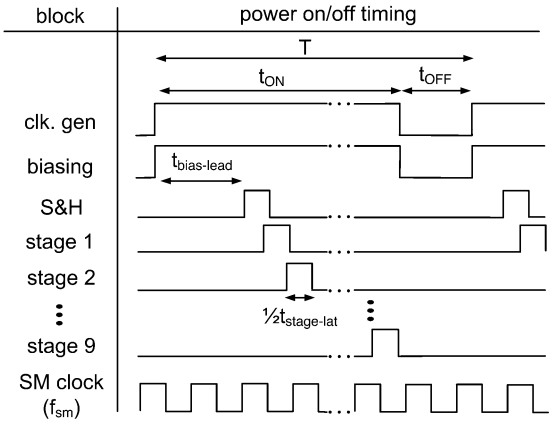

Fig. 4. Power-on/off timing of blocks in ADC when CMPS is enabled.

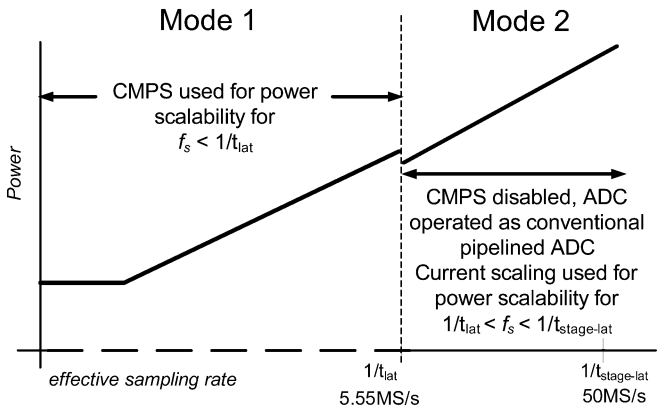

Fig. 5. Two modes of operation to allow for continuous power scalability.

(MDAC). The following sections detail the circuit implementation of each block in Fig. 3.

B. Stage ADC/Comparator Design

The pipeline ADC was implemented with a 1.5-bit architecture for stages 1–8, and a 2-bit flash ADC for stage 9. As digital error correction can be used to relax the matching constraints of comparators in the stage ADC (comparator offset can be as high as one quarter the full scale input), dynamic comparators were used to implement the flash ADC. Dynamic comparators trade higher offset with lower power consumption in comparison to active comparators (e.g., [7], [8]) which have lower offset and a higher power consumption. Dynamic comparators also have the advantage of only consuming power during logic transitions, hence, can be rapidly powered on/off by enabling/disabling the inputs to the comparator. Although several dynamic comparator architectures exist [9], a switched-capacitor-based dynamic comparator, as shown in Fig. 7 [9], was implemented in this work based on its favorable tradeoff between desired offset and power consumption. The threshold of the comparator is given by the ratio of C_{in} and C_{ref} in Fig. 7.

C. Front-End Sample and Hold

A commonly used sample-and-hold architecture with unity gain (e.g., [10]) was used before the first stage in the pipeline, as shown in Fig. 8. A front-end sample-and-hold prevents the

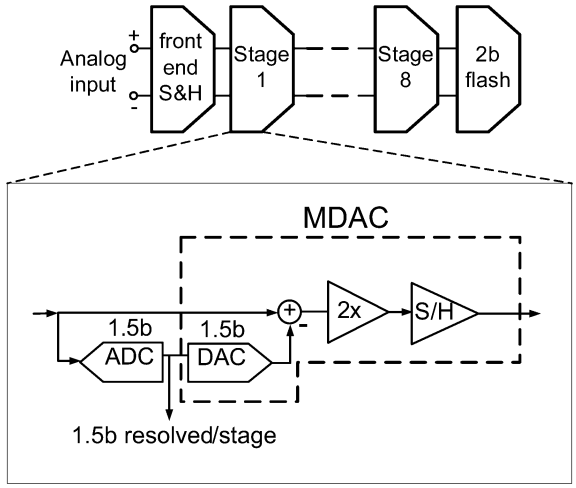

Fig. 6. Block diagram of sub-blocks in pipeline core.

MDAC and stage ADC in the first pipeline stage from operating on different analog inputs due to skew, hence, significantly minimizes errors in the output's MSB for high bandwidth inputs. Previous publications have shown a mix of ADCs with and without a front-end sample-and-hold for sampling rates on the order of 50 MS/s. In the interest of constant SNDR for input bandwidths up to $f_s/2$, as well as a more relaxed layout, a front-end sample-and-hold was used at the penalty of increased power consumption [11], [12].

Capacitor C_1 in Fig. 8 was sized to be 500 fF such that kT/C noise [13] contributed to less than contributed to less than one quarter of a least significant bit when input referred for a 1.6-V p-p differential input signal. The size of the input sampling MOS switches was such that the maximum RC time constant was sufficiently small to allow for a maximum sampling rate of 50 MS/s, and determined by simulation to be linear well beyond 10 bits.

D. Stage MDAC Architecture

Shown in Fig. 9, a commonly used architecture was used to implement the MDAC [6], [10], [14] of this work. The MDAC architecture has a large feedback factor hence fast transient response, and good matching due to identical capacitor sizes to realize a gain of two. As less accuracy is required by subsequent stages in the pipeline, capacitors C_1 and C_2 were scaled along the pipeline to minimize power consumption [11], [15], [16]. Determined by input-referred kT/C noise considerations $C_1 = C_2$ were sized to be 500, 100, and 50 fF for stages 1–2, 3–5, and 6–8, respectively, and implemented with MIM capacitors. MOS switches sizes were optimized for sufficiently low RC time constant delay, to attain a maximum sampling rate of 50 MS/s.

E. Rapid Power-On/Off Opamp for Front-End Sample and Hold, MDAC

From Figs. 8 and 9, to rapidly power-on/off the pipeline core using CMPS requires an opamp which also rapidly powers on/off. Opamps with the ability to power-on and off are seen in previous literature in the form of switched opamps [17] (e.g., [18]–[21]). A method used to modulate power in switched

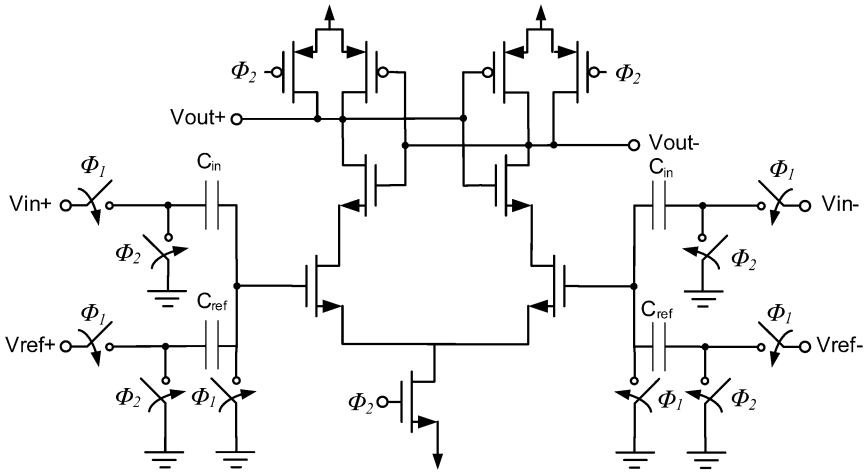

Fig. 7. Switched capacitor based dynamic comparator used in 1.5-bit, and 2-bit flash ADCs.

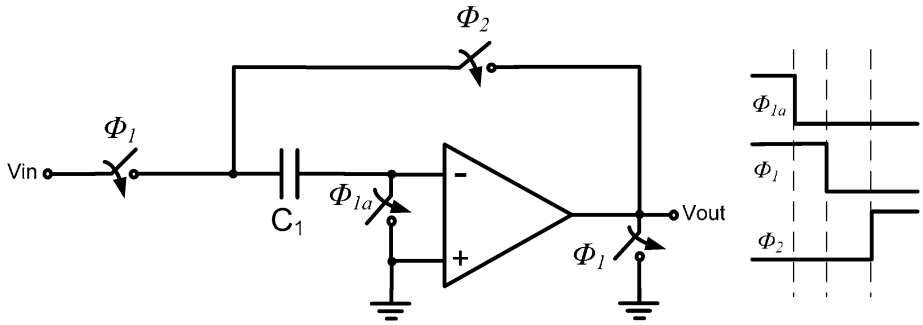

Fig. 8. Front-end sample-and-hold architecture (shown single-ended but implemented fully differentially).

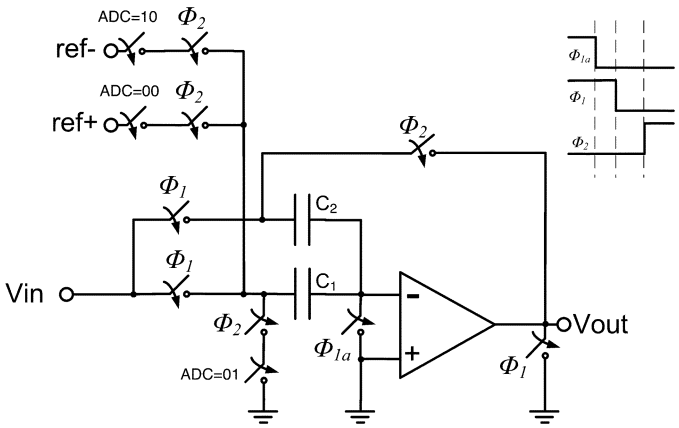

Fig. 9. MDAC architecture (shown single-ended but implemented fully differentially).

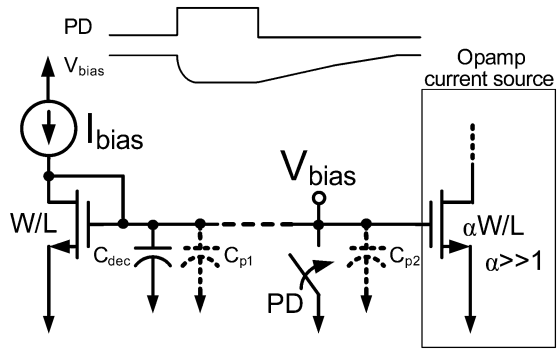

Fig. 10. Switched bias approach to modulate current source power (current source powers down on PD high).

opamps is to switch the bias voltage of an opamp's current source between the bias voltage and ground [17], [20] as shown in Fig. 10. Since bias nodes are typically loaded with large capacitors to decouple supply noise (on the order of picofarads; $C_{\rm dec}$ in Fig. 10) as well as parasitic capacitors (C_{p1}, C_{p2}), and are usually set by relatively small biasing currents (on the order of micro-amps; $I_{\rm bias}$ in Fig. 10), the slew time given by $t_{\rm slew} = (\Delta V)C/I$ required when powering on the opamp is excessive [21] for a $t_{\rm ON}$ of only $1/50$ MHz $= 20$ ns (noting that for a rapid power-on $t_{\rm slew} \ll t_{\rm ON}$). Thus, although a short power-off time is realized with switched biasing, in practice switching bias voltages results in slow opamp power-on time.

To alleviate slew-rate-limited power-on time, a feedback-based switching technique was developed to decrease slew time, and combined with a folded cascode opamp, as shown in Fig. 11. This approach buffers the bias voltage, allowing for a copy of the bias voltage loaded with a relatively small capacitance to be switched, rather than the original bias voltage which is loaded with a larger capacitance as shown in Fig. 12. Since the copied bias voltage is loaded with a much smaller capacitance than the original bias voltage, and can be set by a relatively large current, the slew time at the switching node is much shorter than if the original bias voltage were

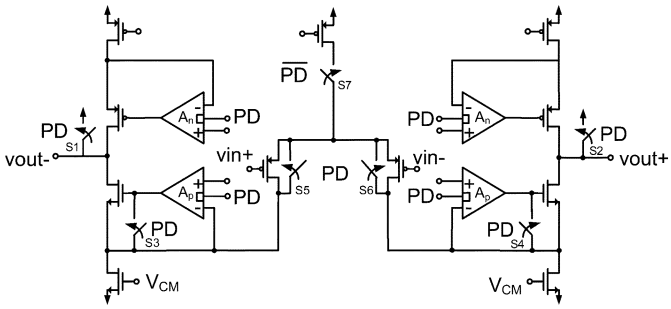

Fig. 11. Schematic of rapid power-on opamp.

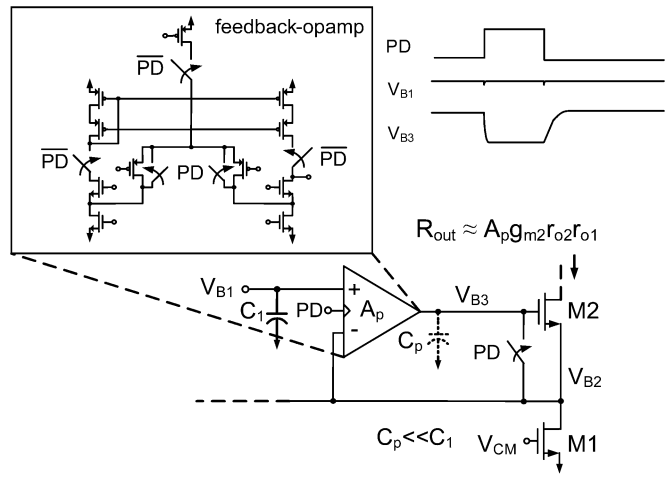

Fig. 12. Detail of current source in output of rapid power-on opamp.

switched. Furthermore, the large input resistance of the feedback opamp isolates the original bias voltage from switching induced perturbations, thus, maintains the original bias voltage at the nominal value over the entire switching interval.

An added advantage of this approach is the feedback increases the output resistance of the current source by the gain of the feedback-opamp (A_p in Fig. 12) [22]. When feedback based switching is combined with a single-stage folded cascode opamp, a DC gain-boosted architecture [23] results. As such, this approach satisfies two key design criteria for the opamp of this work: a short power-on time, and large DC gain to minimize MDAC gain errors [22]. Furthermore, as a large gain is realized in only a single stage, simple load compensation and passive common-mode feedback are afforded, simplifying the design. A passive common-mode-feedback circuit based on [18] was used in this work. As less settling accuracy is required by subsequent MDACs in the pipeline, the DC gain of the MDAC opamps were scaled to be 105, 73, and 52 dB for stages 1–2, 3–5, and 6–8, respectively, noting that large DC gains were used to minimize opamp DC gain induced nonlinearity errors. Opamp bandwidths were also designed to exceed minimum design constraints such that in simulation the settling accuracy was 12 bits for stages 1–2, 10 bits for stages 3–5, and 7 bits for stages 6–8. To reduce design complexity, the opamp of the first stage in the pipeline was re-used in the front-end sample-and-hold. Switches S1–S4 in Fig. 11 were used to decrease the time required to power off the opamp, and switches S5 and S6 to avoid floating nodes when the opamp powers off.

To power off the feedback-opamp during t_{OFF}, MOS switches in series with the feedback- opamp's current sources (e.g., [18], [19]) were used as shown in Fig. 12. Series current switching allows for rapid power on/off of the feedback-opamp as bias voltages are not perturbed during switching events. The small-signal swing requirements of the feedback-opamp allow for voltage drops across the series resistance of the switches to have a negligible impact on the feedback-opamp's performance.

An alternative to using feedback-based switching in the main opamp would be to use series current switching for rapid opamp power-on. Series current switching was not used in the current sources at the output of the main opamp in the interest of maximizing the opamp's signal swing, and realizing a large DC gain in only a single stage. All tail current transistors in both the feedback and main opamp, however, used series current switching (S7 in Fig. 11 for the main opamp), as opamp output signal swing is minimally affected by IR drops in the tail current path.

F. Reduced Power Consumption With Rapid Power-On/Off Opamps

By powering off both the main opamp and the feedback opamps, the opamp of this work completely powers off during t_{OFF}. An advantage of an opamp which rapidly and completely powers on and off is that it can be rapidly powered on only when needed, and powered off when not required in high-speed applications. The sample-and-hold and MDAC circuits of this work only require the opamp during the hold state, hence, to further reduce power, the opamps are powered off during the sampling phase of the MDACs and sample-and-hold. To quantify the amount of power reduction afforded by powering off the opamps during the sampling phase, in the ADC mode in which CMPS is disabled, the opamps can be programmed to be powered on or off during the sampling phase. As high-speed ADCs typically do not completely power off the opamps during the sampling phase, by measuring ADC power with the opamps always on and always off in the sampling phase, respectively, the power savings afforded can be measured. Thus, the ADC of this work has a total of three modes of operation (where the specific mode is set by programming the state machine with external control bits).

Mode 1: CMPS enabled (used for sampling rates up to 5.55 MS/s):

i) CMPS used to achieve power scalability, i.e., state machine enabled;
ii) opamps only powered-on during hold phase in MDAC and sample-and-hold to reduce power.

Mode 2: CMPS disabled, pipelining enabled (used for sampling rates between 5.55 and 50 MS/s):

i) bias current scaling used to achieve power scalability, i.e., state machine disabled;
ii) opamps powered *off* during sampling phase in MDAC and sample-and-hold to reduce power.

Mode 3: CMPS disabled, pipelining enabled (used for sampling rates between 5.55 and 50 MS/s):

i) bias current scaling used to achieve power scalability, i.e., state machine disabled;
ii) opamps powered *on* during sampling phase in MDAC and sample-and-hold to compare power reduction with mode 2.

To minimize the impact of supply variations induced by rapidly modulated currents (*Ldi/dt* supply noise [24]), a mix of decoupling MOS and MIM capacitors [24] were placed between $V_{\rm DD}$ and $V_{\rm SS}$ in all noncircuit-occupied areas in the fabricated chip. The total decoupling capacitance was on the order of 100 pF.

G. Biasing Circuitry

The rapid power-on opamp developed in Section IV-E relies on bias voltages which are well settled before the opamp is required to power-on. As bias generating circuits have long power-on times, they are powered-on before the front end sample-and-hold as shown in Fig. 4. The lead time ($t_{\rm bias\text{-}lead}$ in Fig. 4, which is digitally programmable in the state machine) required for bias circuits to settle increases the minimum latency of the pipeline ADC when operating with CMPS from 4.5 to 9 clock cycles of the state machine's clock. Thus, the minimum amount of current scaling required for continuous power scalability is for sampling rates between 50 MS/s and $50/9 = 5.55$ MS/s (i.e., only 1:9). Bias circuits are powered on/off by using switches in series with biasing currents.

H. Digital State Machine and Non-Overlapping Clock Generator

A digital state machine is used to sequence the power-on times of each pipeline stage according to the timing of Fig. 4, where $t_{\rm OFF}$, and thus, T, is digitally programmable. The settling time for each stage $(t_{\rm stage})$ is equal to the pulsewidth of the clock supplied to the state machine $(f_{\rm sm})$. As the state machine consumes power during $t_{\rm OFF}$, it limits the lowest power achievable with CMPS. By reducing $f_{\rm sm}$ however, the power of the state machine can be reduced; e.g., with $f_{\rm sm} = 50$ MHz, the state machine consumes 460 μW; with $f_{\rm sm} = 1$ MHz, the power is reduced to only 9 μW. The state machine was designed without commercial standard cells. It is conceivable that if power-optimized standard cells were used to implement the state machine, its power could be further reduced, thus increasing the power-scaleable range.

Non-overlapping clocks required for the sample-and-hold and MDACs were generated using a commonly used nonoverlapping clock generator (e.g., [10]). The block's power was modulated by passing/blocking the input clock (from an off-chip clock generator) via a transmission gate. The clock input to the nonoverlapping clock generator was the same clock provided to the state machine, i.e., $f_{\rm sm}$.

I. Digital Error Correction/Reference Voltages

To make the prototype easily testable, digital error correction and reference voltages were implemented off-chip. For digital error correction, the digital output from each pipeline stage was routed off chip, where a Matlab script was written to emulate digital error correction on the captured digital output. With the output of each stage available off chip, the functionality of each pipeline stage could be quickly verified. The power consumption of the error correction and reference voltage blocks are not included in the measured results.

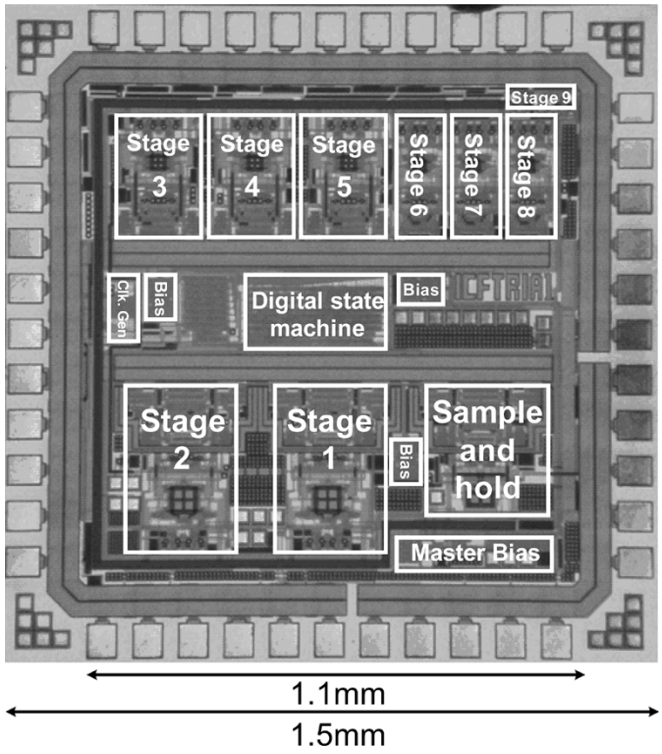

Fig. 13. Photograph of fabricated chip.

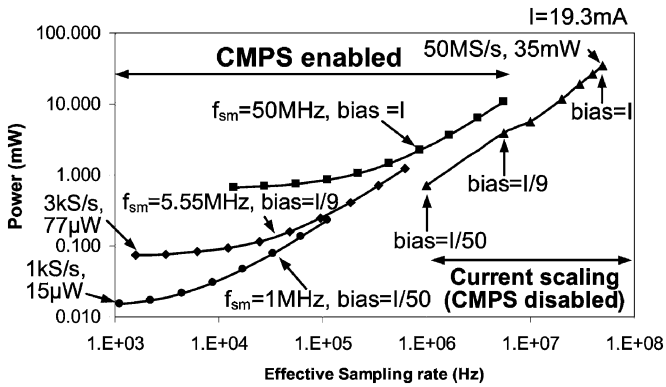

Fig. 14. Measured power versus sampling rate between 1 kS/s and 50 MS/s.

V. Measured Results

A prototype of the power-scaleable ADC was fabricated in a 1.8-V 0.18-μm CMOS process, and packaged in a standard 44-pin CQFP package. The active area of the prototype was 1.2 mm^2, and is shown in Fig. 13.

A. Measured Power and Accuracy

Fig. 14 shows the power of the ADC versus sampling rate between 1 kS/s and 50 MS/s. The measured power includes all blocks shown in Fig. 3 except off-chip blocks (which are shown in dashed boxes). With CMPS disabled, the power of the ADC at the maximum sampling rate of 50 MS/s was 35 mW. Using

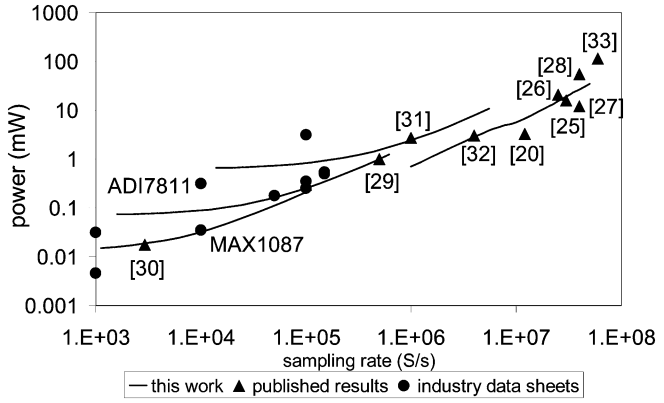

Fig. 15. Comparison of power of this work versus recently published and commercial 10-bit ADCs.

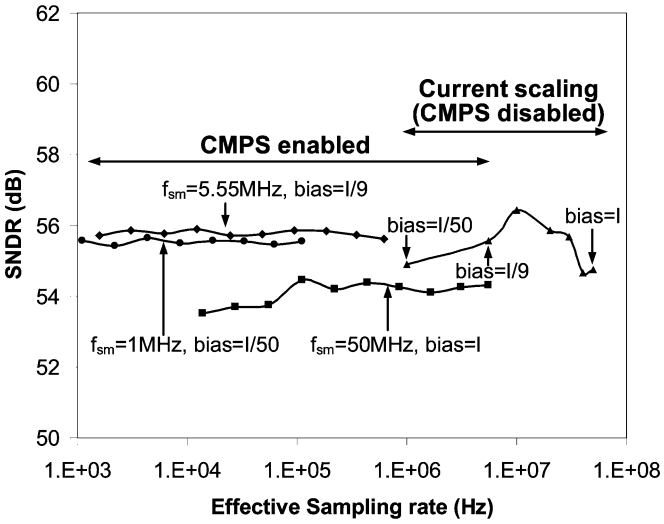

Fig. 16. Measured SNDR versus sampling rate between 1 kS/s and 50 MS/s.

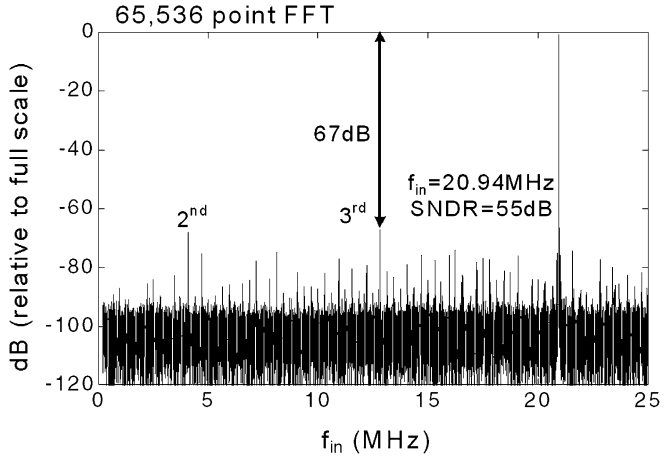

Fig. 17. FFT of digital output at 50 MS/s.

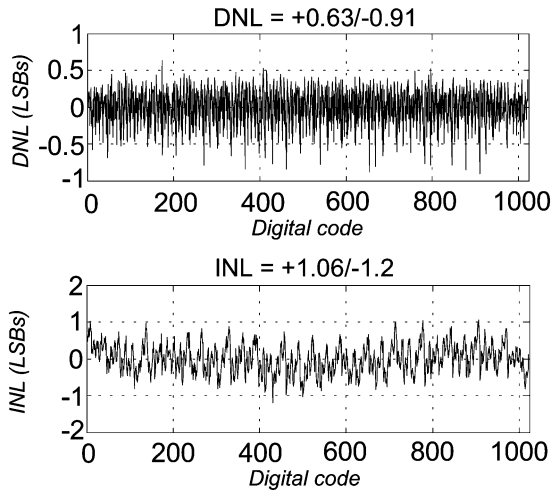

Fig. 18. DNL and INL at 50 MS/s.

fixed bias currents and enabling CMPS with a 50–MHz clock, the power of the ADC was scaleable with sampling rate from ~100 kS/s to 5.55 MS/s. As described in Section IV-H, the power-scaleable range of the ADC is limited at lower sampling rates by the power of the state machine. To have a continuous power-scaleable range as shown in Fig. 5, the bias currents were scaled by a factor of nine between 50 and 5.55 MS/s, where the power for a given sampling rate is shown in Fig. 14. Note when CMPS is disabled, the power shown in Fig. 14 is of mode 2, i.e., opamps powered off during the sampling interval. When CMPS is applied to the current scaled sampling rate of 5.55 MS/s (i.e., 1/9th the bias current of 50 MS/s, and a state machine clock of 5.55 MHz), the power of the ADC was scaleable between 617 and 3 kS/s, where only 77 μW was consumed at 3 kS/s. To emphasize the power-scaleable range enhancement afforded by CMPS, bias currents were further reduced to 1/50th the bias current of 50 MS/s and CMPS applied to the current scaled sampling rate of 1 MS/s (i.e., 1-MHz state machine clock), where the ADC was measured at 1 kS/s to consume only 15 μW (of which 9 μW was due to the digital state machine). Thus, although bias currents are scaled by a factor of 50, by additionally using CMPS, the power-scaleable range is enhanced 50 times, yielding a total power-scaleable range of $50 \times 50 = 2500$. The ultimate limit in power-scaleable range is constrained by the power consumption of the digital state machine, and the maximum amount of current scaling tolerable by a given application.

Fig. 15 compares the power of the ADC of this work versus recently published and commercial 10-bit ADCs between 1 kS/s and 50 MS/s. The similar power consumption compared to a broad array of 10-bit ADCs over a wide variation in operating speed verifies the techniques used in this work to achieve power scalability are both effective at realizing a wide power-scaleable range as well as attaining a low power for a given sampling rate.

Fig. 16 shows the measured SNDR of the ADC between 1 kS/s and 50 MS/s. For all sampling rates, the SNDR is between 54 and 56 dB, and is virtually constant for a given $f_{\rm sm}$ due to the fixed bias currents between different sampling rates.

Fig. 17 shows a 65 536 point fast Fourier transform (FFT) of the digital output at the maximum speed of 50 MS/s, where an SNDR of 55 dB was measured with a 1.6-V p-p input sinusoid at 20.94 MHz. The SFDR at 50 MS/s was measured to be 67 dB. Fig. 18 shows the measured DNL and INL at 50 MS/s, where the peak INL was $+1.06/-1.2$ LSB, and peak DNL $+0.63/-0.91$ LSB.

TABLE I
ACCURACY AND POWER MEASUREMENTS OF ADC IN MODE 2 (OPAMPS POWERED OFF DURING SAMPLING PHASE) AND MODE 3 (OPAMPS POWERED ON DURING SAMPLING PHASE)

Accuracy and Power measurements of ADC						
f_s	f_{in}	*SNDR (dB)*		*Power (mW)*		*Power*
(Msps)	*(MHz)*	*Mode2*	*Mode3*	*Mode 2*	*Mode 3*	*reduction*
1	0.17	55	55	0.7	1.1	32%
5.55	2.50	56	55	4.0	5.7	30%
10	4.75	56	55	5.4	7.4	27%
20	9.54	56	55	12	16	25%
30	14.01	56	54	19	25	24%
40	19.01	55	53	26	34	23%
50	20.94	55	52	35	44	21%

B. Comparison of Power in Mode 2 and Mode 3

To measure the amount of power reduction afforded by powering off the opamps during the sampling phase, the power of the ADC was measured in mode 2 and mode 3 (as described in Section IV-F). The power and accuracy for current scaled sampling rates between 1 MS/s and 50 MS/s using modes 2 and 3 are compared in Table I. For a given sampling rate, the master off-chip reference current is identical between modes 2 and 3, i.e., both modes have the same bias currents. The measured results show the total power of the ADC is reduced between 20%–30% by powering off the opamps during the sampling phase, without compromising accuracy in the ADC. The amount of power saving is limited by the percentage of total power the opamps consume, and the nonoverlap time of the nonoverlapping clock generator (nonoverlap time reduces the hold phase to less than 50% of the total period) [34]. Higher sampling rates show less power reduction in mode 2 as the fixed nonoverlap time of $\sim$1.4 ns in this work is a larger percentage of the sampling period for faster clock rates. A small difference between measured SNDR in modes 2 and 3 at higher sampling rates was attributed to a clocking oversight which slightly reduced the available settling time (hence, settling accuracy) by a fixed amount in mode 3 compared to mode 2 [34].

As many switched-capacitor architectures have times in which the opamp is idle, it is conceivable the techniques used to rapidly power on/off the opamp of this work could be used to reduce power consumption in other high-speed switched-capacitor circuits.

VI. CONCLUSION

A power-scaleable pipelined ADC which achieves a wide power-scaleable range without commensurate variations in bias current has been presented. By minimizing the required bias current variation for a wide power-scaleable range, poorer yield due to weak inversion can be avoided. The keys to power scalability at high sampling rates were the use of a current-modulation-based architecture, and the development of a novel rapid power-on opamp, which by virtue of a feedback approach is able to completely and quickly power on/off. Measured results from a prototype fabricated in 0.18-μm CMOS show the combination of CMPS and current scaling result in the ADC having a power that is a function of sampling rate between 1 kS/s (15 μW), and 50 MS/s (35 mW) while maintaining an SNDR of 54–56 dB over the entire power-scaleable range. The rapid power-on opamp of this work was also shown to allow for reduced power consumption in high-speed switched-capacitor circuits, where by powering off the opamps during the sampling phase of the pipeline's sample-and-holds, a 20%–30% reduction in power could be obtained. Table II summarizes the key measured results of this work.

TABLE II
SUMMARY OF ADC PERFORMANCE

Technology	1.8V, 0.18µm CMOS
Resolution	10 bit
Full scale input	1.6V p-p
Area	1.2mm^2
f_s *(power) range*	1kS/s (15µW) - 50MS/s (35mW)
bias current scaling	1:50

Performance at 50MS/s	
Power	35mW
SNDR (f_{in}*=20.94MHz)*	55dB (8.8ENOB)
SFDR (f_{in}*=20.94MHz)*	67dB
DNL/INL	+0.63/-0.91, +1.06/-1.2

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