Charge-pump based switched-capacitor integrator for ΔΣ modulators

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A low power switched-capacitor (SC) integrator based on a capacitive charge-pump (CP) is proposed. The CP integrator circuit consumes approximately a quarter of the power of a conventional SC integrator while maintaining the same thermal noise performance. Power consumption of the CP integrator is analysed and compared with a conventional parasitic-insensitive integrator. Simulation results verifying the thermal noise and settling performance of the CP integrator are also provided.

Introduction: In a switched-capacitor (SC) delta-sigma (ΔΣ) analogue-to-digital converter (ADC) with a large oversampling ratio (OSR), the first integrator of the loop filter is typically the largest consumer of power in the ADC. Without the noise shaping effect for the first integrator, maintaining thermal noise floor below the overall accuracy requirement of the modulator puts severe demands on the operational transconductance amplifier (OTA) power consumption. More specifically, sampling capacitors are sized to achieve sufficiently low thermal noise and for a given sampling rate and settling accuracy this translates to certain bandwidth and power dissipation for the first integrator OTA [1]. This Letter describes a circuit technique using capacitive charge-pumps, to maintain the thermal noise performance of the integrator while reducing its power dissipation to approximately a quarter of that of a conventional parasitic-insensitive SC integrator.

Proposed charge-pump (CP) integrator: The circuit diagram of a conventional parasitic-insensitive SC integrator with an integrator coefficient of k is shown in Fig. 1*a*. The proposed CP integrator circuit is shown in Fig. 1*b*. In this circuit, during Φ_1 the sampling capacitor is divided into two halves $C_{S1} = C_{S2} = C_S/2$. During Φ_2, C_{S1} and C_{S2} are connected in series and discharged into the integrating capacitor, $C_I = C_S/2k$, through the virtual ground of the OTA. In this phase, $2V_{DAC}$ is applied in order to integrate $V_{in} - V_{DAC}$. Ignoring parasitic capacitances, series connection of the sampling capacitors implements a passive gain of two for the input voltage, which is stored across an equivalent input capacitance of $C_S/4$. The integrator coefficient in this case can be shown to also equal k.

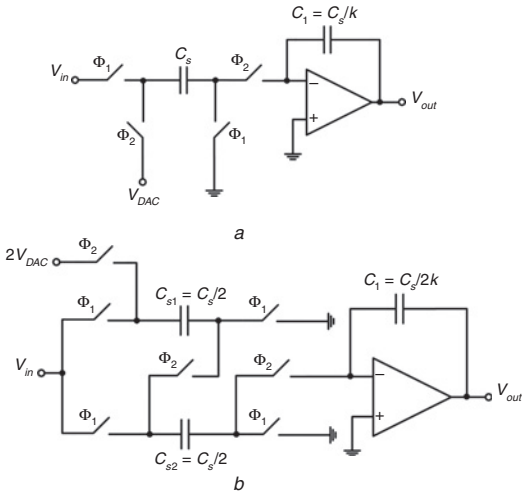

Fig. 1 *CP SC integrator circuits*

a Conventional CP
b Proposed CP

The idea can be further extended by splitting the sampling capacitor C_S into $n > 2$ capacitors during Φ_1. In Φ_2 the n sampling capacitors are connected in series and driven by the feedback voltage nV_{DAC}. The integrating capacitor in this case is equal to $C_I = C_S/nk$. It can be shown that this approach ideally reduces the power consumption of the OTA by $1/n^2$. In this Letter, however, we focus only on splitting C_S into two capacitors C_{S1} and C_{S2}.

Power consumption analysis: For a single-stage OTA the input differential pair transconductance (g_m) is proportional to the power consumption of the amplifier. Since the input differential pair transistors are typically biased in weak inversion, their transconductance is linearly proportional to their bias current, which is a fixed percentage of the OTA total bias current. The required OTA transconductance can be calculated from the feedback loop parameters as [2]:

$$g_m = \frac{\omega_{-3\text{dB}} C_L}{\beta} \tag{1}$$

where $\omega_{-3\text{dB}}$ is the closed-loop -3 dB frequency, C_L is the load capacitance and β is the feedback factor. The required closed-loop -3 dB frequency is determined by the modulator sampling rate and the integrator settling accuracy specification. The load capacitance C_L and the feedback factor β, however, depend on the integrator circuit architecture. To reduce power one should minimise C_L and maximise β.

Ignoring parasitics and assuming the capacitor loading of the second stage integrator in a ΔΣ loop is negligible due to noise shaping, the effective capacitive load seen by the OTA is equal to the series combination of the feedback capacitor and the input capacitor [2]. For the conventional integrator during Φ_2, C_L and β are found to be

$$C_{L,Conv} = \frac{1}{k+1} C_s, \quad \beta_{Conv} = \frac{1}{k+1} \tag{2}$$

For the CP integrator they are given by

$$C_{L,CP} = \frac{1/2}{k+2} C_s, \quad \beta_{CP} = \frac{2}{k+2} \tag{3}$$

Equations (2) and (3) show that for the same sampling capacitance C_S, the ratio C_L/β in the CP integrator is a quarter of the conventional integrator.

In terms of thermal noise, during Φ_1 the CP integrator samples the same amount of thermal noise as during Φ_1 in the conventional integrator. During Φ_2, the CP integrator has four times the thermal noise of the conventional integrator, owing to the series capacitance of C_{S1} and C_{S2}. However, at this time, the input signal has seen a gain of two and so the CP integrator has the same input-referred noise as the conventional integrator. Hence sampling capacitors (C_S) of equal size can be used in both circuits to meet the thermal noise specification. In this case, for the same sampling rate and settling accuracy, the required OTA transconductance (g_m) in the CP integrator is a quarter of the conventional integrator, which results in a significant power savings of 75% for the CP integrator.

The above analysis assumed linear settling for the OTA and did not account for partial slew-rate settling, but fortunately the CP integrator's lower capacitive load also helps in a slew-rate limited case. Also, the performance improvement discussed above did not take into account the effect of parasitic capacitances. In practice, parasitic capacitors at various nodes can degrade the power savings to less than 75% by increasing the input-referred thermal noise of the CP integrator. Parasitic capacitances can also cause distortion if they are nonlinear. However, in applications with small input signals, such as wireless and sensory systems, performance is fundamentally limited by thermal noise as opposed to linearity. In this case, simulations show promising results for the CP integrator achieving the same performance as the conventional integrator at the cost of significantly less power.

Simulation results: The proposed CP integrator was simulated in Spectre and its thermal noise and settling performance were compared to those of a conventional SC integrator. The integrators were employed as the first stage in a second-order low-distortion ΔΣ modulator [3] utilising a five-level quantiser. Of the two integrator circuits, the OTAs and the capacitors were realised using transistors and metal-insulator-metal (MIM) capacitors, respectively, from a typical 0.13 μm CMOS process. To reduce transient noise simulation time switches of the first stage were modelled behaviourally as ideal switches in series with their on-resistance, which included thermal noise. The single-stage fully-differential OTAs used a folded-cascode architecture with one being four times larger (4X OTA) than the other (1X OTA), hence dissipating four times more power. Transistor thermal noise for the OTAs was also included in the simulations. Circuits other than the first stage integrators were implemented in behavioural form and their thermal noise contribution was assumed to be negligible owing to noise shaping [4].

The modulator input sine-wave was 320 mV peak-to-peak differential (80% of a 400 mV reference voltage). The sampling capacitors of the first integrators were sized as $C_S = 8$ pF to achieve a thermal noise SNR of 89 dB at OSR = 128. To demonstrate the advantage of the CP integrator compared to the conventional SC integrator, modulator performance was evaluated when the following three circuits were used for the first stage integrator: (i) conventional integrator with the 4X OTA (Conv/4X), (ii) CP integrator with the 1X OTA (CP/1X) and (iii) conventional integrator with the 1X OTA (Conv/1X).

Fig. 2 shows the SNDR performance of the three modulators against the sampling rate for a fixed input signal bandwidth. To obtain the SNDR of each data point, 256 × OSR samples were taken to calculate the fast Fourier transform (FFT). At sampling frequencies up to $F_s = 10$ MHz, where quantisation noise is dominant over thermal noise and distortion owing to the OTA's insufficient settling, all three modulators achieve almost the same SNDR. Also, at $F_s = 20$ MHz SNDR remains the same for the three modulators, as it is mainly limited by thermal noise. As the sampling rate increases to $F_s = 40$ and 50 MHz, the SNDR of Conv/4X and CP/1X modulators remains thermal noise limited and therefore the SNDR increases at a rate of approximately 3 dB/Octave rate. However, at these frequencies the Conv/1X integrator becomes severely limited by the OTA's settling distortion and hence its modulator SNDR drops significantly.

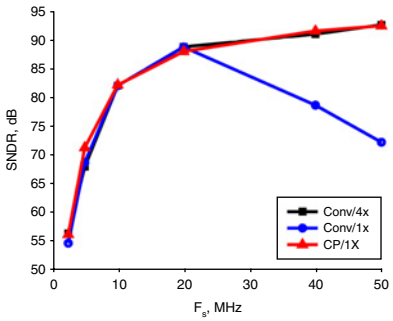

Fig. 2 *Simulated SNDR comparison for second-order ΔΣ modulator employing Conv/4X, CP/1X and Conv/1X integrators as first integrating stage*

Conclusion: A new CP based SC integrator is proposed. It is shown by analysis and simulations that for the same sampling rate, thermal noise and settling accuracy requirements, the CP integrator requires approximately a quarter of the power of a conventional SC integrator.

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One or more of the Figures in this Letter are available in colour online.

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