A Flexible Charge-Balanced Ratiometric Open-Loop Readout System for Capacitive Inertial Sensors

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***Abstract*—This brief presents an open-loop readout circuit for capacitive accelerometers. It combines a ratiometric approach with charge balancing for high linearity. The charge balance is implemented with a delta–sigma loop that acts as an analog-to-digital converter for a readout signal. The system avoids the low-signal-tone power levels present in current charge-balanced implementations, making it a flexible readout technique for accelerometers with varying sensitivities and dynamic ranges.**

***Index Terms*—Accelerometers, capacitive sensors, charge balance, gyroscopes, interface circuits, ratiometric, readout circuits.**

I. Introduction

In the past decade, there has been a proliferation of the use of inertial sensors in electronic devices. Applications have ranged from picture stabilization in digital cameras to fall detection in laptops and gaming control for smartphones and tablets. This, in turn, has led to renewed research interest in the design and implementation of the readout circuits that accompany such sensors. By designing interface circuits with better performance, manufacturing tolerances on the sensor component can be relaxed, leading to lower system costs.

Readout techniques can be categorized from the system level as either open loop [1]–[5] or force-feedback closed loop [6]–[11]. Fig. 1 shows a review of readout circuits with linearity and the power per unit of the bandwidth for recent publications and the proposed system. This figure shows that closed-loop force-feedback systems offer high linearity, but their high power consumption makes them impractical for some applications. On the other hand, open-loop readout circuits have lower linearity while operating at lower power compared with closed-loop systems. Therefore, there is an incentive to design readout circuits that achieve high linearity comparable with closed-loop systems while operating at low power. This would greatly improve on existing applications while allowing other applications such as dead reckoning to be more economical. Toward this goal, we propose a highly linear readout system based on a ratiometric and charge-balanced output. The circuit operates as a delta–sigma analog-to-digital converter (ADC) but is open loop in nature, allowing for lower power consumption than its force-feedback counterparts. Moreover, the readout system is flexible and can adapt to a wide range of sensor specifications without the need to redesign the front-end circuitry.

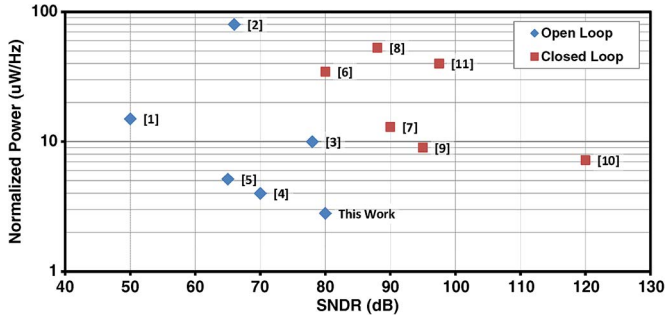

Fig. 1. SNDR versus the normalized power in recent publications and of the proposed system.

This brief is organized as follows. Section II discusses the use of high-linearity readout techniques and the current shortcomings of these circuits. Section III then proposes a new system architecture with analysis and simulation results. Section IV analyzes the noise of the system, whereas Section V analyzes the effect of parasitic capacitance. Concluding remarks are then made in Section VI.

II. High-Linearity Design Approach

A differential capacitive accelerometer has two sets of sense capacitors with a nominal capacitance of C_s at rest. Once the sensor undergoes acceleration, each sense capacitance differentially changes according to

$$C_s^+ = \frac{C_s}{1-\frac{x}{d}} \qquad C_s^- = \frac{C_s}{1+\frac{x}{d}}$$

where x is the displacement due to acceleration, and d is the equivalent distance between each capacitor plate at rest. To achieve high linearity, readout circuits should make use of two techniques, i.e., ratiometric and charge-balanced outputs. In ratiometric implementations, the output signal is the ratio between the differences in sense capacitances over its sum. Such a technique results in an output that is linearly proportional to the acceleration as follows:

$$V_{\text{out}} \propto \frac{C_s^+ - C_s^-}{C_s^+ + C_s^-} \propto \frac{x}{d} \propto \frac{a}{d\omega_n^2} \tag{1}$$

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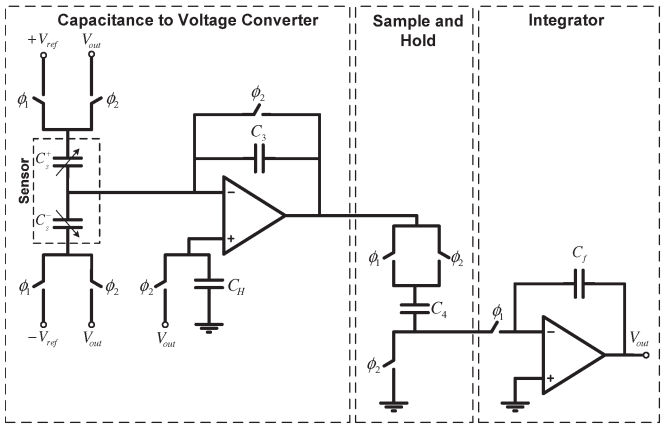

Fig. 2. Simplified Leuthold–Rudolf integrator, which is a charge-balanced readout circuit first presented in [14].

where a is the acceleration, and ω_n is the natural frequency associated with the mechanical resonance of the sensor.

Equation (1) may suggest that any circuit that achieves a ratiometric output is highly linear. This, however, is not the case. The caveat is that readout techniques inevitably involve placing a potential on one and/or both plates of a sense capacitor. The force acting on the capacitor is given by [12]

$$F = \frac{A\epsilon_r\epsilon_0}{2d^2}V^2 \tag{2}$$

where V is the potential difference across the capacitor, ϵ_0 is the permittivity of free space, ϵ_r is the relative permittivity, and A is the equivalent plate area of each sense capacitor. When the sense capacitors undergo acceleration, the capacitance changes in opposite directions; therefore, the electrostatic force on each capacitor is slightly different. These forces in turn cause an unwanted displacement on the sense capacitors, with the effect of creating even and odd harmonics mitigating any benefits of the ratiometric technique [13].

Charge-balanced readout techniques aim to modify traditional readout techniques by dynamically adjusting the voltage across each sense capacitor such that the charge and, hence, the force on each capacitor is equal; therefore, the displacements are equal and do not affect the output. The concept is based on some form of feedback where the output voltage is fed back as a charge difference on the input. The difference in voltage is then integrated, and the output is adjusted. Despite the use of feedback, these techniques are still considered open loop since the feedback is not used to cancel the movement of the capacitive plates. One of the earlier types of charge-balanced readout circuits is the Leuthold–Rudolf integrator [14]. The circuit is a switch-capacitor-based analog feedback system. A simplified version of the circuit is shown in Fig. 2.

The analysis of this circuit shows that its output is given by

$$V_o(z) = V_{\text{ref}}\frac{C_s^+ - C_s^-}{\frac{C_f}{C_4}C_3}\frac{z}{z-\left(1-\frac{C_s^+ + C_s^-}{C_f}\frac{C_4}{C_3}\right)} \tag{3}$$

where V_{ref} is a dc reference voltage. Note that, at the dc $(z=1)$, we have a ratiometric output.

TABLE I
ACCELEROMETER SPECIFICATIONS USED FOR SIMULATIONS

Parameter	Symbol	Value
Capacitance at rest	C_s	500 fF
Capacitive sensitivity	$\frac{C_s^+ - C_s^-}{a}$	7.1 fF/g
Natural frequency	ω_n	3.2 kHz
Displacement at rest	d	3.50 μm
Effective Area	A	1.98×10^{-7} m^2
Accelerometer mass	m	$2.5\times10^{-8}kg$
Spring constant	k	10 N/m
Damping coefficient	b	$9.0\times10^{-4}Ns/m$

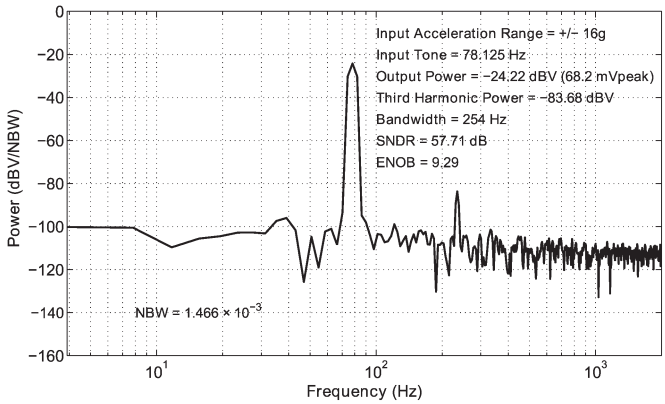

Fig. 3. Output power spectral density of the Leuthold–Rudolf charge-balanced circuit (see Fig. 2) with switch thermal noise. The number of points used in the fast Fourier transform (FFT) is 2^{10}.

Despite their fundamental merits, present charge-balanced techniques suffer from a low-output-signal power level. To demonstrate this phenomenon, a simulation of the Leuthold–Rudolf integrator using an accelerometer with the specifications in Table I was performed. The accelerometer was modeled by a mass–damper–dashpot system [2]. Mechanical systems have a thermal noise component called Brownian noise with a white spectral density [12], and this noise was modeled with a resistor of appropriate value. To include the effect of the force due to the voltage difference across the capacitor and the Brownian noise, the corresponding force was calculated at each time step using (2) and then, it was divided by the mass and applied as an external acceleration to the system.

The simulation uses an input acceleration of $\pm16g$ (where $g=9.8$ m/s^2) corresponding to a differential capacitance $(C_s^+ - C_s^-)$ of approximately 114 fF. Reference voltage $V_{\text{ref}}=600$ mV, $C_3 = 500$ fF, $C_4 = 100$ fF, $C_f = 500$ fF, and the sampling frequency is Fs $= 4000$ Hz. With these numbers, the integrator has a 3-dB bandwidth of 254 Hz [14].

The operational amplifiers (op-amps) in the simulation are designed to settle with a bandwidth of 15 bits, and their noise contribution (1/f and thermal noise) is disabled. The only source of noise is therefore that of the switch resistance, with switch sizes chosen for a 15-bit settling. This setup ensures that the obtained results are the best possible signal-to-noise-and-distortion ratio (SNDR) that can be achieved for the Leuthold–Rudolf architecture with the given sensor specification and dynamic range.

The simulation is shown in Fig. 3. The output spectrum shows that, despite being ratiometric and charge balanced, the

system only achieves a 58-dB SNDR. The problem is the small output power level in the fundamental tone, which is -24 dB full scale. Intuitively, this small power level can be explained by the fact that the signal is proportional to the differential sense capacitance, whereas the feedback is proportional to the sum of the sense capacitance. Therefore, depending on the sensitivity and size of the capacitors, the feedback may be too large and may reduce the output signal level.

The only parameter to increase the output signal is the reference voltage, and this is limited both from the perspective of the available on-chip supply and, more importantly, from the perspective of the pull-in phenomenon associated with the mechanical capacitors [12].

Over the years, other charge-balanced and ratiometric readout circuits have been implemented [4], [15]. However, the feedback mechanism is similar to the Leuthold–Rudolf integrator; therefore, the systems also suffer from low fundamental tone power. When low-sensitivity accelerometers are used, the power level is considerably low relative to the full scale. Although high-sensitivity accelerometers are available, it may be advantageous to only use a fraction of the possible range since accelerometers suffer worse linearity at higher deflection. In either case, a flexible technique that can make use of the benefits of charge balance for accelerometers for varying sensitivities and dynamic ranges is needed.

III. Proposed System

A. Dual Phase Input and Feedback

To overcome the problem with low output signal power, the feedback mechanism must be decoupled from the input such that its value can be adjusted independently. It is proposed to sample the signal in four phases. In one set of phases, the difference in the sense capacitors is sampled and amplified. In the next set of phases, one of the sense capacitors is sampled, the value is then compared with the sampled signal, and the output is adjusted accordingly. Therefore, the reference voltages for the input and the feedback can be now independently set, and the low-signal-power problem is avoided.

B. Discrete Feedback

Feedback can be accomplished as continuous or discrete. A benefit of discrete time is that the digitization of a capacitive analog signal can be accomplished rather than using a separate ADC. Since the feedback then becomes pulse density modulated, the readout circuit effectively acts as a delta–sigma ADC.

C. Implementation and Analysis

A block diagram of the proposed system is shown in Fig. 4, and the corresponding circuit implementation of the system is shown in Fig. 5. The system can be also extended to higher order delta–sigma loops to increase the ADC resolution.

The operation of the circuit can be looked at from a charge-balanced equation. Over a period of N cycles, the feedback will be high for n cycles and low for $N-n$ cycles. The negative

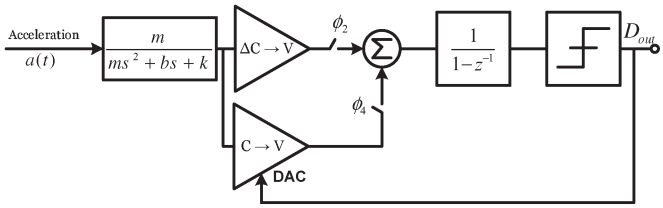

Fig. 4. Block diagram of the proposed system.

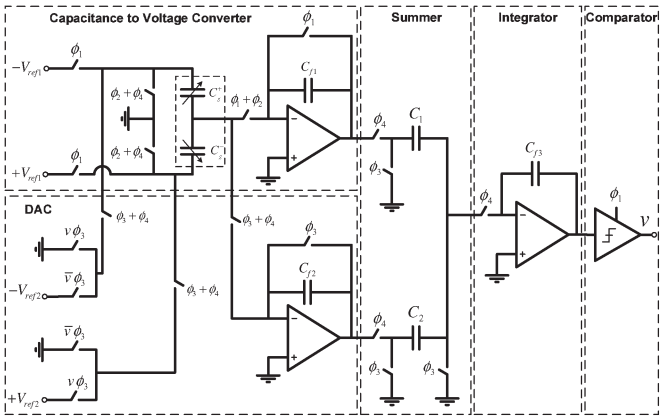

Fig. 5. Circuit implementation of the proposed system. The actual implementation makes use of correlated double sampling but is not shown for simplicity.

feedback causes the total charge at the input of the integrator to be zero; therefore, the following equations can be applied:

$$-nV_{\mathrm{ref}_2}C_s^-\frac{C_2}{C_{f_2}}+(N-n)V_{\mathrm{ref}_2}C_s^+\frac{C_2}{C_{f_2}} + NV_{\mathrm{ref}_1}\left(C_s^+-C_s^-\right)\frac{C_1}{C_{f_1}}=0$$

$$NV_{\mathrm{ref}_1}\left(C_s^+-C_s^-\right)\frac{C_1}{C_{f_1}}=V_{\mathrm{ref}_2}\frac{C_2}{C_{f_2}}\left(nC_s^-+nC_s^+-NC_s^+\right)$$

$$\frac{C_s^+-C_s^-}{C_s^++C_s^-}=\frac{V_{\mathrm{ref}_2}}{V_{\mathrm{ref}_1}}\frac{C_2}{C_1}\frac{C_{f_1}}{C_{f_2}}\left(\frac{n}{N}-\frac{C_s^+}{C_s^++C_s^-}\right)$$

$$B_{\mathrm{ave}}=\frac{1}{2}+\left(\frac{V_{\mathrm{ref}_1}}{V_{\mathrm{ref}_2}}\frac{C_1}{C_2}\frac{C_{f_2}}{C_{f_1}}+\frac{1}{2}\right)\frac{C_s^+-C_s^-}{C_s^++C_s^-} \tag{4}$$

where $B_{\mathrm{ave}}=n/N$ and is the average value of the bitstream. The difference here compared with other charge-balanced ratiometric techniques is that the signal can be now widely adjusted by three ratios, allowing to maximize the input tone power for varying dynamic ranges and sensitivities.

D. Simulations

To demonstrate the effectiveness of the system in suppressing harmonics and achieving high linearity, a circuit-level thermal noise simulation of the second-order system is performed. The result is obtained by running a transient noise simulation. This simulation includes 1.5 pF of parasitic capacitance at each node of the accelerometer, representing the pad and bondwire capacitance. The op-amps used are optimized for noise and power [16]. The same accelerometer as that used for the Leuthold–Rudolf integrator is used with the same dynamic range of $\pm 16g$ corresponding to a differential capacitance $(C_s^+-C_s^-)$ of approximately 114 fF. The capacitor values used are $C_{f_1}=800$ fF, $C_{f_2}=800$ fF, $C_1=1000$ fF, $C_2=1000$ fF,

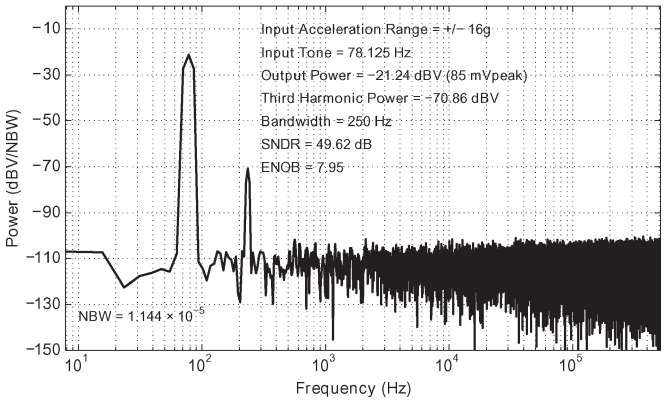

Fig. 6. Power spectral density at the output of the charge-to-voltage converter shown in Fig. 5 with the feedback DAC disabled. The number of points used for the FFT is 2^{17} and uses a Hanning window.

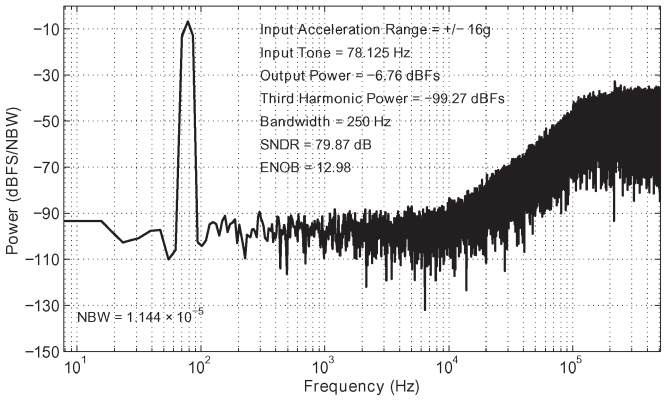

Fig. 7. Power spectral density of the output bitstream for the second-order system with thermal noise. The number of points used for the FFT is 2^{17} and uses a Hanning window.

TABLE II
PROPOSED SYSTEM POWER CONSUMPTION

Circuit Block	Current Consumption	Power
Front End (Converter and DAC)	261μA	313.2μW
First Integrator Stage	85μA	102.0μW
Second Integrator Stage	54μA	64.8μW
Auxiliary Circuits	190μA	228.0μW
Total Power	590μA	708.0μW

and $C_{f_3} = 700$ fF. The reference voltage for the converter stage is $V_{\text{ref}_1} = 600$ mV, and for the digital-to-analog conversion (DAC) feedback stage, it is $V_{\text{ref}_2} = 300$ mV. The sampling frequency is Fs $= 1024$ KHz, and the signal bandwidth is 250 Hz, resulting in an oversampling ratio (OSR) of 2048.

To begin with, we look at the output spectrum of the capacitance-to-voltage converter by itself (the feedback DAC is disabled), as shown in Fig. 6. The output at this stage is neither ratiometric nor charge balanced, and as a result, it has a large third-order harmonic. Fig. 7 then shows the spectrum of the output bitstream for the proposed system. The feedback system creates a charge-balanced and ratiometric output that eliminates the third-order harmonic to below the noise floor.

E. Power Consumption

Table II summarizes the simulated power consumption for the implemented system in the 0.13-μm CMOS technology. Auxiliary circuits include the comparator, the clock generation, and the biasing circuitry. The circuit operates with 708 μW (2.8 μW/Hz) of power from a 1.2-V power supply.

IV. NOISE ANALYSIS

It is convenient for this architecture to choose the output of the integrator as the point to refer all noise sources. Then, the total noise is given by the contribution of the capacitance-to-voltage converter, the DAC, and the first integrator, and it is reduced by the OSR. Accordingly, we can write

$$\overline{V^2}_{\text{total}} \approx \frac{\overline{V^2}_{\text{conv}} + \overline{V^2}_{\text{DAC}} + \overline{V^2}_{\text{int}}}{\text{OSR}}. \tag{5}$$

Any noise after the first integrator is heavily attenuated by the high gain of the first integrator and the noise-shaping property of the delta–sigma loop [17] and can be neglected. For the following derivations, it is assumed that the noise bandwidth is dominated by that of the op-amp, as would be the case for a power-efficient design [16].

For the converter, the total noise is given by

$$\overline{V^2}_{\text{conv}} \approx \left[\frac{kT}{C_{f_1}} + \frac{16kTn_f}{3g_{m_1}}\frac{\beta_1 g_{m_1}}{4C_{o_1}}\left(1+\frac{2C_s+C_{p_1}}{C_{f_1}}\right)^2\right]\left(\frac{C_1}{C_{f_3}}\right)^2$$

where k is Boltzmann's constant, T is temperature in kelvins, C_{o_1} is the effective load that limits the bandwidth of the op-amp, $\beta_1 = C_{f_1}/(C_{f_1} + C_{p_1} + 2C_s)$, with C_{p_1} being the parasitic capacitance at the inverting stage of the op-amp, g_{m_1} is the transconductance of the converter stage op-amp as determined by the settling time requirements, and $n_f \geq 1$ is a noise factor depending on the architecture of the op-amp used.

Similarly, for the DAC feedback stage, the total noise due to the DAC switches and op-amp is given by

$$\overline{V^2}_{\text{DAC}} \approx \left[\frac{kT}{C_{f_2}} + \frac{16kTn_f}{3g_{m_2}}\frac{\beta_2 g_{m_2}}{4C_{o_2}}\left(1+\frac{2C_s+C_{p_1}}{C_{f_2}}\right)^2\right]\left(\frac{C_2}{C_{f_3}}\right)^2$$

where $\beta_2 = C_{f_2}/(C_{f_2} + C_{p_1} + 2C_s)$, C_{o_2} is the effective op-amp load, and g_{m_2} is the transconductance of the DAC op-amp.

Finally, the integrator noise is given by

$$\overline{V^2}_{\text{int}} \approx \left(\frac{kT}{C_1} + \frac{kT}{C_2}\right)\left(\frac{C_1}{C_{f_3}}\right)^2 + \frac{16kTn_f}{3g_{m_3}}\frac{\beta_3 g_{m_3}}{4C_{o_3}}\frac{1-\beta_3^2}{\beta_3^2}$$

where $\beta_3 = C_{f_3}/(C_{f_3} + C_{p_2} + C_2 + C_1)$, C_{o_3} is the effective op-amp load, g_{m_3} is the transconductance of the integrator, and C_{p_2} is the parasitic capacitance at the inverting input of the integrator.

Using the capacitor values used in the simulation with $n_f = 3.5$, the noise values as a percentage of the total as contributed by the DAC, the converter, and the integrator are 40.7%, 47.5%, and 11.8%, respectively. The theoretical SNR can be approximated by taking the ratio of the signal power, as calculated from (4), over the total in-band noise power, as given by (5). Using the capacitor values used in Section III-D, the theoretical SNR is calculated to be 82.1 dB, which is slightly more optimistic than the simulations. The discrepancy can be accounted for by the neglected band-limited switch noise sources and the noise contribution from later stages not accounted for in (5).

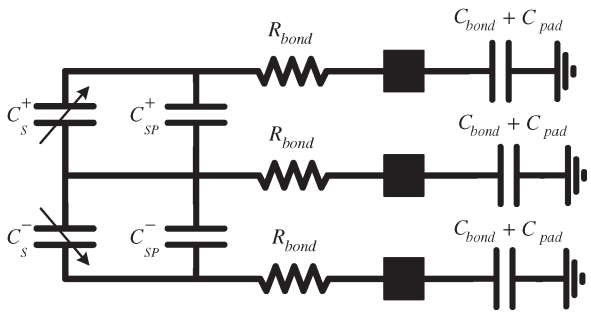

Fig. 8. Front-end circuitry with static and parasitic bondwire capacitances.

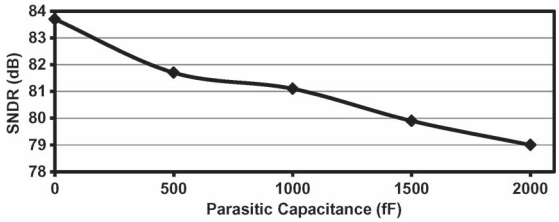

Fig. 9. SNDR versus the interconnect capacitance.

V. Parasitic Capacitances and Linearity Limitation

A. Parasitic Capacitances

Fig. 8 shows the front end of the readout circuit with parasitic capacitances and resistances. The resistance values for the bondwire range in a few ohms and do not adversely affect the settling time of the circuit. The static capacitance is assumed to be small, and digital offset calibration techniques can be also used to minimize its effects [18]. Fig. 9 shows the simulation of the proposed system with bondwire and bondpad parasitic capacitances ranging from 0 to 2000 fF. The parasitic capacitance does not harmonically limit the linearity and only marginally increases the noise, as expected from the noise analysis. The achievable SNDR at the expected single package parasitic capacitance of 1.5 pF is about 80 dB.

B. Linearity Limitation

The simulations in this brief have been performed with an accelerometer modeled by a perfectly linear spring. To achieve the 80-dB SNDR as simulated, the spring constant linearity also has to be at least 80 dB or higher. Ultimately, with a perfectly linear accelerometer and if the power and the area are not of concern, the linearity of the proposed system will be limited by the quantization noise of the circuit or the mechanical thermal noise of the accelerometer.

VI. Conclusion

A flexible charge-balanced readout technique for capacitive accelerometers has been proposed. The system is capable of achieving high linearity compared with conventional techniques at comparatively low power. The system is flexible in accommodating varying sensor sensitivities and dynamic ranges.

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