A 3rd-Order Integrated Passive Switched-Capacitor Filter Obtained with A Continuous-Time Design Approach

Sevil Zeynep Lüleç, David A. Johns, *Fellow, IEEE*, and Antonio Liscidini, *Senior Member, IEEE*

***Abstract*— A 3rd-order passive switched-capacitor low-pass filter is presented together with experimental results. The current input - voltage output filter structure realizes complex-conjugate poles although it is composed of switches and capacitors. The results are verified with measurements performed on the filter prototype integrated in a 0.13 µm CMOS technology. The prototype has a cut-off frequency of 470 kHz, 150 µW power consumption from 1.2 V power supply, 92 dB SFDR, and an active area of 0.06 mm^2. The switch-capacitor filter was obtained using a continuous-time model that is also described here and is useful for design, analysis, and simulation of oversampled switched-capacitor circuits. The model is applicable to a variety of topologies including multi-phase passive switched-capacitor filters, switched-capacitor integrators, as well as switched-capacitor DC/DC converters.**

***Index Terms*—Discrete-time systems, continuous-time design, continuous-time modeling, low-pass filter, passive switched capacitor circuits, switched capacitor circuits.**

I. Introduction

As integrated circuit technology advances towards shorter length transistors, analog designers need to reconsider conventional implementations. Advanced transistors require lower power supply voltages and make the design of high-gain high-bandwidth amplifiers more difficult. However, switch and capacitor based circuits work well in modern technologies due to lower parasitic components and fast clocking circuits. In terms of filter design, these trends favor passive switched-capacitor (PSC) architectures, where the charge transfer between capacitors do not require the presence of an active element [1, 2]. The elimination of the active element leads to high linearity and low noise filter designs with accurate corner frequencies that are set by capacitor ratios. In addition, PSC circuits are easily configurable either by using a capacitor bank or changing the sampling frequency.

In the recent literature, PSC topologies were used as an anti-aliasing integration sampler [3, 4], a channel-selection filter for receivers [5-11], a decimation filter before an ADC [12], and a charge-based DAC for transmitters [13]. The anti-aliasing integration sampler can only realize first-order filtering [3, 4]. However, this sampler shows that the continuous input current integration on the filter capacitor prior to sampling results in a first-order build-in anti-aliasing filtering, which is a property that is also inherited by subsequent higher-order filters [4]. Afterwards, higher-order filtering was achieved using a multi-phase PSC structure for channel-selection filters but had only real poles which resulted in poor filter selectivity [5]. Higher-order real-poled PSC filters were utilized to improve the filter selectivity partially [6]. By adding active feedback to the multi-phase PSC filter, complex conjugate poles were realized, but at the expense of degraded noise, linearity, and power performance [14]. A simplified continuous-time (CT) model enabled easy analysis and design of multi-phase PSC filters with grounded capacitors [9]. This modeling approach replaces switches and sampling capacitors with ideal voltage buffers and equivalent resistors leading to great simplifications in the analysis and design. As a result, a 3rd-order low-pass PSC filter with complex conjugate poles was implemented passively using only switches and capacitors [10]. This passive feedback implementation restores the sharper filtering with no additional noise, linearity, and power penalty due to active devices.

This paper extends the work in [9, 10] and presents a continuous-time model and design approach for oversampled switched-capacitor topologies by focusing on PSC structures. In contrast with [9], the model proposed here is applicable to the circuits regardless whether the capacitors are grounded or both plates are switching. The accuracy of the model is explored, and limitations are derived. The design methodology of a 3rd-order filter prototype is investigated in detail while showing measurement results that closely agree with the prediction. The paper is organized as follows: Section II describes the continuous-time modeling approach. Section III gives modeling examples for non-grounded capacitor circuits. Section IV covers the limitations of the continuous-time model. Section V describes the filter design using the continuous-time design approach and gives the implementation details, and Section VI provides measurements verifying the continuous-time model.

Manuscript was submitted for review on January 17, 2019.

The authors are with the Edward S. Rogers Sr. Department of Electrical & Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: sz.lulec@mail.utoronto.ca; david.johns@utoronto.ca; antonio.liscidini@utoronto.ca).

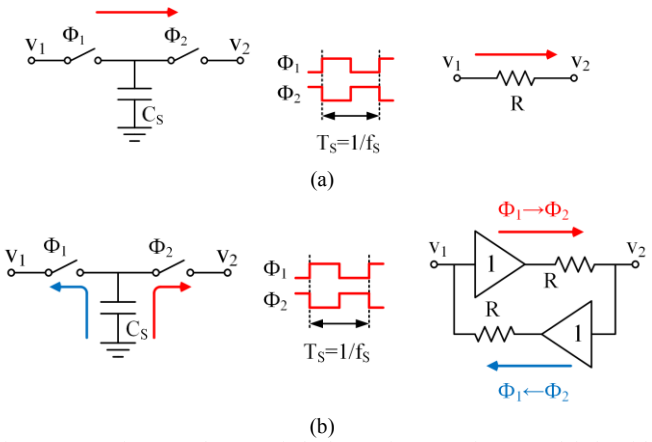

Fig. 1. Basic two-phase switched-capacitor topology modeled with a) traditional equivalent resistance, and b) two buffer + equivalent resistance branches.

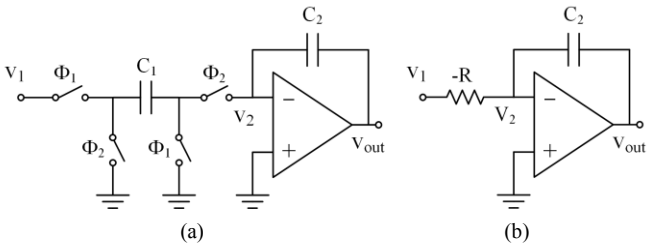

Fig. 2. a) Parasitic insensitive switched-capacitor integrator, b) its continuous-time model.

II. From Discrete to Continuous-Time Modelling

Switched-capacitor circuits have linear time-varying characteristics requiring charge balance equations and z-domain analysis for exact representation of their behavior in discrete-time [15, pp. 398]. However, under specific conditions, it is possible to analyze these structures with good accuracy using linear time-invariant components. For instance, it is well known that a capacitor, C_S, connected to two voltage sources V_1 and V_2 in two different clock phases, Φ_1 and Φ_2, respectively, can be modeled using an equivalent resistance, R, as shown in Fig. 1a (where R is equal to T_S/C_S with T_S corresponds to the clock period) [15, pp. 399, 16]. This equivalence is derived by assuming ideal DC voltage sources connected to V_1 and V_2 nodes and by calculating the average current transfer in one clock period. While this derivation is quite well known for DC signals, to the authors' knowledge, there is no equivalent derivation for low frequency ac signals. For completeness, Appendix A shows the same equivalent resistance T_S/C_S can be derived for ac voltage sources with the input signal frequency much lower than the sampling frequency, f_S.

Fig. 1b shows a continuous-time modeling approach, where the current supplied by each node is considered separately and modeled using an ideal voltage buffer + equivalent resistance branch [9]. The total number of buffer + R branches is equal to the number of clock phases during which C_S is connected to different voltage sources. Although this approach may seem redundant for a two-phase switched-capacitor topology, it can address multi-phase switched-capacitor structures, where a simple equivalent resistor approach does not work. Moreover, this model is capable of addressing non-reciprocal topologies by employing branches with ideal voltage buffers, which can create unilateral paths [9]. (For completeness, the derivation of buffer + equivalent resistor model for voltage sources with input frequencies much smaller than the sampling frequency is covered in Appendix B.)

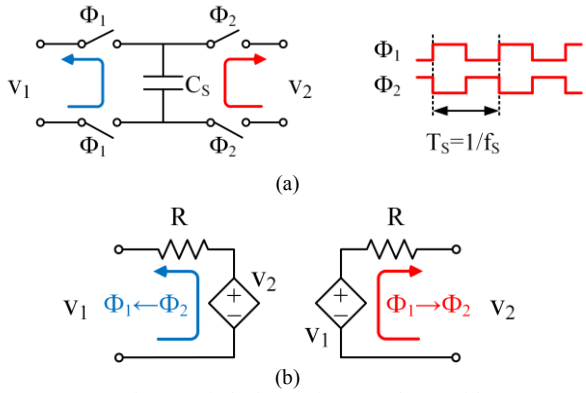

Fig. 3. a) Two-phase switched-capacitor topology with non-grounded sampling capacitor and b) proposed continuous-time model.

The modeling approach with buffers and equivalent resistors can address multi-phase switched-capacitor structures; however, it relies on a grounded sampling capacitor. There are a variety of switched-capacitor implementations that employ sampling capacitors with both plates switching in between different nodes. One common example is the parasitic insensitive switched-capacitor integrator shown in Fig. 2a. Conventionally, the switching parts are modeled using a –R as shown in Fig. 2b [15, pp, 417]. This approach can capture the correct positive voltage gain value. However, -R indicates that for positive V_1 values, the current is flowing into V_1 from the virtual ground, which is not the case. Moreover, if this continuous-time approach is used to analyze the effect of finite amplifier gain or offset voltage, the analysis may result in false or inaccurate values together with a fictitious right-half plane pole at $+1/[(1+A)RC]$ rad/s, where A is the finite amplifier gain defined by $v_{out}/(v_+-v_-)$. Apart from the parasitic insensitive switched-capacitor integrator, DC/DC converters with flying capacitors and even PSC filters can include sampling capacitors with non-grounded switching plates.

A. Floating Switched-Capacitor Continuous-Time Model

A two-phase switched-capacitor topology where both plates are non-grounded is shown in Fig. 3a. The average current flows into V_2 in one clock period can be written as: $(V_1-V_2)f_SC_S$. This current can be modeled using a voltage controlled voltage source (VCVS) whose value is equal to V_1, connected in series with an equivalent resistance of R, whose value is $1/f_SC_S$. Another branch of VCVS and R is necessary to model the average current flowing into V_1 node to complete the model as shown in Fig. 3b. Although it is not covered, this proposed model can be easily adapted to multi-phase switched-capacitor structures by merely increasing the number of VCVS + R branches. A similar model for switched-capacitor structures

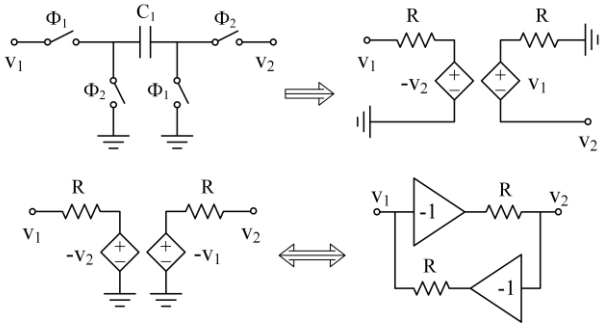

Fig. 4. A common non-grounded switched-capacitor structure modeling.

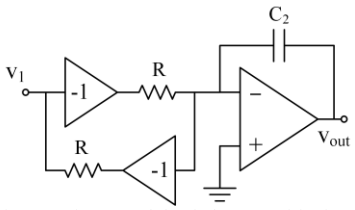

Fig. 5. The continuous-time model of the parasitic insensitive switched-capacitor integrator.

with two phases was also previously investigated [17]. (The derivation of the model for voltage sources with input frequencies much smaller than the sampling frequency is similar to the proofs given in Appendices A and B.)

III. Modelling Examples

In this section, two examples of switched-capacitor topologies that cannot be modelled in continuous-time with a traditional approach will be analyzed with the proposed model to highlight the effectiveness of the model.

A. *Parasitic Insensitive Switched-Capacitor Integrator*

The proposed continuous-time model can be used to analyze the parasitic-insensitive switched-capacitor integrator. Fig. 4 shows the switching parts of the integrator, where V_1 corresponds to the input voltage, and V_2 corresponds to the virtual ground of the amplifier shown in Fig. 2a. In Φ_1, C_1 is connected in between V_1 and ground nodes, this sampled voltage value, (V_1-0), becomes the value of the VCVS in the second branch. Whereas during Φ_2, C_1 is connected in between ground and V_2 nodes, thus the VCVS value in the first branch becomes $-V_2$. Since there exist two ground nodes, it is possible to rearrange this continuous-time model as shown in Fig. 4 bottom side, where VCVSs can be shown by ideal inverting voltage buffers to have a more intuitive schematic. Fig. 5 shows the parasitic insensitive integrator where the switching parts are replaced.

It should be noted that this continuous-time integrator model can capture the correct sign of the voltage transfer function by the use of inverting voltage buffers rather than having –R. Furthermore, this model captures the correct input current direction. This new model can also be used to analyze the effects of finite amplifier gain and offset voltages without resulting in a fictitious right half plane pole.

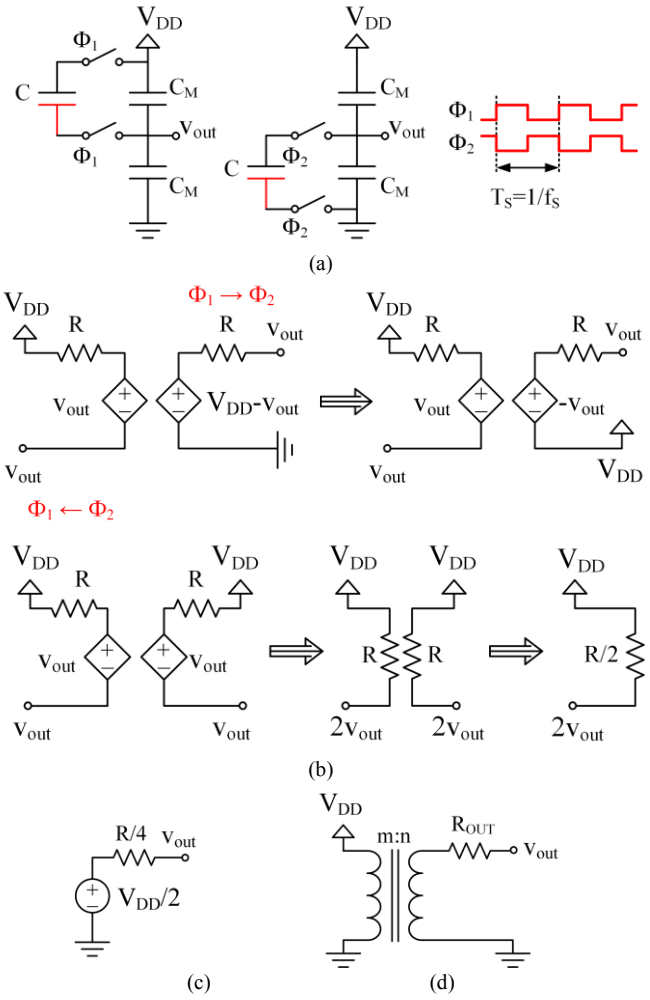

Fig. 6. a) Switched-capacitor DC/DC voltage converter, b) its simplified continuous-time model, c) Thévenin equivalent of v_{out} obtained with the continuous-time model, d) conventionally used switched-capacitor converter transformer model.

B. *Flying Capacitor DC-DC Converter*

The switched-capacitor DC/DC converter structure shown in Fig. 6a can be analyzed using the differential continuous-time model to determine the Thévenin equivalent of the switching parts. This structure involves a flying capacitor, C, and large capacitors, C_M's , for storing the DC value of the output voltage. The frequency of interest is much smaller than the sampling frequency [18]. During Φ_1, C is connected in between V_{DD} and V_{out} nodes, sampling a voltage of V_{DD}-V_{out}. Whereas, during Φ_2, C is connected in between V_{out} and the ground node sampling a voltage of V_{DD}-0 across itself. The top left schematic in Fig. 6b shows analyses of this circuit using the differential switched-capacitor continuous-time model, where $R=1/f_SC$. It is possible to simplify further the model as shown in Fig. 6b and obtain the Thévenin equivalent circuit shown in Fig. 6c. In order to find v_{out} from $2v_{out}$, the open circuit voltage, V_{DD}, and the output resistance, R/2, are divided by two. The conventional approach is to use a DC transformer model as shown in Fig. 6d [18]. The conversion ratio, (m:n), and the output resistance, R_{OUT}, can be calculated to be exactly the same as Fig. 6c. However, this approach is not intuitive and the derivation is cumbersome.

IV. Limitations of the Model

The branch-based continuous-time model inherits the assumptions of the traditional two-phase switched-capacitor resistor equivalence: The driving node voltage should dictate the voltage sampled by the sampling capacitor, C_S. However, limited settling time and charge sharing paths may disturb this behavior. Moreover, as previously discussed, the continuous-time model is only valid for input voltage sources with frequencies much smaller than the sampling frequency. In this section, these limitations will be studied to determine the accuracy of the model when the assumptions are not met perfectly.

A. Settling Time

A resistance in series with the sampling capacitor creates a non-zero time constant, which leads to settling error. This series resistance can be due to the switch on resistance or the source resistance. For a conventional switched-capacitor topology shown in Fig. 1, when switches have on resistances of R_{SW}, the equivalent resistance seen can be rewritten as follows:

$$R = \frac{1}{f_S C_S} \cdot \frac{1+e^{-1/(2 f_S R_{SW} C_S)}}{1-e^{-1/(2 f_S R_{SW} C_S)}} \quad (1)$$

where f_S is the sampling frequency. As R_{SW} goes to zero, R becomes $1/f_S C_S$, as expected. For example, if the settling time constant ($R_{SW}C_S$) is set to 15% of the sampling period, $1/f_S$, the error in the equivalent resistance becomes 7.40 %, while if the time constant is set to 5% of the sampling period, the accuracy becomes 0.01%.

One way to relax this problem without requiring a higher clock frequency is to increase the sampling frequency of the switched-capacitor by introducing time-interleaved stages [19], as done in the presented prototype described in Section V.

B. Charge Sharing

In the case C_S is connected to a capacitive driving impedance, there is an issue of charge sharing between two capacitors that leads to an error in the equivalent resistor behavior. For example, Fig. 7a shows a 1st-order PSC filter with current input and voltage output, where C_S is switching between an integrating capacitor, C_I, and a ground node. C_I capacitor can be treated as a voltage source for C_I values much larger than C_S, and thus the switching parts can be replaced by an equivalent resistor with a value of $1/f_S C_S$ (Fig. 7b). However, when C_S becomes comparable to the driving impedance, C_I, the charge stored in C_S is not an accurate representation of the initial voltage on C_I. Moreover, the pole created (proportional to C_S/C_I) moves toward the higher frequencies, where the model accuracy is limited.

It is possible to investigate the continuous-time model accuracy for this 1st -order PSC filter. Fig. 8 shows the frequency transfer functions simulated using periodic steady state and periodic AC analysis for a sampling frequency of 160 MHz, C_S=200fF, and with a large (40) and a small (4) C_I/C_S ratio. For C_I/C_S=40, the error in the 3dB cut-off frequency is 1%, whereas for C_I/C_S=4, the error becomes 12%. Fig. 9 shows the percentage error in the simulated 3 dB cut-off frequency for changing f_{3dB}/f_S ratios. The error increases, as f_{3dB} becomes closer to f_S.

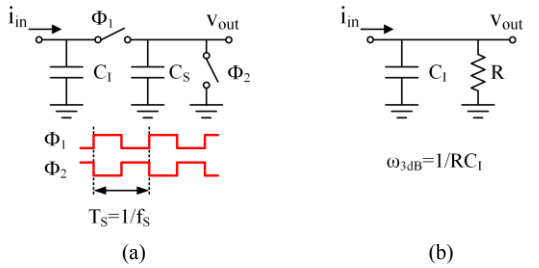

Fig. 7. a) 1st-order PSC filter and b) its continuous-time model with the traditional equivalent resistance approach.

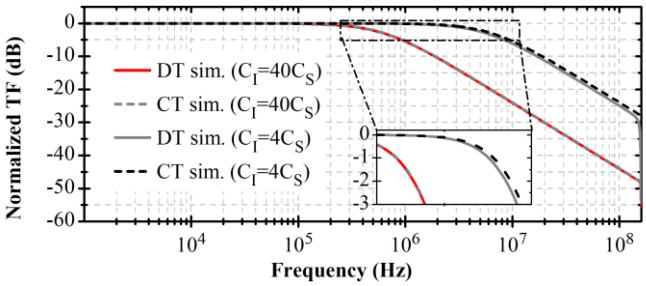

Fig. 8. 1st-order PSC filter simulated discrete-time implementation and continuous-time model frequency responses for C_I/C_S=40 and C_I/C_S=4.

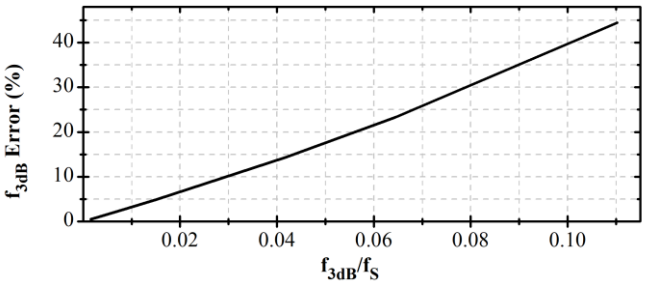

Fig. 9. Error in the 3dB cut-off frequency calculation of a 1st-order PSC filter using the continuous-time model.

C. Accuracy of the Model in PSC Filters Response

The continuous-time model is valid for bandlimited sources with frequencies much smaller than the sampling frequency. However, it is shown that PSC filter frequency responses obtained using the continuous-time model closely follows the discrete-time analysis up to Nyquist frequency, $f_S/2$, as long as the pole frequencies are much smaller than the sampling frequency [9, 10]. This is because when the model accuracy starts to decrease at higher frequencies, the dominant impedance is determined by the large integrating capacitors present in the system. As an example, it is possible to analyze the 1st-order low-pass PSC filter shown Fig. 7. As $C_I \gg C_S$ and $f_{3dB} \ll f_S$, the model can predict the pass-band gain and the pole frequency with high accuracy. For the input frequencies closer to $f_S/2$, i.e., for frequencies higher than the pole frequency, C_I impedance starts to be the dominant impedance determining the overall frequency response. Thus, although at those frequencies the continuous-time model of the switching parts is not accurate, the continuous-time model of the filter results in the correct transfer function.

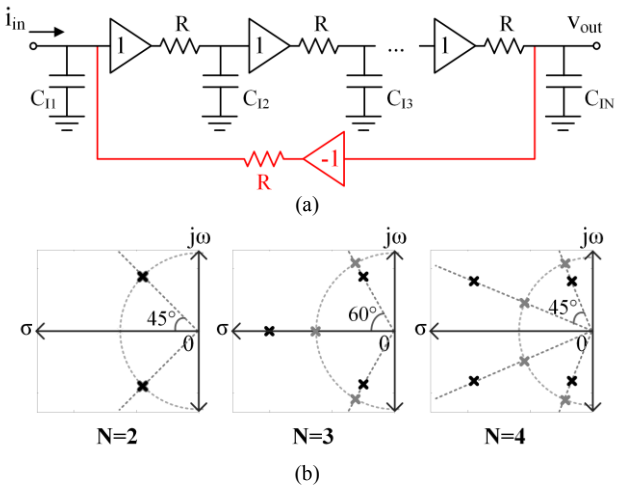

Fig. 10. a) Low-pass PSC filter with complex conjugate poles, and b) the pole locations of the 2nd, 3rd, and 4th order filters, where the gray markers shows the same order Butterworth pole locations having the same 1 dB cut-off frequency.

V. Design and Implementation

The strength of the continuous-time approach is that it offers a new point of view to develop novel topologies. In this section, starting from a cascade of real poles, complex conjugate poles are realized using the continuous-time approach. The continuous-time design approach highlights that switched-capacitors do not only act as resistance but with the help of time-variance, it is possible to create unilateral loops. This observation is important because the unilaterality makes it possible to realize complex conjugate poles. A 3rd-order low-pass PSC filter with complex conjugate poles was designed and fabricated to validate the continuous-time design approach. Design trade-offs and implementation details will be discussed through the section.

A. Design of the PSC Filter

It is known that complex conjugate poles can be generated by closing feedback around a cascade of stages with real poles. In Fig. 10a, the feedback is realized by connecting the output of the cascade to the input through an inverting buffer and an equivalent resistance, R. This structure is also the Nth-order realization of the 2nd-order Butterworth biquad filter reported previously, which has a limited quality factor (Q) of 1/√2 [9]. Thanks to the continuous-time approach, it is easy to analyze how the number of branches will affect the pole locations and change the associated quality factors. To determine the pole locations, the transfer function of the filter shown in Fig. 10a can be written as follows:

$$\frac{v_{out}}{i_{in}}(s)=\frac{R}{(1+sRC_{I1})(1+sRC_{I2})(1+sRC_{I3})\ldots(1+sRC_{IN})+1} \quad (2)$$

Fig. 10b shows the locations of the poles generated by a cascade of 2, 3, and 4 elements with the same valued C_I's for each stage. For a loop gain equal to one, which is the maximum achievable with a PSC network, the maximum quality factor is obtained starting from a cascade of coincident real poles, which demands identical C_I's. The generated poles have the same quality factors as the poles of a Butterworth filter but different frequencies (Fig.10b). The shift in the pole frequencies results in in-band peaking in the filter transfer function that increases with the order of the filter.

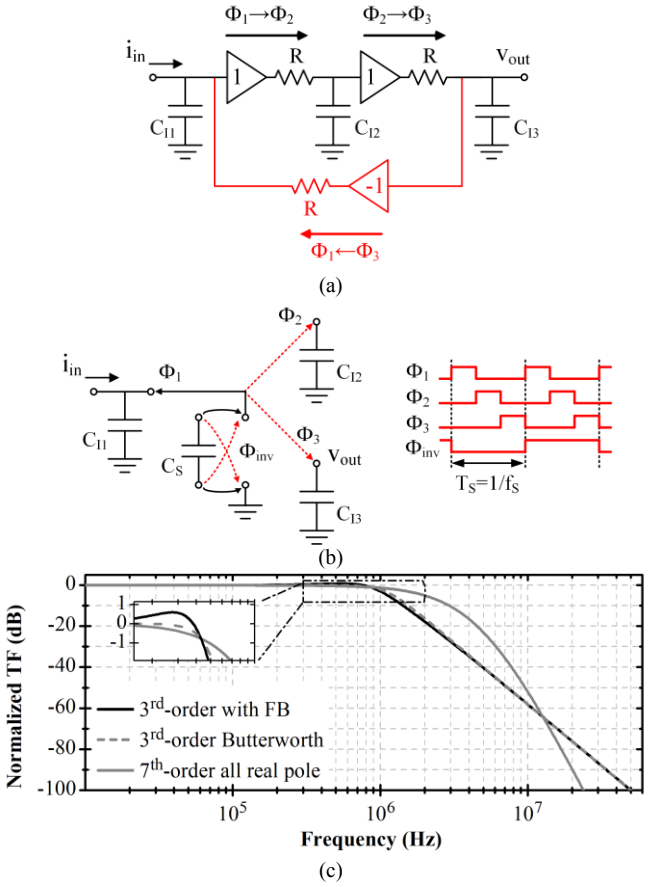

Fig. 11. a) The continuous-time model of the 3rd-order filter with complex-conjugate poles, b) an example PSC implementation, and b) its transfer function compared with the same order Butterworth and the 7th-order real pole filter having the same 1 dB droop frequency.

A 3rd-order filter is chosen to be designed as it can approximate the Butterworth filter behavior with less than 1dB in-band peaking. Fig. 11a shows the 3rd-order filter continuous-time model. And, an example of a 3rd-order implementation is shown in Fig. 11b. In this filter, C_S shares charge with C_{I1}, C_{I2}, and C_{I3} in Φ_1, Φ_2, and Φ_3, respectively, creating a unilateral signal flow. During the phase change from Φ_3 to Φ_1, C_S is flipped to create the negative feedback. Note that Fig. 11a also shows the related phase changes corresponding to each branch.

The pole locations derived from the model can be verified by evaluating the z-domain transfer function of the filter shown in Fig. 11a as follows (assuming equal C_I's for simplicity):

$$\frac{V_{out}(z)}{Q_{in}(z)}=\frac{1}{C_S}\frac{z^3(1-\alpha)^3}{(z-\alpha)^3+z^2(1-\alpha)^3} \quad (3)$$

where α is $C_I/(C_I+C_S)$ and Q_{in} is the amount of charge fed into the filter in one sampling period, T_S. Although the network shown in Fig. 11a is periodic with $2T_S$, T_S is defined for three phases because the output is sampled in every three phases. The quality factor of the created poles can be found by mapping z-domain poles to s-domain using the bilinear approximation. As C_I/C_S ratio increases, Q of the complex conjugate pair approaches 1, which is the Q value predicted by the continuous-time model used for the synthesis of the filter.

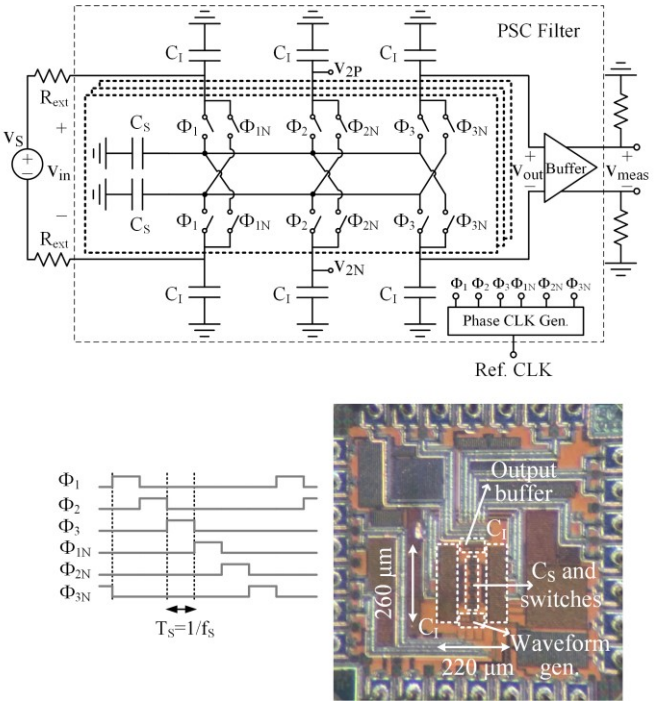

Fig. 12. Fabricated 3rd-order low-pass PSC low-pass filter schematic, timing diagram, and chip photo.

Simulation of the proposed filter and the 3rd-order Butterworth response (with the same DC gain and 1 dB droop frequency) are compared in Fig. 11b. Although the pole location deviates from the ones of a Butterworth, the 3rd-order filter maintains similar in-band flatness and selectivity. The figure inset shows that the response of the proposed filter deviates from a Butterworth one less than 1dB close to the filter band edge. Fig. 11b also compares the proposed solution with the 7th-order all real pole reported by Tohidian et al. in [5] by assuming a maximum in-band drooping of 1 dB. Although the proposed filter has a lower order, a higher selectivity is achieved over a decade close to the filter pass-band due to the presence of the complex conjugate poles.

B. Implementation of the PSC Filter

A fully differential 3rd-order PSC filter was designed and fabricated in 0.13 µm TSMC CMOS process. Fig. 12 shows the PSC filter implementation. The charge inversion of C_S is realized by exploiting the differential structure and cross-coupling of positive and negative nodes. The filter uses six phases: Three non-inverting phases (Φ_1, Φ_2, and Φ_3) when top C_S is connected to the top C_I's sequentially, while the bottom C_S is connected to the C_I's on the bottom differential side. During the following three inverting phases (Φ_{1N}, Φ_{2N}, and Φ_{3N}) the C_S's are connected to the C_I's, on the opposite sides.

In order to increase the sampling rate, three time-interleaved blocks, which consists of C_S's and switches, are employed. Thus, the resulting sampling period becomes equal to the period of a single phase (Fig. 12).

The z-domain transfer function of the time-interleaved filter can be written as:

$$\frac{V_{out}(z)}{Q_{in}(z)} = \frac{2}{C_S}\frac{z(1-\alpha)^3}{(z-\alpha)^3+(1-\alpha)^3} \tag{4}$$

where α is $C_I/(C_I+C_S)$, coefficient 2 is due to the differential structure, and Q_{in} is the amount of charge fed into the filter in one sampling period. The z-domain transfer function reported in (4) seems considerably different than the previously derived transfer function in (3). The reason is that the sampling period, T_S, in (4) is defined for a single phase due to the time-interleaved structure, whereas in (3), T_S is defined for three phases. However, once mapped back to s-domain it can be seen that (3) and (4) result in similar filtering characteristics for the same T_S. The quality factor of the complex conjugate pole pair can be calculated as 1.08 by mapping z-domain poles to s-domain using Bilinear approximation (assuming C_I/C_S=10 and all C_I's are equal to each other).

For a sampling frequency of 160 MHz, the filter 3 dB bandwidth was designed to be 470 kHz. C_I's are chosen to be equal for maximum Q. All capacitors, C_I's and C_S's, are used as MIM capacitors with values 12.6 pF and 225 fF, respectively, together with the added parasitic capacitances. Each sampling capacitor, C_S, is directly connected to six switches (Fig. 12), and 20 % of the C_S's are made of switch parasitic capacitances that are added on top of MIM capacitances. Although each integrating capacitor, C_I, is also directly connected to six switches, the effect of switch parasitic capacitances on C_I's is negligible due to larger capacitance sizes. Smaller switches can help lower switch parasitic capacitances; however, there is a minimum limit on switch sizes due to the settling. The switches in this prototype are implemented using transmission gates and sized for 1.5 kΩ maximum on resistances for the operation range. A ring counter is implemented to produce six non-overlapping clock phases using an external clock signal at 160 MHz. A g_m-cell was not included in the design in order not to dominate the noise and linearity responses of the PSC filter. Thus, the noise model can also be verified. In the prototype, the PSC filter is followed by an on-chip open drain output buffer to drive the probe used for the measurements. In order not to affect the noise measurements, the output buffer was designed to have lower noise spectral density compared to the filter.

C. Component Mismatch Effect on the Quality Factor

Component mismatch in between C_I's or C_S's can affect the filter transfer function by changing the filter cut-off frequency and the quality factor of the poles. It is possible to analyze these effects using the continuous-time model. As an example, a single-ended 2nd-order passive switched-capacitor filter can be investigated using the denominator of the filter transfer function given in (2) for N=2 as follows:

$$D(s) = \left(1+sRC_{I1}\right)\left(1+sRC_{I2}\right)+1 \tag{5}$$

By rearranging the terms in (5) and equating it to the well-known 2nd-order biquad filter formula ($s^2 + s\omega_0/Q + \omega_0^2$), it is possible to find the corresponding 3 dB cut-off frequency, ω_0, and quality factor, Q, of the poles as follows [9]:

$$\omega_0 = \frac{\sqrt{2}}{R\sqrt{C_{I1}C_{I2}}} \quad \text{and} \quad Q = \frac{\sqrt{2C_{I1}C_{I2}}}{C_{I1}+C_{I2}} \tag{6}$$

From (6) it can be calculated that for example for a 10% mismatch in between C_{I1} (+5%) and C_{I2} (-5%), Q decreases by 0.13 %, which corresponds to a change from 0.707 to 0.706, i.e., the phase of the complex-conjugate poles changes from 45°

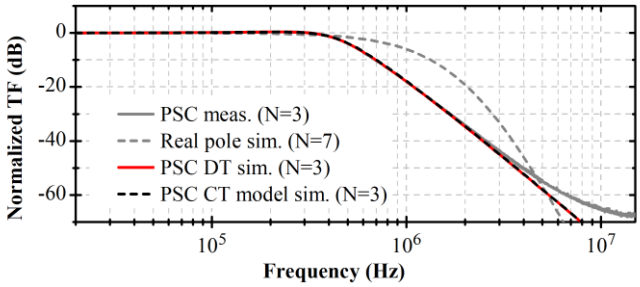

Fig. 13. Transfer functions of the simulated and measured 3rd-order low-pass PSC filter and the simulated 7th-order all real pole filter.

to 44.93º. C_S mismatch in between the time-interleave stages affects the R value. Thus, it does not affect the quality factor (see (6)).

VI. Measurement Results

For measurements, a voltage source is fed into the filter through large external resistors (R_{ext}) in series, similar to what has been done in [20]. The voltage source together with R_{ext} models the Thévenin equivalent of a g_m-cell with a finite output resistance (Fig. 12). The total external resistance is 200kΩ (where the filter input resistance is 27.8kΩ, $R_{eqv}=1/f_SC_S$). The filter consumes 125µA from a 1.2V power supply, which is the power consumed by the phase clock generator. The active area of the chip is 0.06 mm^2 dominated by the integrating capacitors (Fig. 12).

Fig. 13 shows the normalized transfer functions of the prototype measurements, post-layout schematic simulations, and the continuous-time model simulation. A good agreement has been obtained between measurements, simulation, and theory. For comparison, 7th-order all real pole PSC filter simulation response is also added to the figure. The 7th order filter reported in [5] was designed to have the same DC gain and 1 dB droop frequency. It can be observed that the 7th-order filter transfer function has a much smoother roll-off around the cut-off frequency compared to other filter transfer functions, which causes more than 10 dB attenuation loss around the band-edge. Towards 10 MHz, the measured filter response shows a flattening caused only by leakage on the PCB used for testing. External resistors lead to around 18 dB attenuation on the PCB, which worsen the filtering profile by elevating the leakage level. Fig. 14a shows the normalized measured transfer function of the filter for changing sampling frequency, f_S. It can be seen that the filter passband gain decreases for increasing f_S values, because the equivalent switched-capacitor resistance, R ($=1/f_SC_S$), decreases, which is proportional to the low-frequency gain of the filter as derived in (2). Whereas, the filter cut-off frequency, which is proportional to the $1/RC_I$ ($=f_SC_S/C_I$), increases for increasing f_S values. Fig. 14b shows the first (v_{in}), the second (v_{2P}-v_{2N}), and the third (v_{out}) order filtering nodes normalized measured transfer functions together with the continuous-time model simulation results, which match with very good agreement.

Output noise spectral density measurement results are shown in Fig. 15a with a resolution bandwidth of 1 Hz. The noise is measured at the output of the buffer and later referred to the output of the filter, v_{out}. At low frequencies, noise is equal to the noise of the R_{eqv} (i.e., $4kT/f_SC_S$). The solid black line shows the

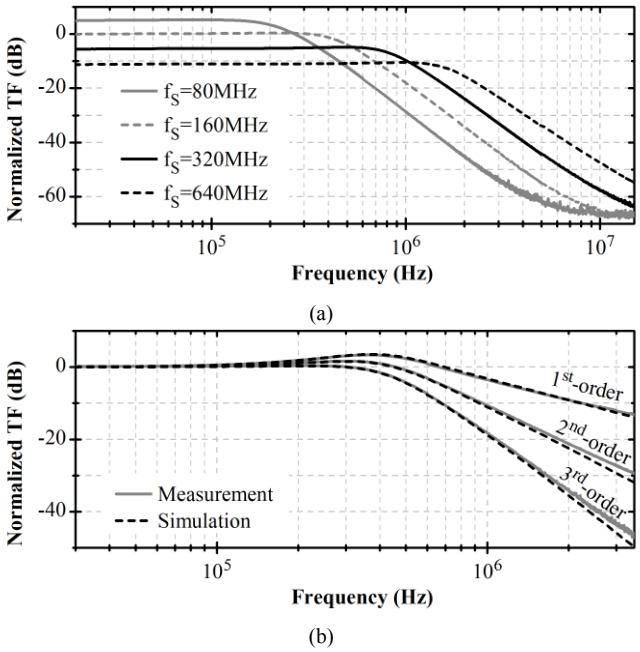

Fig. 14. Measured low-pass PSC filter a) output response for changing sampling frequencies, f_S, and b) 1st, 2nd, and 3rd -order output nodes for f_S=160MHz.

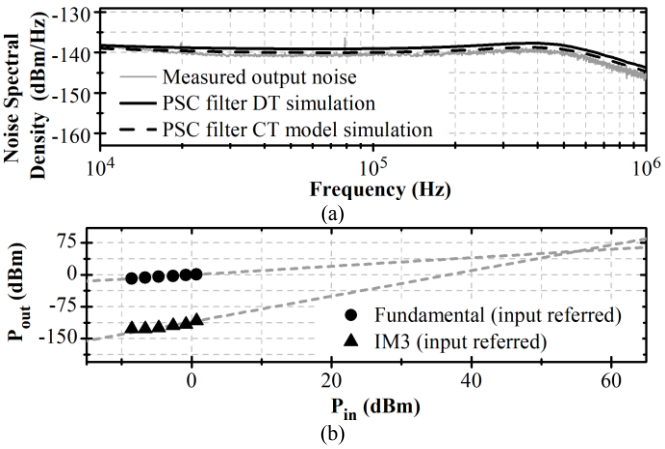

Fig. 15. a) Measured output noise spectral density over the filter bandwidth, b) Out-of-band IIP3 measurements of the PSC filter with two tones.

simulation result of the PSC filter and the dashed line shows the continuous-time model simulation result. The noise spectral density is reported up to 1 MHz due to the comparable noise floor of the spectrum analyzer. However, this measurement can show the in-band noise spectral density as well as the out-of-band decay close to the filter band edge. It can be seen that measured noise spectral density closely follows the simulations and theory. The measured input referred noise is 15.8µV, integrated between 10 kHz and 470 kHz. Out-of-band IIP3 is extrapolated using two blockers at 3.4 MHz and 6.7 MHz creating an intermodulation product at 100 kHz. Fig. 15b shows the input signal power and the third-order intermodulation distortion measurement results referred to the chip input (V_{in} in Fig. 12). The out-of-band IIP3 extrapolated is 55.1 dBm leading to 92 dB SFDR.

Table I summarizes the measurement results and compares them with the 7th-order PSC filter [5] and also with the recently published 4th order PSC filter that uses active feedback structure

TABLE I.
SUMMARY RESULTS AND COMPARISON TABLE

	This Work	[5]	[14]
Technology (nm)	130	65	180
Order	3rd	7th	4th
Poles	1 real + 2 complex conj.	7 all real	4 complex conj.
Power (mW)	0.15	1.98	4.3
Wave. gen. (mW)	*0.15*	*1.68*	*2.4*
G_m-cells (mW)	-	*0.3*	*1.9*
Voltage supply (V)	1.2	1.2	1.8
3dB cut-off (MHz)	0.47	0.4-30	0.49-13.3
Sampling Rate (MS/s)	160	800	65-300
OB IIP3 (dBm)	55.1	11.7	15.03
Int. Noise (μV)	15.8*	13.7**	13.6***
IRN (nV/√Hz)	23.3	4.57	6.54***
SFDR (dB)	92’	64	68
Active area (mm²)	0.06	0.42	2.9

Integrated over *10 kHz – 470 kHz, ** 50 kHz – 9 MHz bandwidth.
*** Averaged from 100 kHz to 4.4 MHz
’ $SFDR = 2/3 \cdot (IIP3 - Int.Noise)$

[14]. The SFDR obtained with this work is more than 20 dB better with a much lower power consumption partially thanks to the presence of complex conjugate poles which allowed to reduce the filter order without compromising the filter selectivity close to the cut-off frequency. However, it should be noted that both other works employ a transconductance at the input, and [14] also uses another transconductance as active feedback, which degrade filter’s linearity and increases power consumption. Although the transconductance on the feedback path is not needed in this work thanks to the passive feedback topology, the input g_m-cell is only avoided due to testing purposes. Thus, Table I should be reviewed considering these differences.

VII. CONCLUSION

A continuous-time model for oversampled switched-capacitor circuits with non-grounded sampling capacitors was introduced with examples. The limitations of the modelling approach were discussed. A 3rd-order passive switched capacitor filter prototype with complex-conjugate poles was obtained using the continuous-time approach. Measurements performed on the filter prototype result in state-of-art performance meanwhile verifying the continuous-time modeling and design approach. With this prototype, for the first time, switched-capacitor complex conjugate poles have been integrated on silicon without the need of any active circuitry. This represents a remarkable result that makes it possible to obtain sharp filtering profiles using PSC filters while showing that the design approach can lead to the invention of novel structures.

APPENDIX A: DERIVING EQUIVALENT SWITCHED-CAPACITOR RESISTANCE

Assume that V_1 and V_2 nodes in Fig. 1a are connected to two voltage sources with maximum frequencies well below the sampling frequency, f_S, and switches are ideal with zero on resistances. Then, the current supplied by V_1 can be written as follows:

$$i_1(t) = i_{1pulse}(t) + i_{1cap}(t) \tag{7}$$

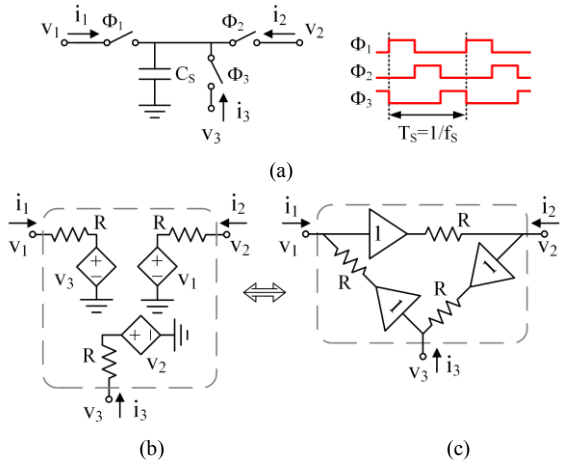

Fig. 16. a) A three-phase switched-capacitor topology, and b,c) its continuous-time model.

where $i_{1pulse}(t)$ is the current pulse occurs at the instant the switch is closed at Φ_1, and $i_{1cap}(t)$ is the current supplied to the capacitor during Φ_1, as the V_1 voltage slowly varies. These two components can be written as below:

$$i_{1pulse}(t) = C\left[v_1(t) - v_2(t)\right] \sum_{n=-\infty}^{+\infty} \delta(t - nT_S)$$

$$i_{1cap}(t) = C\frac{dv_1(t)}{dt} \sum_{n=-\infty}^{+\infty} a_n e^{jn\omega_S t}$$

$$with \quad a_n = \begin{cases} \frac{2}{n\pi}(-1)^{\frac{n-1}{2}}, & n \ is \ odd \\ 0, & n \ is \ even \ and \ n \neq 0 \\ 0.5, & n = 0 \end{cases} \tag{8}$$

where $i_{1pulse}(t)$ is a series of current pulses whose area is equal to $C.\Delta V$ ($=Cv_1(nT_S)-Cv_2(nT_S)$), and $i_{1cap}(t)$ is the capacitor current equation multiplied by the rectangular pulse train, which is represented by its Fourier series. Note that rectangular pulse train has the same phase of Φ_1 with an amplitude of 1.

In order to define an impedance to model the topology as a linear time-invariant (LTI) system, the resulting current in response to the V_1 and V_2 voltages should be examined. From (7) and (8), it is possible to write the Fourier transform of the produced current as:

$$I_1(\omega) = \frac{C}{T_S}\sum_{k=-\infty}^{+\infty}\left[V_1(j\omega - jk2\pi f_S) - V_2(j\omega - jk2\pi f_S)\right] + j\omega C\sum_{k=-\infty}^{+\infty} a_k V_1(j\omega - jk2\pi f_S) \tag{9}$$

where a_k are the Fourier series coefficients and equal to a_n for n=k. It can be observed from (9) that the current produced has a fundamental harmonic and also higher harmonics at the multiples of f_S. To model the circuit behavior for low frequencies, only the fundamental harmonic would be of interest [21], which can be written as below:

$$I_{1Fund}(\omega) = f_S C\left[V_1(j\omega) - V_2(j\omega)\right] + j\omega\frac{C}{2}V_1(j\omega) \tag{10}$$

It can be seen that I_{1Fund} results in a $1/f_S C$ resistance in between V_1 and V_2 nodes and a C/2 valued capacitance in between the V_1 node and ground. Although C/2 is needed for the exact representation at the fundamental frequency, for

simplicity, it is ignored in this paper, as all the cases that are covered, sampling capacitors are connected to low impedance nodes, where the effect of C/2 becomes negligible. Moreover, it should be noted that $2/j\omega C$ impedance is much greater than $1/f_S C$ for the frequencies of interest ($\pi f << f_S$).

The impedance seen from the V_2 node can be derived similarly by writing the current equation sunk into the V_2, $i_2(t)$. In this case, the Fourier Transforms of the current produced can be written as follows:

$$I_{2pulse}(\omega) = e^{\frac{-j\omega}{2f_S}} \frac{C}{T_S} \sum_{k=-\infty}^{+\infty} \left[V_2(j\omega - jk2\pi f_S) - V_1(j\omega - jk2\pi f_S) \right]$$

$$I_{2cap}(\omega) = j\omega C \sum_{k=-\infty}^{+\infty} b_k V_2(j\omega - jk2\pi f_S)$$

$$with \quad b_k = \begin{cases} \frac{2}{n\pi}(-1)^{\frac{n+1}{2}}, & n \ is \ odd \\ 0, & n \ is \ even \ and \ n \neq 0 \\ 0.5, & n = 0 \end{cases} \tag{11}$$

whose fundamental component becomes:

$$I_{2Fund}(\omega) = e^{\frac{-j\omega}{2f_S}} f_S C \left[V_2(j\omega) - V_1(j\omega) \right] + j\omega \frac{C}{2} V_2(j\omega) \tag{12}$$

The exponential term in I_{2Fund} expression is due to the sampling phase shift, and it can be ignored for the frequencies of interest ($\pi f << f_S$). Once the exponential term is ignored, it is seen that the first part of I_{2Fund} results in the same $1/f_S C$ resistance in between V_1 and V_2 nodes, whereas the second part of I_{2Fund} results in a C/2 valued capacitance in between V_2 node to ground. This capacitance can be ignored as well because the impedance of $2/j\omega C$ is much greater than $1/f_S C$ for the frequencies of interest ($\pi f << f_S$). Thus, the voltage and current relationship in between V_1 and V_2 voltage sources can be modeled by an equivalent resistance of $1/f_S C$ in between those two nodes.

APPENDIX B: DERIVING MULTI-PHASE EQUIVALENT MODEL

Assume that V_1, V_2, and V_3 in Fig. 16a are all connected to ideal voltage sources with input frequencies much smaller than the sampling frequency, f_S, and switches are ideal with zero on resistances. Then, the current supplied by V_1 can be written as follows:

$$i_1(t) = i_{1pulse}(t) + i_{1cap}(t)$$

$$i_{1pulse}(t) = C\left[v_1(t) - v_3(t) \right] \sum_{n=-\infty}^{+\infty} \delta(t - nT_S)$$

$$i_{1cap}(t) = C \frac{dv_1(t)}{dt} \sum_{n=-\infty}^{+\infty} c_n e^{jn\omega_S t}$$

$$with \quad c_n = \begin{cases} -\frac{2}{n\pi}\sin\left(\frac{n\pi}{3}\right), & n \in Z \\ \frac{1}{3}, & n = 0 \end{cases} \tag{13}$$

It can be shown that these current equations lead to a resistance in between V_1 and V_3 nodes with a value of $1/f_S C$ for the frequencies of interest. Moreover, (13) also leads to a C/3 valued capacitance in between the V_1 node and ground (the derivation and assumptions are similar to the ones discussed in Appendix A).

In order to complete the model and to replace the switching parts, all current components (i_1, i_2, and i_3) should be considered. It can be shown that, for the frequencies of interest, there is a general current equation valid for i_1, i_2, and i_3 that can be written as follows in the Fourier domain:

$$I_k(\omega) = f_S C\left[V_k(j\omega) - V_{Prev}(j\omega) \right] \tag{14}$$

where I_k represents the Fourier transform of the current component sourced by V_k voltage source (where k=1,2, and 3), and V_{Prev} represents the voltage source that C is connected to in the prior phase before connecting to V_k. It is important to note that although there exit three voltage sources, the current component related to each node only depends on two voltage sources that C is connected (one at the relevant phase and the other one is at the phase prior to the relevant phase).

Fig. 16b shows the schematic representation of (14) employing ideal voltage control voltage sources (VCVS) in series with the $1/f_S C$ valued equivalent resistances. This schematic can be modified to have a more intuitive view as shown in Fig. 16c, where VCVS's are replaced with ideal voltage buffers.

REFERENCES

[1] A. Winoto and B. Nikolic, "Discrete-time processing of RF signals," in *Multi-Mode/Multi-Band RF Transceivers for Wireless Communication*, G. Hueber and R. B. Staszewski, eds., New York, NY, USA: Wiley, 2011, ch. 8, sec. 1, pp. 219-245.

[2] F. –J. Wang, G. C. Temes, and S. Law, "A quasi-passive CMOS pipelined D/A converter," in *IEEE J. Solid-State Circuits,* vol. 24, no. 6, pp. 1752-1755, Dec. 1989. DOI: 10.1109/4.45017.

[3] R. Bagheri et al., "An 800-MHz–6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2860-2876, Dec. 2006, DOI: 10.1109/JSSC.2006.884835.

[4] A. Mirzaei, S. Chehrazi, R. Bagheri, and A. A. Abidi, "Analysis of a first-order anti-aliasing integration sampler," in *IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 55, no. 10, pp. 2994-3005, Nov. 2008. DOI: 10.1109/TCSI.2008.924127.*

[5] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," in *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2575-2587, Nov. 2014. DOI: 10.1109/JSSC.2014.2359656.

[6] M. Tohidian, I. Madadi, and R. B. Staszewski, "3.8 A fully integrated highly reconfigurable discrete-time superheterodyne receiver," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2014, pp. 72-73.

[7] I. Madadi, M. Tohidian, and R. B. Staszewski, "Analysis and design of I/Q charge-sharing band-pass-filter for superheterodyne receivers," in *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 2114-2121, Aug. 2015, DOI: 10.1109/TCSI.2015.2437514.

[8] Y. Xu and P. R. Kinget, "A switched-capacitor RF front end with embedded programmable high-order filtering," in *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1154-1167, May 2016, DOI: 10.1109/JSSC.2016.2520359.

[9] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A simplified model for passive-switched-capacitor filters with complex poles," in *IEEE Trans. Circuits Syst. II, Express Briefs*, vol. 63, no. 6, pp. 513-517, June 2016, DOI: 10.1109/TCSII.2016.2530804.

[10] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A 150-μW 3rd-order Butterworth passive-switched-capacitor filter with 92 dB SFDR," *2017 Symp. VLSI Circuits*, Kyoto, June 2017, pp. C142-C143.

[11] P. Payandehnia, H. Maghami, M. Kareppagoudr, and G. C. Temes, "Passive switched-capacitor filter with complex poles for high-speed applications," in *Electronics Letters*, vol. 52, no. 19, pp. 1592-1594, Sept. 2016, DOI: 10.1049/el.2016.2487.

[12] J. Yli-Kaakinen, V. Lehtinen, and M. Renfors, "Multirate charge-domain filter design for RF-sampling multi-standard receiver," in *IEEE Trans.*

Circuits Syst. I, vol. 62, no. 2, pp. 590-599, Feb. 2015, DOI: 10.1109/TCSI.2014.2363514.
[13] P. E. Paro Filho, M. Ingels, P. Wambacq, and J. Craninckx, "An incremental-charge-based digital transmitter with built-in filtering," in *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3065-3076, Dec. 2015, DOI: 10.1109/JSSC.2015.2473680.
[14] P. Payandehnia et al., "A 0.49-13.3 MHz tunable fourth-order LPF with complex poles achieving 28.7 dBm OIP3," in *IEEE Trans. Circuits Syst. I*, vol. 65, no. 8, pp. 2353-2364, Aug. 2018, DOI: 10.1109/TCSI.2017.2788466.
[15] D. A. Johns and K. Martin, *Analog Integrated Circuit Design.* New York, NY, USA: Wiley, 1997.
[16] J. C. Maxwell, "Comparison of the electrostatic with the electromagnetic units," in *A Treatise on Electricity and Magnetism*, 2nd ed., vol. 2, Oxford, England: Clarendon Press, 1881, ch. 19, sec. 3, pp. 384-386.
[17] M. Keskin, N. Keskin, and G. C. Temes, "An efficient and accurate DC analysis technique for switched-capacitor circuits", in *Analog Integrated Circuits and Signal Processing*, vol. 30, no. 3, pp. 239-241, Mar. 2002.
[18] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," in *IEEE IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841-851, Mar. 2008, DOI: 10.1109/TPEL.2007.915182.
[19] M. Ghaderi, J. Nossek, and G. Temes, "Narrow-band switched-capacitor bandpass filters," in *IEEE Trans. Circuits Syst.,* vol. 29, no. 8, pp. 557-572, August 1982, DOI: 10.1109/TCS.1982.1085188.
[20] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," in *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1770-1780, Sept. 2010, DOI: 10.1109/JSSC.2010.2056831.
[21] A. Mirzaei, H. Darabi, J. C. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," in *IEEE Trans. Circuits Syst. I*, vol. 57, no. 9, pp. 2353-2366, Sept. 2010, DOI: 10.1109/TCSI.2010.2043014.

Sevil Zeynep Lüleç (M'14) received the B.Sc. degree from METU, Ankara, Turkey, the M.Sc. degree from EPFL, Lausanne, Switzerland, and the Ph.D. degree from the University of Toronto, Ontario, Canada, all in electrical engineering, in 2008, 2010, and 2019, respectively.

She worked as a Research Engineer at Koc University, Optical Microsystems Laboratory, Turkey, and at METU-MEMS Research and Application Center, Turkey, in between 2010-2012. She joined Analog Devices, Inc., Toronto, Canada as a Mixed Signal Design Engineer in May 2019. Her research interests include analog, RF, and mixed signal IC design, MEMS front-end and system-level design, and plasmonic integrated IR imaging.

Dr. Lulec was a recipient of EPFL Excellence Fellowship, ADI Outstanding Student Designer Award, Huawei Prize, and Ontario Graduate Scholarship. Currently, she is serving as IEEE Solid-State Circuits Society Young Professional Committee Chair.

David A. Johns (S'81–M'89–SM'94–F'01) received the B.A.Sc., M.A.Sc., and Ph.D. degrees from the University of Toronto, ON, Canada, in 1980, 1983, and 1989, respectively.

In 1988, he was hired at the University of Toronto where he is currently a Full Professor. He has on-going research programs in the general area of analog integrated circuits. His research work has resulted in more than 80 publications as well as the 1999 IEEE Darlington Award. Together with academic experience, he also has spent a number of years in the semiconductor industry and was a co-founder of a successful IP company called Snowbush Microelectronics.

Dr. Johns served as a guest editor of the IEEE Journal of Solid-State Circuits and an Associate Editor for IEEE Transactions on Circuits and Systems as well as being a member of the SSCS AdCom from 2002 to 2008.

Antonio Liscidini (M'06–SM'13) was born in Tirano, Italy, in 1977. He received the Laurea (summa cum laude) and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was a summer Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS low-noise amplifiers. From 2008 to 2012, he was an Assistant Professor with the University of Pavia and a Consultant with Marvell Semiconductors, Pavia, in the area of integrated circuit design. In 2012, he moved to the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently an Associate Professor. His research interests are focused on analog mixed signal interfaces with particular emphasis on the implementations of wireless transceivers and frequency synthesizers for cellular and ultra-low power applications.

Dr. Liscidini was a recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits and a co-recipient of the Best Invited Paper Award at the 2011 IEEE Custom Integrated Circuit Conference. He has served as an Associate Editor for the IEEE Transactions on Circuits and Systems II: Express Briefs (2008-2011) (2017- 2018) and as a Guest Editor for the IEEE Journal of Solid-State Circuits (2013) (2016), and Guest Editor on IEEE RFIC Virtual Journal Issue dedicated to frequency synthesizers . Between 2016 and 2018, he has been a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He has been member of the International Solid-State Circuit TPC (2012- 2017) and member of the European Solid-State Circuit Conference TPC (2010-currently) and Custom Integrated Circuit Conference TPC (2018-currently).