
ANALYSIS OF SAMPLE AND HOLD
CIRCUITS FOR ANALOG TO DIGITAL
CONVERTERS

David Halupka

971113290

November 14, 2002

© 2002

TABLE OF CONTENTS

1. INTRODUCTION.....	1
2. ADC ARCHITECTURES.....	2
2.1. Flash Quantizers.....	2
2.2. Folding/Interpolating quantizers.....	6
2.3. Successive Approximation quantizers.....	10
2.4. Sub ranging quantizers.....	12
3. SAMPLE AND HOLD FOR QUANTIZERS.....	13
3.1. Performance requirements of S/H stage for One-Step quantizers.....	15
3.2. Performance requirements of S/H stage for Multi-Step quantizers.....	16
4. FUTURE DEVELOPMENTS OF SAMPLE AND HOLD CIRCUITS AND ANALOG TO DIGITAL CONVERTERS.....	16
5. CONCLUSION.....	17
6. REFERENCES.....	18

1. INTRODUCTION

Most signal processing is performed using digital means, analog circuits are used only for very high speed or low amplitude signal processing [1]. In order to be able to perform digital signal processing on natural signals that are analog in nature, they must first be sampled and quantized into digital form [2]¹.

An analog to digital converter (ADC) converts an analog signal of interest into a digital signal. ADCs are required, as a front end, for most practical digital signal processors (DSPs.) Figure 1 shows a simplified schematic of an ADC; the analog signal is first sampled in the time domain, producing a discrete time signal with a continuous magnitude. This intermediate signal is quantized to produce a signal that is both discrete in time and in magnitude. The sampling operation is usually performed by a sample and hold (S/H) circuit, while the quantization is performed by a quantizer. It is worthwhile to note that most sample and hold circuits actually perform a track and hold function [3], however I shall refer to them as sample and hold without loss of generality.



Figure 1: Block diagram of a typical analog to digital converter.

Most ADCs, as illustrated in figure 1, are composed of two distinct circuit blocks performing the sampling in time and in magnitude. However, for some ADC architectures a S/H block is crucial and for some others it is not necessary in principle [4], as shall be shown. I will also show that jitter (aperture uncertainty or variation in the

¹ The reader is assumed to have knowledge of basic signal processing concepts, which are discussed in [2].

sampling instant) is the main limitation on high performance ADCs [5]. This paper will discuss criteria for when it is necessary to use a S/H circuit at the front end of an ADC. Four ADC architectures will be discussed and the criteria for when a S/H front end is necessary for each will be explored.

2. ADC ARCHITECTURES

ADC architectures can be largely divided into the following two categories, one-step converters and multi-step converters [6]. One-step converters convert the analog signal to digital form almost instantly, whereas a multi-step converter will take more than one clock cycle to perform the conversion: usually utilizing successive approximation.

2.1. FLASH QUANTIZERS

The simplest ADC architecture is the flash quantizer [7]. A B bit flash quantizer employs $2^B - 1$ level comparators arranged in parallel to perform comparison between the analog signal and the reference quantization voltages. A simplified flash quantizer schematic is shown in figure 2. All comparison are done in parallel and ideally at the same time instant. The comparators are designed to evaluate their inputs on either a rising or falling clock edge.

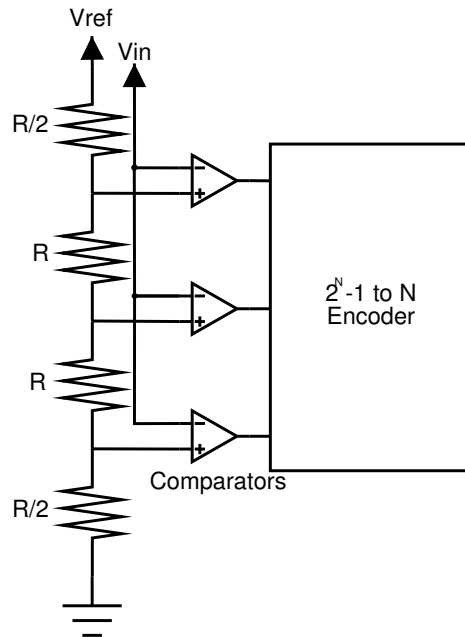


Figure 2: Simplified schematic view of a two bit flash ADC.

The typical resolution of a flash quantizer is usually around 8 bits [7], with higher bit resolutions becoming more rare, since for every additional bit of accuracy the number of comparators doubles. However, well designed flash quantizers can usually achieve high conversion speed and thus a high sampling rate, around 30 mega samples per second [7].

Each of the comparator's reference voltages are biased by a constant voltage higher than the previous. The difference between two successive reference voltages is equal to the voltage level of the least significant bit, or the smallest quantization step. The results of the comparisons are encoded using “thermometer” coding² and then converted to bin-

2 A string of ones represents all of the reference voltages that a current input level exceeds, and zeros for all the reference voltages that the current input level does not exceed, indicating the output signal's amplitude level much like a thermometer.

All of the previously mentioned short comings of flash quantizers cause harmonic distortions³ in the digital signal. All of these problems can be eliminated with a S/H circuit. The S/H circuit relaxes the timing requirements that a flash quantizer has to meet by keeping the input signal constant during the quantizer's evaluation stage.

The main performance limitation of a flash quantizer is the aperture delay time (the maximum allowed combined clock and signal jitter) defined as:

$$T_A = \frac{E_N}{dE_S/dt}$$

Where E_N is the maximum allowable noise in the digital signal, usually one bit⁴, and dE_S/dt is the maximum rate of change of the input signal [7]. Modeling the input as a sine wave, with amplitude equal to the dynamic range of the signal and frequency equal to half the sampling frequency and substituting into the equation for aperture delay results in a maximum aperture delay defined as,

$$T_{A \max} = \frac{LSB}{LSB 2^B \frac{d}{dt} \sin(2\pi \frac{f_S}{2})} = \frac{LSB}{LSB 2^B 2\pi \frac{f_S}{2} \cos(2\pi \frac{f_S}{2})} = \frac{1}{2^B \pi f_S}$$

Where B is the bit resolution of the quantizer and f_S is the sampling frequency. Thus, for a 8 bit 30 MHz flash quantizer the aperture delay time is only 41.5 ps! Meaning the maximum skew between the sampling clock and the input signal between all comparators must be less than 41.5 ps. This is very little time considering the possible layout size of the quantizer, the distance the input signal and clock signals have to travel, and the fan-

3 Harmonic distortion tends to increase in magnitude as the frequency is increased.

4 The smallest error allowed also corresponds to the least significant bit (LSB).

out of the clock and input analog signals. A S/H circuit can eliminate this constraint since the input is held constant during the comparisons, and a distributed sampling clock is no longer necessary for the comparators. Therefore, there is no jitter inherent in the quantizer.

A S/H circuit is not needed for low frequency signals, such as voice, because if the sampling frequency decreases or the precision of the quantizer decreases so does the aperture delay. A voice signal sampled at 22 kHz with 8 bits of precision needs to meet an aperture delay of 56 ns, which is quite a reasonable delay to design for.

2.2. FOLDING/INTERPOLATING QUANTIZERS

The main disadvantage of using a flash quantizer is the number of comparator stages. Thus the layout size, grows as the precision of the quantizer is increased. A folding/interpolating quantizer overcomes this shortcoming by using less comparators while still performing on par with a flash quantizer.

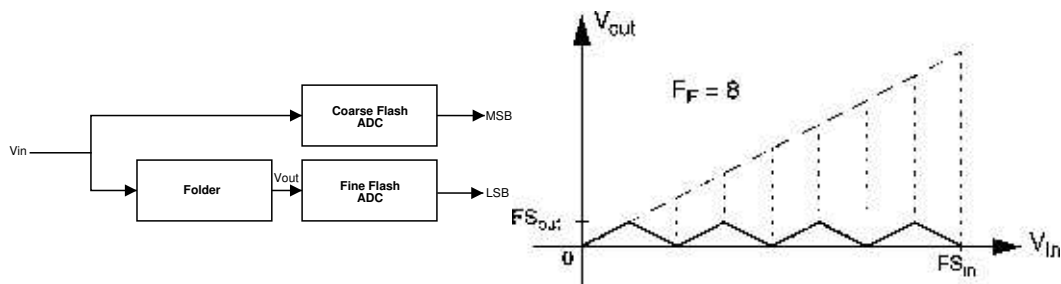


Figure 4: Block diagram of a folding A/D using an ideal folder and the input-output characteristic of an ideal folder with a folding factor of 8 [8].

In a folding/interpolating quantizer the input signal's most significant bits (MSBs) are first estimated by a flash quantizer. Simultaneously, a folding/interpolating circuit performs a modulo-like operation on the signal wrapping the input signal to a smaller voltage range. The resulting signal is then flash converted to get the least significant bits (LSBs) [8]. The simplified signal flow using an ideal folding circuit is shown in figure 4 along with the input/output characteristics of the folder.

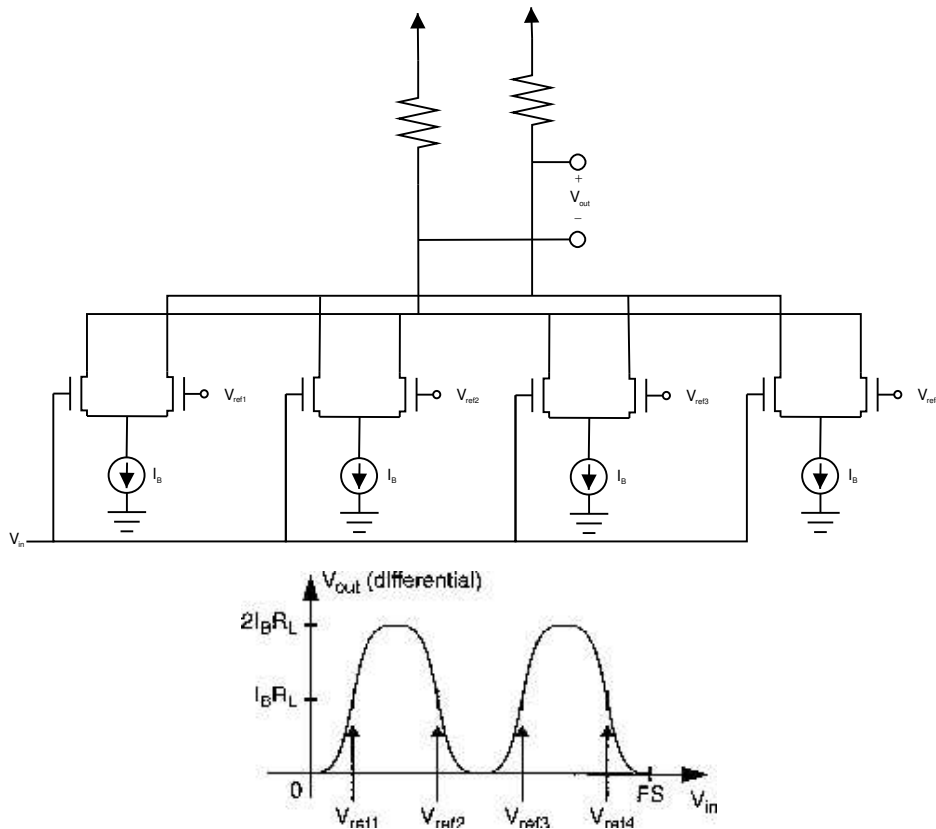


Figure 5: CMOS realization of a folder with folding factor of 4 and the resulting input-output transfer characteristic of the CMOS folder [8].

The folding operation reduces the total number of comparators needed to determine the digital signal. The folding factor, F_F , is the number of segments that the input is folded into: in figure 4 the folding factor is 8. As the number of folds increases, the number of levels needed to be resolved by the flash LSB quantizer drops, since the voltage range that the signal is folded into is of a lower amplitude and does not require as many quantization levels.

The folding circuit is implemented using differential pairs cross connected and tied to an output resistance, as shown in figure 5. This circuit has an input output characteristic that roughly approximates a sinusoid, also shown in figure 5. To avoid distortion only the linear part of the transfer curve is actually used for the folded output [8] that is to be converted by the LSB flash quantizer. However, using the output of this folding circuit would cause great distortion of the LSB bits, as the transfer curve is non-ideal.

To overcome the non-ideal nature of the transfer characteristic, folding is repeated several times in order to arrive at a transfer curve as shown in figure 6. The eight folds in this figure have been offset from each other by one LSB. The comparison needed in this case amounts to one comparator per bit, comparing a folding output to a reference voltage. If a dummy differential pair is inserted into each folding circuit, then the DC offset can be eliminated and a zero-crossing circuit can be used to evaluate the LSBs [8]. To eliminate the large number of differential pairs needed to generate the folds, interpolation circuits can be used to generate intermediate folds. A 6 bit folding/interpolating quantizer would utilize 7 comparators to generate the 3 MSBs, and 8 comparators and 8

folding circuits to generate the 3 LSBs. A flash quantizer would use 63 comparators to generate the required 6 bits of resolution. Thus a folding/interpolating quantizer offers significant savings in the number of comparators required.

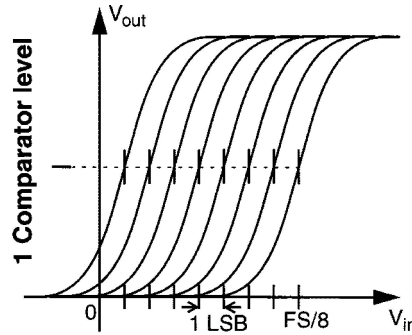


Figure 6: Multiple non-linear folds used to evaluate three LSBs, using 8-non ideal folds with a folding factor of 8.

There are several timing issues that need to be considered during the design of a folding/interpolating circuit without a S/H front end. The folding circuits add an additional delay to the signal path for the LSBs. Therefore, the clocking of the MSBs has to be delayed so that its sequenced with the clocking of the LSBs. This required delay shrinks the aperture time even more than that of a flash quantizer.

Using a simple analysis we can find the approximate aperture time delay at the inputs of the LSB comparators. Using the fact that the folding circuits output bandwidth is related to the input bandwidth by $f_{out} = \sqrt{2} F_F f_i$ and assuming again that the input waveform is the same as for the analysis of the flash quantizer, we can approximate the aperture time as follows,

$$T_A = \frac{1}{2^B \pi f_{out}} = \frac{1}{2^B \pi \sqrt{2} F_F f_S}$$

The aperture time is smaller for the folding/interleaving ADC than for the flash ADC, largely due to the increase in signal bandwidth at the outputs of the folding circuitry and the additional delay through the folders. Moreover, the clocking of the MSB flash quantizer and the LSB comparators must be performed simultaneously. Basically, the input waveform cannot change too much between the time different comparators are strobed, but it cannot also change too much between the time LSBs are generated and the time MSBs are generated. Also, because of the large signal bandwidth at the outputs of the folding circuitry, large phase changes will develop for different frequencies of the signal. Thus the input signal will become distorted at the input to the LSB comparators.

2.3. SUCCESSIVE APPROXIMATION QUANTIZERS

The successive approximation quantizer is an attractive design option for low frequency and high precision quantizers: 8 to 16 bit of resolution at 2.5 MHz is possible [7]. A simple block diagram for a successive quantizer is shown in figure 7. The successive approximation quantizer is simple in its design. The linearity and precision of the quantizer is mainly determined by the linearity and precision of the digital to analog converter (DAC) [7]. Another advantage of the successive approximation quantizer is that it naturally provides the resulting digital data stream in serial fashion, starting with the MSB.

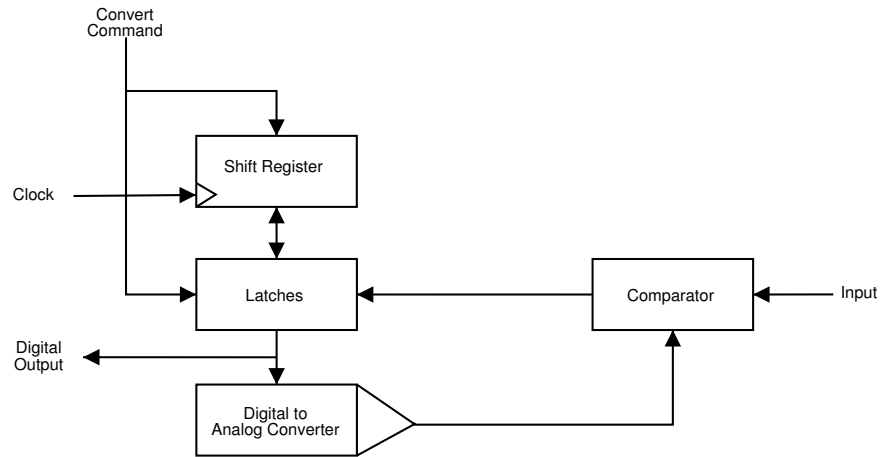


Figure 7: Block diagram of successive approximation ADC [7].

In order to better understand what the aperture delay for the successive approximation quantizer is, we must first understand how it converts an input to digital form. The successive approximation quantizer is idle until it receives a command to start encoding. At the beginning of encoding the bits to the DAC are low except for the most significant bit. The DAC converts this bit vector into a analog signal which is compared to the input signal. From this comparison we make a decision as to whether to keep the MSB on or off; if the input signal exceeds the DAC signal then the MSB stays on, otherwise it is turned off. All successive bits in the bit vector are turned on, one at a time, and the input signal is compared against this new approximation of the input signal to check whether the bit being tested should be kept on or turned off. Once a bit is decided upon it is not changed, until all of the other bits are evaluated [7].

Obviously, the aperture time of the successive approximation quantizer is the conversion time of one bit vector or B iterations for a resolution of B bits. It is necessary to

hold the input signal stable while each successive bit is being evaluated [7]. Thus the speed of the quantizer is greatly influenced by the speed of the digital logic, the speed of the DAC and the speed of the comparator. Moreover, if more bit precision is required, then more iterations are required, and the aperture time is longer. If the input signal is not stable during the conversion process serious distortions will be present in the digital output. Therefore, a S/H front end is absolutely critical for a successive approximating quantizer in order to keep the input waveform stable during the conversion iterations.

2.4. SUB RANGING QUANTIZERS

The sub ranging quantizer is a mixture of concepts from the folding/interpolating quantizer and that of the successive approximating quantizer. Its speed is generally faster than that of the successive approximation quantizer with equivalent bit resolution. A block diagram of this architecture is shown in figure 8.

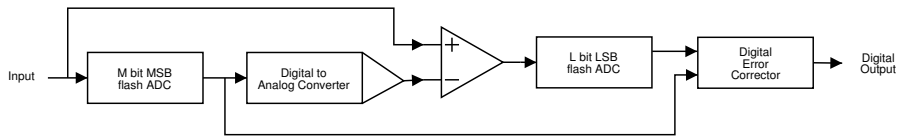


Figure 8: Block diagram of sub ranging ADC quantizer [7].

The operation of this ADC is as follows. The MSB flash quantizer makes a M bit rough approximation of the input signal. This rough approximation is converted back to an analog signal using the DAC. This approximate analog signal is compared to the input analog signal and the difference is amplified and converted to digital form using an L bit LSB flash quantizer. A digital error correction circuit combines the M MSBs and the L

LSBs to obtain the overall B bits of resolution for the sub ranging quantizer. For a sub ranging quantizer to operate properly is it necessary for $M+L>B$, the extra bits are used to encode errors developed internally in the quantizer, which can be corrected using a simple algorithm [7].

The aperture delay time of the sub ranging ADC can be approximated by calculating the time difference between the delay along the critical path from the input to the output and the delay along the shortest path from the input to the output. The longest path, from input to output, in terms of operations is to the LSB quantizer outputs. The shortest path is from the input to the MSB quantizer outputs. This delay is not the maximum delay, since the maximum clock skew between the two ADCs has not been factored in. From this simple analysis it is apparent that the input signal must be held during the time that the MSB quantizer performs its comparison and the time when the LSB quantizer perform its comparison. This is a quite substantial delay, as it is composed of the aperture times of two flash quantizers plus the settling time of the DAC.

3. SAMPLE AND HOLD FOR QUANTIZERS

As shown in the previous two sections, the performance, in terms of distortion, of an ADC is largely influenced by the frequency and amplitude of the signal present at its input. A front end sample and hold circuit, samples the input waveform and then holds it constant during the quantizer's evaluation phase. Thus the frequency of the signal during the evaluation phase is effectively zero, and the aperture delay, or signal/clock jitter is now effectively zero.

Sample and hold circuits come in two flavors, shown in figure 9. The main distinction is in how the capacitor is placed in relation to the signal: in parallel or in series. The switches in these circuits are usually implemented using metal-oxide-semiconductor field-effect transistor (MOSFETs.) The parallel S/H is DC coupled to the input, whereas the serial S/H is not. These simple sample and hold circuits suffer from many non-linearities, such as clock feed-through, charge injection, and input dependent on resistance of the switch. These non-linearities and S/H circuits that eliminate them are further explored by [9 and 10] and will not be explored here further. Ideally these non-linearities should not cause more distortions than we are trying to eliminate by using an S/H front end.

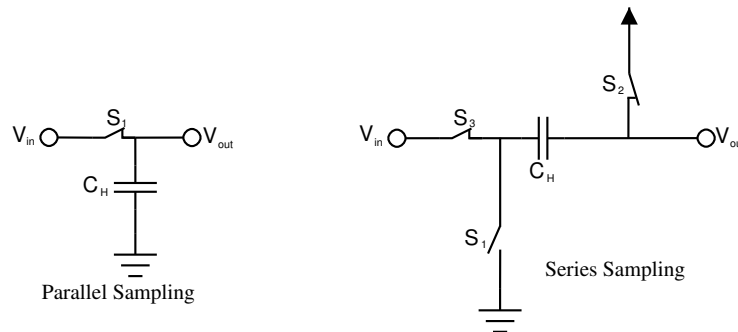


Figure 9: Simple sample and hold circuits illustrating the two main configurations: capacitor in parallel with the signal and a capacitor in series with the signal.

In the previous section it was shown that if the bandwidth required is achievable (aperture delay can be met) then a front end S/H is not necessary. However, even if bandwidth can be met it is beneficial to add a front end S/H to make the design of the following quantizer easier, as timing requirements tend to be less aggressive. The question

that remains to be answered for a sample and hold circuit is what type of performance criteria are important for one step quantizer and for multi-step quantizers.

3.1. PERFORMANCE REQUIREMENTS OF S/H STAGE FOR ONE-STEP QUANTIZERS

For flash and folding/interpolating quantizers the front end S/H circuit is not necessary as each comparator can be configured to perform a “distributed” sampling operation [6]. However timing imperfections in these quantizers degrade performance and increase distortion as input signal frequencies increase. A front end S/H circuit would only have to hold the input signal stable for a short period of time in order for all of the distributed comparators to sample the same input signal level.

Important parameters for S/H circuits for one-step ADCs are acquisition and hold setting times, linearity, jitter, hold-mode feed through, and common-mode compatibility with the ADC [8]. A S/H with short settling times is required so that the S/H does not limit the effective bandwidth of the overall ADC or degrade its performance. It is important that the MOSFET switches have a linear transfer function and constant on resistance, that is effectively independent of input voltage so the RC time constant for charging the capacitor is constant for all input signal amplitudes. Coupling through the MOSFET sampling switch should also be minimal, as for high precision ADCs coupling perturbations in the held signal can cause bit errors, and thus distortions, in the digitized signal. Finally a common DC level between the S/H and the ADC comparators helps in the integration of the two stages.

3.2. PERFORMANCE REQUIREMENTS OF S/H STAGE FOR MULTI-STEP QUANTIZERS

For multi-step quantizers the analog input signal level has to be stable for a relatively long amount of time, in relation to the flash quantizer. Thus the actual speed of the S/H circuit is not as important as its signal holding behavior. The droop rate of the signal while it is being held throughout the conversion cycle should also be less than the LSB. The S/H circuit should be able to reject noise injected onto the hold capacitor from the quantizer, called kickback noise [6]. Moreover, the circuit should be able to recover from any kickback noise injected before the next iteration is about to sample the held signal.

4. FUTURE DEVELOPMENTS OF SAMPLE AND HOLD CIRCUITS AND ANALOG TO DIGITAL CONVERTERS

The current driving trend in integrated chip design is towards system on a chip architectures. With shrinking gate sizes more transistors can be placed onto one piece of silicon, however as transistor dimensions shrink the supply voltage has to scale down accordingly. Designing high speed circuits with low supply voltages is becoming more of a challenge.

The next generation of analog to digital converters would have to be current based in order to cope with a reduced supply voltage. Dynamic current mirrors can be used instead of sample and hold circuits to hold a current constant while a current based analog to digital converter quantizes the current magnitude. This approach has several advant-

ages: increased noise immunity due to the signal (current) not being limited by the supply voltages and no need for locally generated step-up supply voltages.

I recently had the benefit of attending a presentation by a researcher from Intel. He used an ADC to create an on chip digitizing oscilloscope that was able to probe a signal of interest on chip while not adversely loading the circuit under test. This is a novel application of ADCs, one that I would think will probably drive researchers towards developing more precise and fast ADC along with more linear and robust S/H circuits.

5. CONCLUSION

The governing criteria as to whether a sample and hold (S/H) circuit is required at the front end of an analog to digital converter (ADC) is the input and clock jitter (aperture uncertainty.) S/H circuits greatly reduce the complexity of the design of an ADC by lessening the timing constraints that have to be met by the quantizer while at the same time lowering the bandwidth requirements of the comparators in the quantizer and of the ADC itself. In general, S/H circuits greatly improve the AC performance of an ADC. We have also seen that for some ADCs (successive approximation and sub ranging) a S/H circuit is mandatory, as the architecture of the design requires that the input is stable for the duration of the conversion.

REFERENCES

- [1] C. W. Therrien, *Discrete Random Signals and Statistical Signal Processing*, Prentice-Hall, Inc., New Jersey, 1992.
- [2] A. V. Oppenheim, R. W. Schaffer, *Discrete-Time Signal Processing*, Prentice-Hall, Inc., New Jersey, 1999.
- [3] U. Gatti, F. Maloberti, and G. Palmisano, "An Accurate CMOS Sample-and-Hold Circuit," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 1, pp. 120-122, 1992.
- [4] M. A. M. Zin, et al., "A High-Speed CMOS Track/Hold Circuit," *IEEE International Conference on Electronics, Circuits and Systems 1999*, vol. 3, pp. 1709-1712, 1999.
- [5] D. Jakonis, C. Svensson, "A 1 GHz Linearized CMOS Track-and-Hold Circuit," *IEEE International Symposium on Circuits and Systems*, vol. 5, pp. 577-580, 2002.
- [6] B. Razavi, "Design of Sample-and-Hold Amplifiers for High-Speed Low-Voltage A/D Converters," *Proceedings of the IEEE 1997 Custom Integrated Circuits Conference*, pp. 59-66, 1997.
- [7] M. Koen, "High Performance Analog to Digital Converter Architectures," *Proceedings of the 1989 Bipolar Circuits and Technology Meeting*, pp. 35-43, 1989.
- [8] S. Limotyrakis, K. Y. Nam, B. A. Wooley, "Analysis and Simulation of Distortion in Folding and Interpolating A/D Converters," *IEEE Transactions on Circuits and Systems - II: Analog and Digital Signal Processing*, vol. 49, no. 3, pp. 161-169, 2002.
- [9] J. C. W. Wong, "CMOS Sample-and-Hold Circuits," Department of Electrical and Computer Engineering, University of Toronto, Toronto, 2001.
- [10] E. Säll, "Design of a Low Power, High Performance Track-and-Hold Circuit in 0.18 μm CMOS Technology," Master Thesis, Department of Electrical Engineering, Linköping University, Sweden, 2002.
- [11] D. A. Mercer, "A 12-b 750-ns Subranging A/D Converter with Self-Correcting S/H," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 12, pp. 1790-1799, 1991.
- [12] M. A. Mohamed Zin, et al., "A High-Speed CMOS Track/Hold Circuit," *The 6th IEEE International Conference on Electronics, Circuits and Systems*, vol. 3, pp. 1709-1712, 1999.