5.7 A 2.5dB NF Direct-Conversion Receiver Front-End for HiperLAN2/IEEE802.11a

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The continuous rise in the cut-off frequency of bipolar and MOS devices in modern scaled technologies allows the use of feedback circuit topologies to process signals even in the GHz range. This is attractive for the design of wireless transceivers where feedback can facilitate low-noise solutions under matching conditions and improve circuit linearity [1]. In this paper, we exploit the potential of a feedback-controlled LNA that demonstrates excellent performance in terms of noise and linearity. The proposed topology lends itself to multi-standard/multi-band applications. This work is tailored to a HiperLAN2/IEEE802.11a system, including the down-extension to the 4.9GHz Japanese band. The SiGe 0.25μm BiCMOS technology is used and the chip, adopting a direct conversion architecture, comprises LNA and variable gain quadrature mixers.

Figure 5.7.1 shows the LNA diagram of principle. The voltage-voltage feedback loop, built around transistor T_1, controls the output voltage V_{out}, comparing the base and the emitter voltage signals (v_b and v_e respectively). The feedback network is assumed ideal with a feedback factor equal to α. Analytical expressions for the main parameters of interest (input impedance Z_{in}, frequency transfer function $T(j\omega)$, and noise factor F at peak gain), derived assuming the inductor L_C noiseless and implementing a large impedance at signal frequency, are as reported in Fig. 5.7.1. The feedback loop input reflects the load impedance. The input matching is made narrow-band employing a narrow-band load, and frequency-tunable load by simply tuning the output load. The input matching frequency is automatically aligned to the peak gain frequency. This is particularly advantageous in the frame-work of multi-band/multi-standard applications because tuning of one single LC network allows band-switching. The main contributions to the noise factor come from the shot noise in the base and collector currents, the thermal noise in the base and load resistances (R_b and R_{load} respectively). Due to the opposite dependence on the biasing current of the various contributions, the noise factor presents a minimum value. This minimum is very broad and can be considered almost constant above 3mA.

The adopted feedback linearizes the circuit. In impedance matching conditions, the amplitude of the signal that modulates the base-emitter junction, determining the LNA non-linearity, is $V_i/2g_mR_S$, with g_m the transconductance of T_1 and R_S the source resistance. For g_mR_S approaching infinity, v_b-v_e approaches 0 meaning the non-linearities of T_1 are not explored and the input-output response is linear. As a comparison in a common base LNA the signal modulating the base-emitter junction is $V_i/2$.

Figure 5.7.2 shows the realized differential LNA. The feedback is made of capacitive elements and $\alpha=C_1/(C_1+C_2)$. A bank of 3 capacitors, connected to the LNA output by means of MOS switches, realizes, together with inductor L_{load}, a tunable LC load with 8 bands between 4.9GHz and 5.825GHz. The different selectable bands overlap with each other and cover the IEEE802.11a and HiperLAN2 bands. The inductors L_{SMD} are external SMD devices. From simulations, peak gain=23dB, NF=1.6dB and IIP3=0dBm, with 6mA current.

The I and Q mixers are modified Gilbert cells. Figure 5.7.3 reports the schematic. The input stage uses NMOS differential pairs instead of bipolars for linearity reasons. Pseudo-differential structures are chosen to improve IIP3. PMOS transistors P_1 and P_2 are used for current boosting, allowing low-noise without linearity degradation. Bipolar transistors are used in the switching stage, due to lower 1/f noise and faster commutation. Differential inductor L_{diff} cancels out the parasitic capacitances at local oscillator (LO) frequency, improving dynamic range [2]. A resistive load minimizes 1/f noise contribution. The penalty is a large voltage room.

A variable gain feature is implemented in the mixers. The variable gain control node (V_{gc}) activates 5 switches plus a variable resistor and, while reducing the gain, produces the following effects: 1) P_1 and P_2 are switched off resulting in higher switching pair current with benefit to linearity; 2) the DC output level is the same as in high gain mode because the increase in the output current balances the resistance reduction from R_1+R_2 to R_2; 3) transistor P_3 works in linear region and, together with R_2, determines the load resistance i.e. the low gain value; 4) capacitors C_2 increase the load capacitance to compensate for the reduced resistance, keeping the output pole at the same frequency as in high gain mode.

The front-end fabricated in the STMicroelectronics BiCMOS7G process is housed in a 36-pin plastic package. Figure 5.7.4 shows the chip micrograph. All the pads are ESD protected. The die area is 1.6mm^2. Figure 5.7.5 shows S_{11}. The 8 measured curves correspond to all the possible combination of the LNA switches. The front-end input is matched between 4.6GHz and 5.9GHz, i.e. HiperLAN2/IEEE802.11a are covered with margin. Figure 5.7.6 shows the gain measured as a function of the RF input frequency, with an LO frequency 500kHz apart. The LO power is 0dBm. As evident, finely slicing the overall band allows maximum receiver gain in each band of interest. When the variable gain control is activated the gain reduction is 11dB. The output DC voltage differs by 30mV between the two gain modes. The output pole is located at 10.5MHz and at 12MHz in high and low-gain condition, respectively. The measured I and Q matching is better than 0.3dB. The noise figure is evaluated in each band and the maximum value is 2.5dB. A minimum 2.3dB value is measured, but 0.2dB are considered within the measurement setup error. In minimum gain condition, the NF is equal to 2.9dB. Third order inter-modulation distortion is evaluated injecting two tones 20MHz and 40.5MHz from the LO frequency. The resulting IIP3 is –9.5dBm in high gain mode and –6dBm in low gain mode. For second order inter-modulation distortion the two tones are at 40MHz and 40.5MHz and IIP2=23dBm. The chip draws 16mA from 2.5V. The measurement results are summarized in Fig. 5.7.7.

Acknowledgments:
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References:
[1] D. Cassan, J. Long, "A 1V Transformer Feedback Low-Noise Amplifier for 5GHz Wireless LAN in 0.18μm CMOS," *IEEE J. Solid-State Circuits*, vol. 38, pp. 427-435, Mar. 2003.
[2] H. Sjoland, A. Karimi-Sanjani, A. Abidi, "A Merged CMOS LNA and Mixer for a WCDMA Receiver," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1045-1050, Jun. 2003.

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$$Z_{in} \cong \frac{1}{g_m} + \alpha \cdot Z_{load}$$

$$T(j\omega) \cong \frac{Z_{load}}{R_S + \frac{1}{g_m} + \alpha \cdot Z_{load}}$$

$$F \cong 1 + \frac{1}{2} \cdot \frac{1}{g_m \cdot R_S} + \frac{R_b}{R_S} + \frac{g_m \cdot R_S}{2 \cdot \beta} + \frac{1}{R_{load} \cdot R_S}\left(R_S + \frac{1}{g_m}\right)^2$$

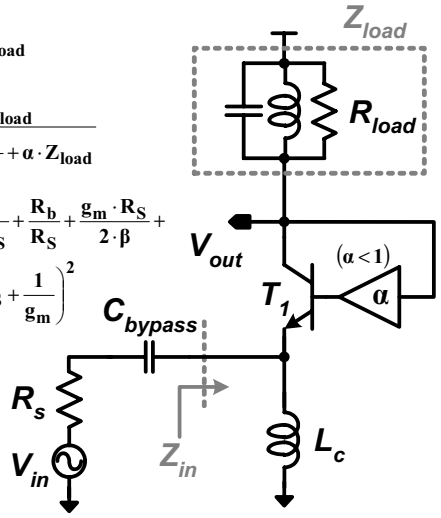

Figure 5.7.1: LNA diagram of principle.

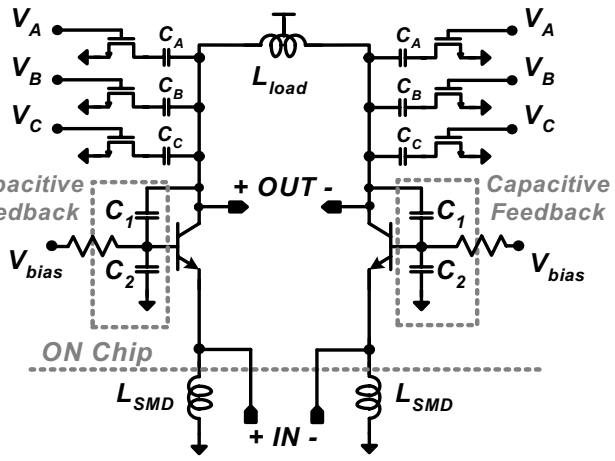

Figure 5.7.2: LNA schematic.

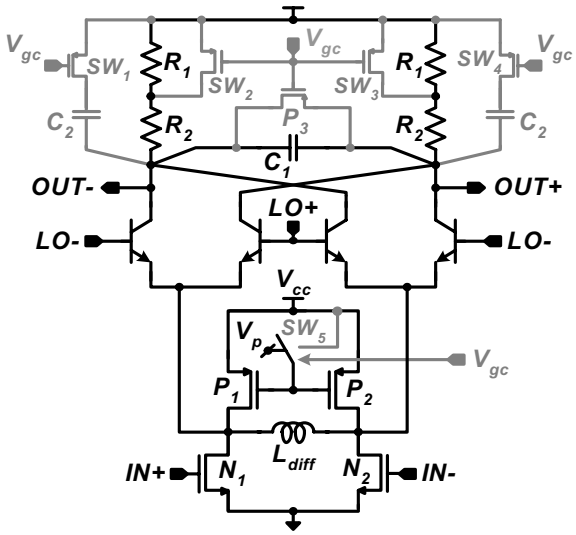

Figure 5.7.3: Mixer schematic.

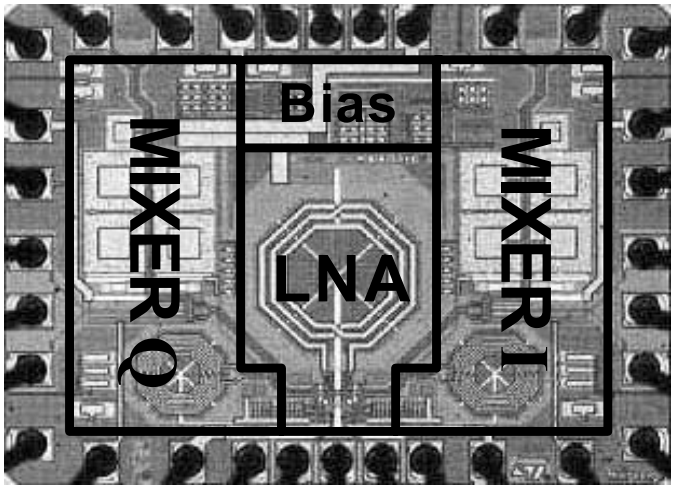

Figure 5.7.4: Die micrograph.

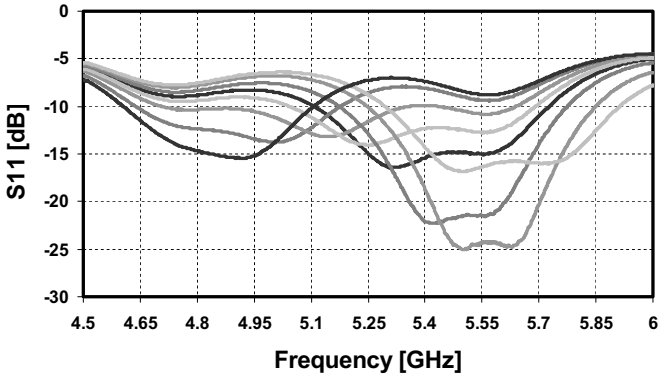

Figure 5.7.5: S11 versus frequency.

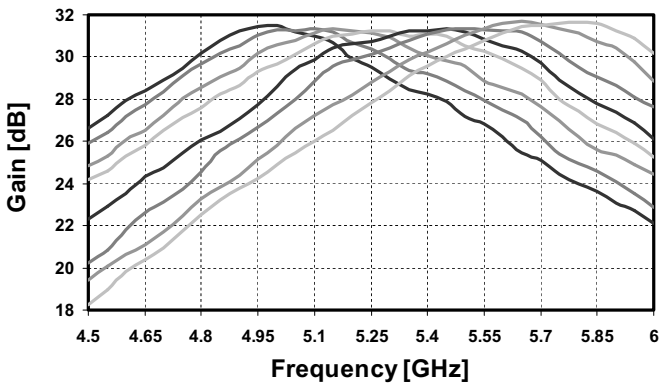

Figure 5.7.6: Gain versus frequency.

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	High Gain	Low Gain
Voltage Gain [dB]	31.5	20.5
NF [dB]	2.5	2.9
IIP3 [dBm]	-9.5	-6
IIP2 [dBm]	23	31
Voltage Supply [V]	2.5	
Current consumption [mA]	16	
Die area [mm^2]	1.6	
Package	QFN 36	
Technology	STM-BiCMOS7G	

Figure 5.7.7: Measurement summary.

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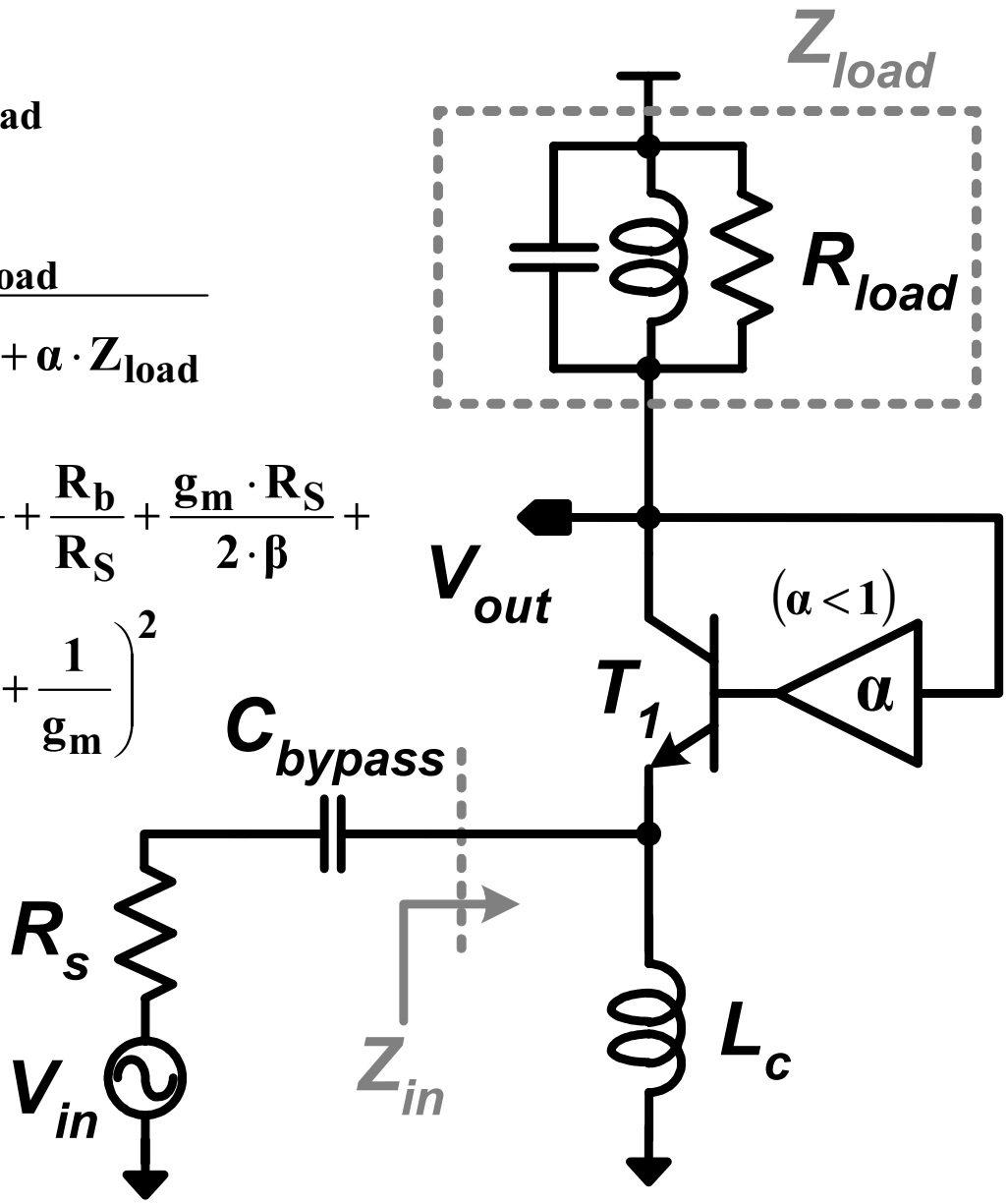

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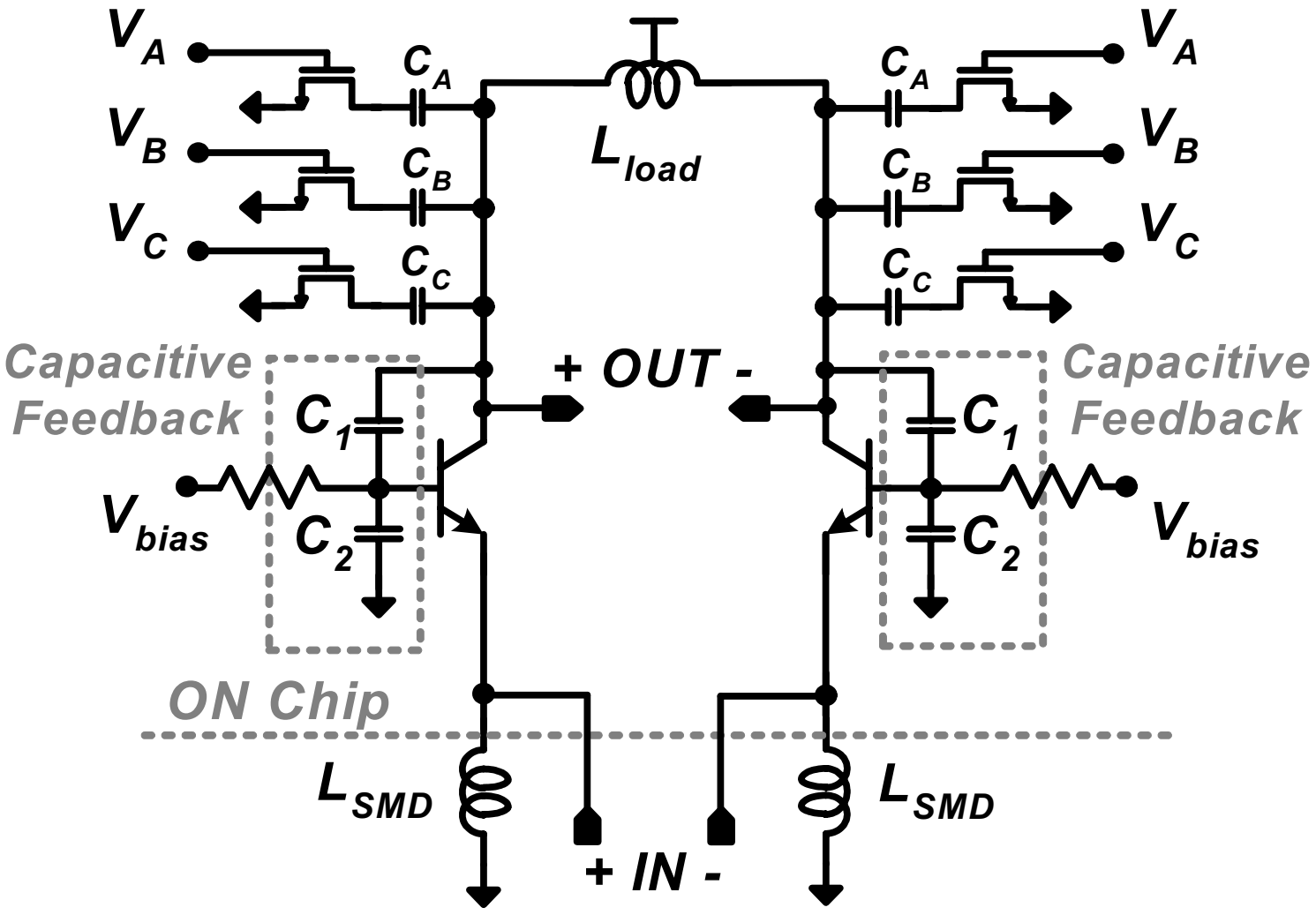

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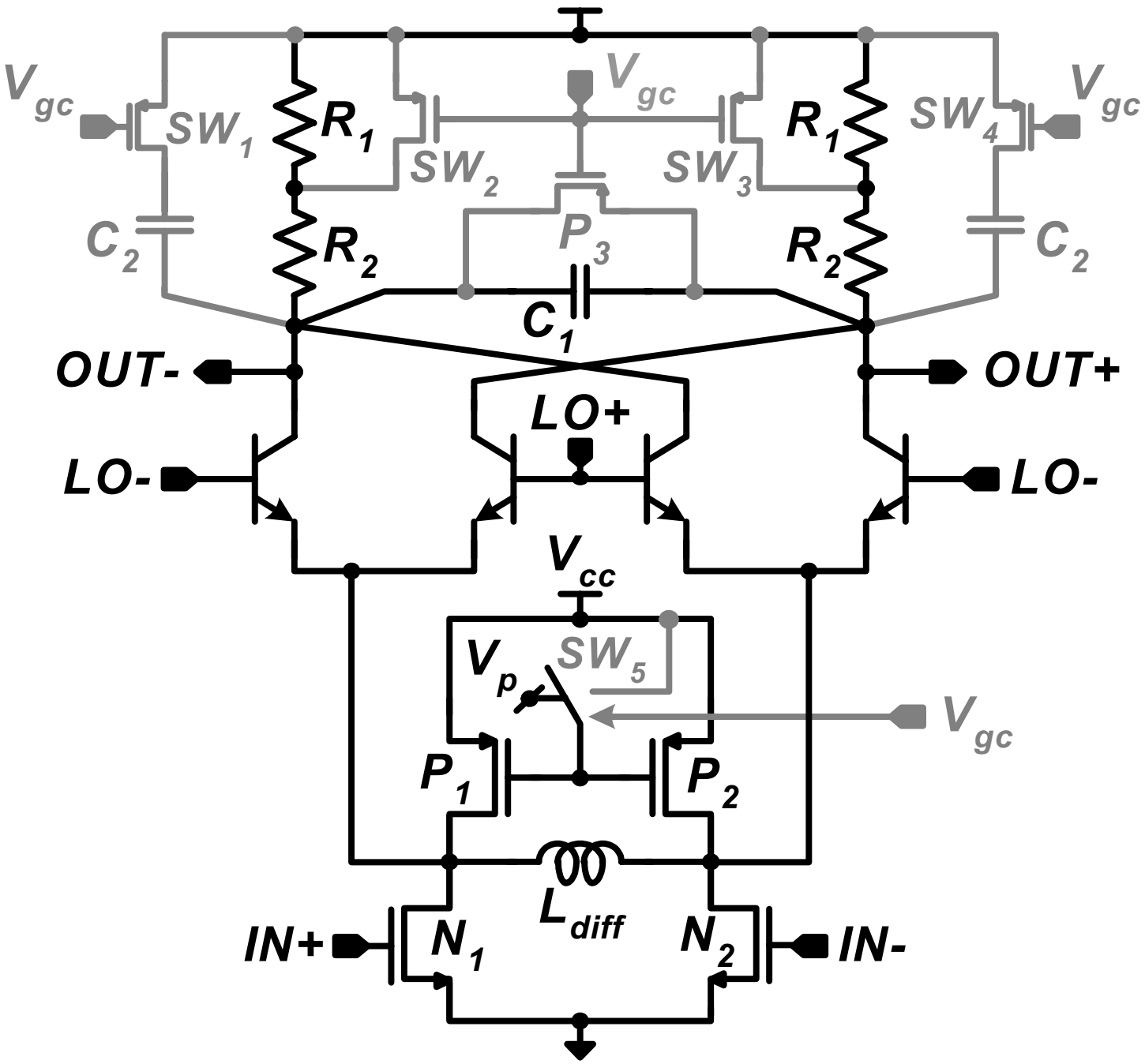

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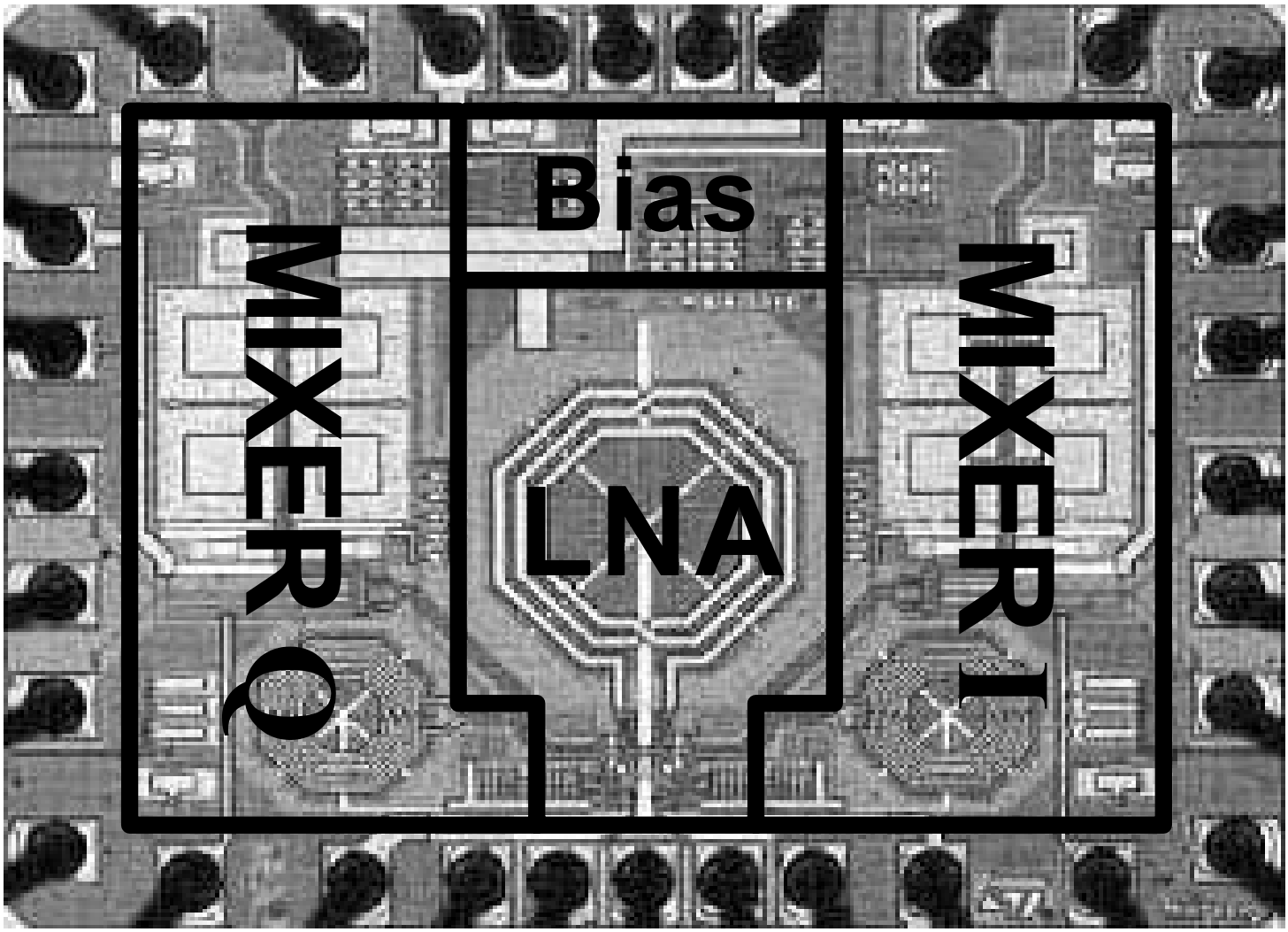

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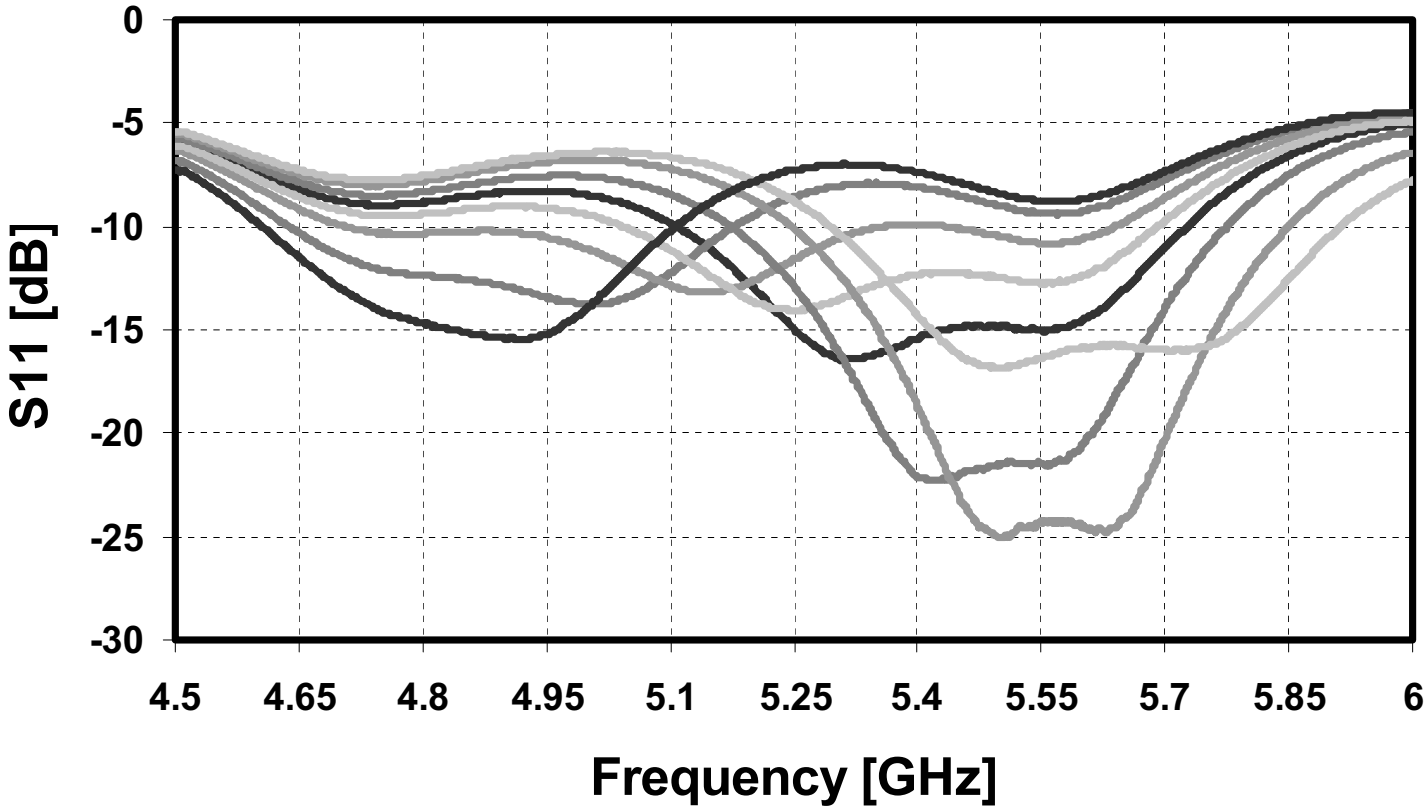

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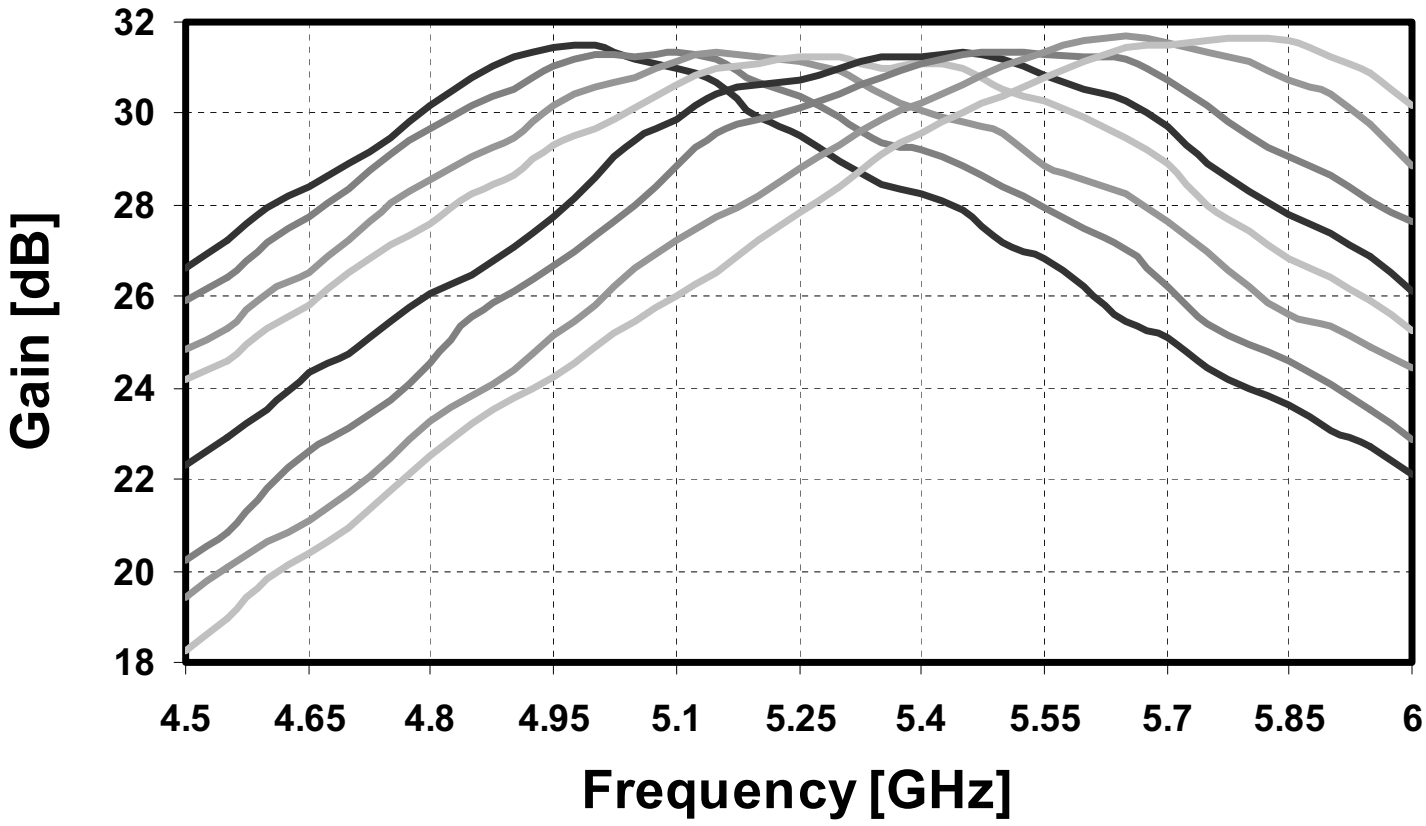

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