A Variable Gain RF Front-End, Based on a Voltage–Voltage Feedback LNA, for Multistandard Applications

Paolo Rossi, *Student Member, IEEE*, Antonio Liscidini, *Student Member, IEEE*, Massimo Brandolini, *Student Member, IEEE*, and Francesco Svelto, *Member, IEEE*

***Abstract*—Employing feedback circuits in RF front-ends can be a key aspect for easy reconfiguration of multistandard receivers. A narrow-band filter can shape the frequency transfer function and, by reflection due to the feedback network, the input impedance. Switching one single filter component thus allows selecting a different standard. We introduce a voltage–voltage feedback low noise amplifier that, besides being easily reconfigurable, shows roughly the same noise and better linearity, for same power consumption, as the conventional inductively degenerated topology. A direct conversion front-end, including the LNA and I and Q mixers, tailored to WLAN applications in the 5–6 GHz range, has been realized in a 0.25-μm SiGe BiCMOS process. Prototypes show the following performances: 2.5 dB NF, 31.5 dB gain, $-$ 9.5 dBm IIP3, and $+$23 dBm minimum IIP2 while consuming 16 mA from a 2.5 V supply.**

***Index Terms*—BiCMOS, direct conversion, feedback amplifier, HiperLAN2, HiSWANa, IEEE 802.11a, low noise amplifier (LNA), mixer, multiband, multistandard, RF receiver, wireless local area network (WLAN).**

I. Introduction

THE current scenario of portable wireless systems is characterized by several communication standards widely differentiated for both supported services and geographical areas. The key aspect for global mobility is the capability to efficiently exploit the available resources. This stimulates the research and development of transceivers, compact, highly integrated, and able to support as many communication standards as possible. Several solutions have been proposed in order to increase the reuse of hardware resources [1]–[6]. Peculiar challenges in the design of these systems are reconfigurability and programmability. Up to now, the block sharing in multistandard receivers is limited to base-band and, only in some cases, to quadrature mixers.

Inductively degenerated low noise amplifiers (LNAs) are intrinsically narrow-band and do not lend themselves to multiband/multistandard applications [7]. Several RF front-ends in parallel, each dedicated to a single standard, are usually adopted [4]–[6]. Topologies, able to continuously cover a broadband, have been proposed to process signals belonging to different standards [8], [9]. The main drawback of this approach is a stringent linearity requirement, because out-of-band interferers are not filtered out at all. In feedback based LNAs a narrow-band, frequency tunable load shapes both the transfer function and the input impedance, so that switching one single reactive element allows selection of a different standard [10], [11]. In this paper, we propose an LNA with voltage–voltage feedback network, realized by means of theoretically noiseless elements. Fig. 1 shows the circuit diagram. The proposed feedback LNA is more linear than the inductively degenerated solution, for the same noise and consumption.

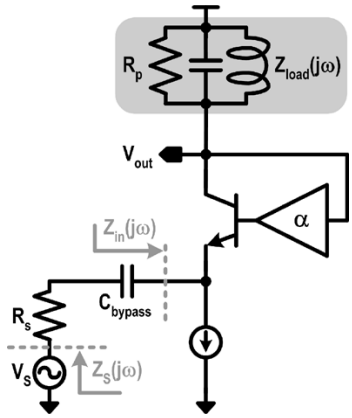

Fig. 1. Diagram of principle of the feedback LNA.

An RF front-end, comprising the newly introduced LNA and I and Q variable gain mixers, tailored to IEEE 802.11a, ETSI HiperLAN2, and MMAC HiSWANa has been realized in a 0.25-μm SiGe BiCMOS technology. Prototypes show the following performances: 31.5 dB gain, 2.5 dB NF, $-$ 9.5 dBm IIP3, and $+$ 23 dBm minimum IIP2 while drawing 16 mA from a 2.5-V supply.

This paper is organized as follows. Section II describes the voltage–voltage feedback LNA and analytical expressions for input impedance, frequency transfer function, noise figure, and IIP3 are derived. Section III proposes the design of the receiver front-end for multistandard wireless local area network (WLAN) applications. The experimental results are discussed in Section IV and conclusions are drawn in Section V.

Manuscript received July 7, 2004; revised October 4, 2004. This work was supported by the Italian National Program F.I.R.B. under Contract RBNE01F582.

P. Rossi was with the Department of Electronics, University of Pavia, I-27100 Pavia, Italy. He is now with Maxim Integrated Products, I-20089 Rozzano (Milan), Italy (e-mail: prossi@design.mxim.com).

A. Liscidini, M. Brandolini, and F. Svelto are with the Dipartimento di Elettronica, Università degli Studi di Pavia, Pavia, Italy (e-mail: antonio.liscidini@unipv.it; massimo.brandolini@unipv.it; francesco.svelto@unipv.it).

Digital Object Identifier 10.1109/JSSC.2005.843631

II. Voltage–Voltage Feedback LNA

Inductively degenerated LNAs do not lend themselves to multistandard applications because both input and output stages should be reconfigured and precisely realigned around each new band. In particular, tuning of input stage reactive elements is troublesome because any introduced switching element would severely impair noise performance. On the contrary, the here proposed feedback solution can be reconfigured simply by means of load switching.

Referring to Fig. 1, the application of the feedback theory allows easy determination of $Z_S(j\omega)$, the impedance between the voltage source terminal and ground:

$$Z_S(j\omega)=Z_{\rm OL}(j\omega)\cdot[1+G_{\rm loop}(j\omega)]=Z_{\rm OL}(j\omega)\cdot[1+\alpha\cdot A(j\omega)] \tag{1}$$

where $Z_{\rm OL}(j\omega)=R_S+(1/g_m)/(1+j\omega(C_\pi/g_m))\simeq R_S+1/g_m$ is the open-loop input impedance, $G_{\rm loop}(j\omega)=\alpha\cdot A(j\omega)$ is the loop gain and $A(j\omega)$ is the open-loop voltage gain.

$A(j\omega)$ is easily determined by inspection of the circuit:

$$A(j\omega)=\frac{g_m}{1+g_m\cdot R_S}\cdot Z_{\rm load}(j\omega) \tag{2}$$

with $Z_{\rm load}(j\omega)$ the load impedance.

Combining (1) and (2) gives

$$\begin{aligned} Z_S(j\omega)&=\left(R_S+\frac{1}{g_m}\right)\cdot\left[1+\alpha\cdot\frac{g_m}{1+g_m\cdot R_S}\cdot Z_{\rm load}(j\omega)\right]\\ &=R_S+\frac{1}{g_m}+\alpha\cdot Z_{\rm load}(j\omega). \end{aligned} \tag{3}$$

The input impedance $Z_{\rm in}(j\omega)=1/g_m+\alpha\cdot Z_{\rm load}(j\omega)$ is purely resistive at the load resonance frequency. The LNA is thus matched to the source resistance, provided $1/g_m+\alpha\cdot R_p=R_S$, where R_p is the tank parallel resistance at resonance.

Based on (2), the frequency transfer function $T(j\omega)$ is easily determined:

$$T(j\omega)=\frac{A(j\omega)}{1+\alpha\cdot A(j\omega)}=\frac{\frac{Z_{\rm load}(j\omega)}{R_S}}{1+\frac{1}{R_S}\left(\frac{1}{g_m}+\alpha\cdot Z_{\rm load}(j\omega)\right)}. \tag{4}$$

In matching conditions, the peak gain is equal to $R_p/2R_S$. The corresponding frequency is at the load resonance, aligned to the input matching frequency. Switching one load component allows switching the input impedance and peak gain frequencies, simultaneously. This is a great advantage over the inductively degenerated topology because there is no need to switch components at LNA input thus avoiding performance degradation and allowing area saving. A bank of switchable capacitors at output load makes the LNA suitable for multiband reception of alternative standards, while multiresonant loads allows realizing concurrent solutions [12].

This voltage–voltage feedback LNA can be looked at as an evolution of the common base LNA. The feedback loop provides a degree of freedom so that impedance matching does not set transistor biasing current. As opposite, the current is a design parameter to reduce noise and improve linearity.

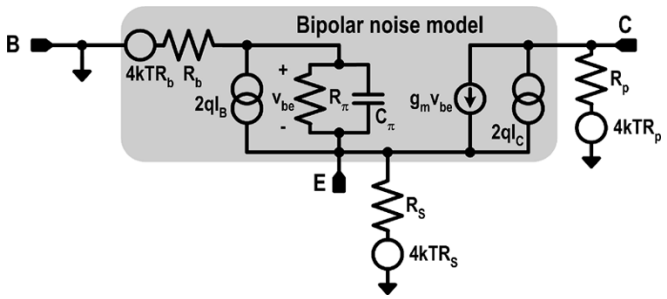

Fig. 2. Small-signal equivalent circuit with noise sources relative to the common base topology.

A. Noise Figure

Assuming a noiseless feedback network and an ideal current source as in Fig. 1, the noise analysis of the voltage–voltage topology can be performed, based on the corresponding common base structure. The noise factor ($F_{\rm FL}$) at resonance is determined by inspection of the equivalent circuit of Fig. 2:

$$\begin{aligned} F_{\rm FL}=1+\frac{R_b}{R_S}+\frac{g_mR_S}{2\beta}+\frac{1}{2g_mR_S}+\frac{g_mR_S}{2}\cdot\left(\frac{\omega_0}{\omega_T}\right)^2\\ +\frac{R_S}{R_p}\cdot\left[\left(1+\frac{1}{g_mR_S}\right)^2+\left(\frac{\omega_0}{\omega_T}\right)^2\right] \end{aligned} \tag{5}$$

where R_b is the base spreading resistance and R_b/R_S its thermal noise contribution. The third term accounts for the shot noise in the base current, fourth and fifth are due to the shot noise in the collector current, while the last is the thermal noise due to the load equivalent resistor.

The various contributions in (5) have different dependence on the transconductance, i.e., on the biasing current, suggesting an optimum current value for minimum noise. In a common base topology, matching the input impedance to the signal source sets $g_m=1/R_S$, i.e., sets the biasing current thus preventing noise minimization. The noise factor ($F_{\rm CB}$), for $\omega_0\ll\omega_T$, can be expressed as:

$$F_{\rm CB}\simeq\frac{3}{2}+\frac{R_b}{R_S}+4\frac{R_S}{R_p}. \tag{6}$$

Assuming $R_b=5\ \Omega$, $R_S=50\ \Omega$, and $R_p=500\ \Omega$ as typical values gives ${\rm NF_{CB}}=10\cdot{\rm Log}(F_{\rm CB})=3$ dB. The common base topology is thus too noisy, given the sensitivities required by typical wireless standards.

On the contrary, the impedance matching in the voltage–voltage feedback topology is guaranteed by the feedback network, and minimum noise can be simultaneously achieved. Curve a in Fig. 3 plots the noise figure of the LNA in feedback loop (${\rm NF_{FL}}=10\cdot{\rm Log}(F_{\rm FL})$) versus the biasing current, at 5 GHz, with the same assumptions and parameter values as in the common base example. ${\rm NF_{FL}}$ minimum is 1.15 dB. The minimum is very broad, and above 2 mA the noise figure is already reduced to less than 1.5 dB.

Also in the inductively degenerated topology, the noise performance can be optimized under matching conditions. In fact, source impedance matching sets the values of the input stage reactive elements, for given device cut-off frequency. The current

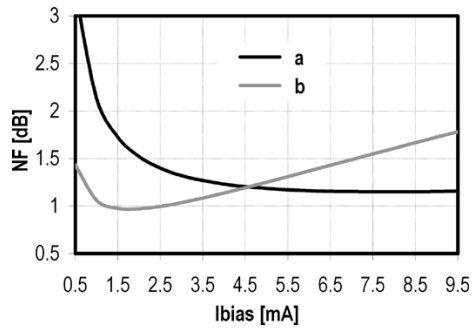

Fig. 3. Equations (5) and (7) versus biasing current at 5 GHz. $R_b = 5\ \Omega$, $R_S = 50\ \Omega$, $R_p = 500\ \Omega$, and $\beta = 150$.

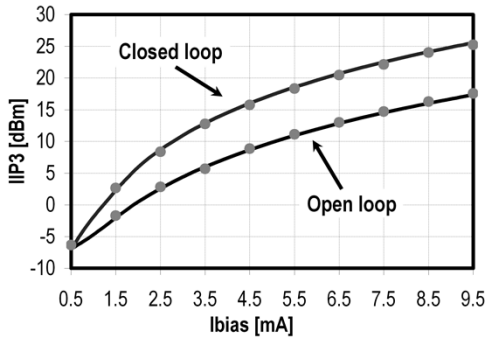

Fig. 4. Equations (8) and (9) as a function of biasing current (solid line). Simulations (dots) are also reported.

can thus optimize the noise performance. According to [13], an analytical expression for the noise factor of the inductively degenerated topology (F_{ID}), at resonance, is given by

$$F_{ID} = 1 + \frac{R_b}{R_S} + \frac{g_m R_S}{2\beta} + \frac{1}{2\beta \cdot g_m R_S} \cdot \left(\frac{\omega_T}{\omega_0}\right)^2 + \frac{g_m R_S}{2} \cdot \left(\frac{\omega_0}{\omega_T}\right)^2 + 4 \cdot \frac{R_S}{R_p} \cdot \left(\frac{\omega_0}{\omega_T}\right)^2. \quad (7)$$

Comparing (5) and (7) confirms the intuition derived from inspection of the two LNA circuit topologies. In fact, the shot noise contribution in the base current is magnified by the input resonant circuit of the inductively degenerated LNA and gives rise to a more important contribution in (7) (third and fourth terms) than in (5). As opposite, the shot noise in the collector current and the load thermal noise contributions are made weaker due to the larger input transconductance. To gain more insight, (7) has been plotted in Fig. 3 (curve b). The two noise minima differ by 0.2 dB with curve b being lower. On the other hand, the NF of the inductively degenerated LNA increases quite rapidly, the difference being negligible for current values where linearity requirements usually suggest biasing. Both solutions allow noise performance adequate for the most stringent applications.

B. Linearity

By inspection of the circuit in Fig. 1, in input impedance matching conditions, the amplitude of the signal that modulates the base-emitter junction, determining the LNA nonlinearity, is $v_S/2g_mR_S$. The larger g_m, the lower the voltage signal, meaning the nonlinearities of the input transistor are less explored and the input–output relation is more linear. As a comparison, in a common base LNA matched to 50 Ω, the modulating signal is $v_S/2$. The improvement in linearity of the feedback LNA, with respect to the 50 Ω–matched common base topology, is due both to the increase in the biasing current and to the beneficial effect of the feedback network α. The two effects are separately analyzed. Detailed calculations are carried out in the Appendix . The resulting IIP3, when the feedback network α is open ($\mathrm{IIP3_{OL}}$) and closed ($\mathrm{IIP3_{CL}}$) are given by

$$\mathrm{IIP3_{OL}} = \frac{4 \cdot V_T^2}{R_S} \cdot \left|\frac{(1+g_mR_S)^4}{1-2g_mR_S}\right| \quad (8)$$

$$\mathrm{IIP3_{CL}} = \frac{4 \cdot V_T^2}{R_S} \cdot \left|\frac{(1+g_mR_S)^4}{1-2g_mR_S}\right| \cdot \left|\frac{2g_mR_S}{1+g_mR_S}\right|^3 \cdot \left|\frac{1-2g_mR_S}{\frac{3}{2g_mR_S} - 2g_mR_S - \frac{1}{2}}\right| \simeq \mathrm{IIP3_{OL}} \cdot |1+G_{\mathrm{loop}}|^3 \quad (9)$$

where V_T is the thermal voltage.

For $g_m \gg 1/R_S$, $\mathrm{IIP3_{OL}}$ grows as the transconductance cube, i.e., as the biasing current cube. Furthermore, at resonance $\mathrm{IIP3_{CL}} \simeq 8 \cdot \mathrm{IIP3_{OL}}$, being $G_{\mathrm{loop}} \simeq 1$.

To validate the analysis, simulations have been performed and the results are reported in Fig. 4 versus the biasing current. Calculated values, reported as solid lines, are in very good agreement.

In the conventional inductively degenerated topology noise figure trades with linearity, allowing modest linearity performance when extremely low noise figures are required [14]. Techniques aimed at increasing the stage linearity, based on the implementation of a low input impedance at low frequency have been proposed [15], [16]. Several realizations demonstrate the effectiveness of these techniques. Nevertheless many drawbacks arise: need for external components and increase in power consumption due to auxiliary circuits, as examples. A comparison between linearities of the two alternative LNAs reveals favorable to the voltage–voltage LNA proposed here, for the same consumption [16], [17].

III. Design of the Multistandard Front-End for WLAN Applications

The block diagram of the 0.25 μm SiGe BiCMOS direct conversion receiver front-end is reported in Fig. 5. The solution is tailored to WLAN applications in the 5–6 GHz range and intended for operability in different geographical areas (North America, Europe, and Japan). As shown in Fig. 6, the corresponding standards cover roughly 1 GHz band, however divided in sub-bands smaller than 250 MHz [18]–[20]. This fragmented frequency allocation suggests solutions other than broadband LNAs. A narrow-band reconfigurable amplifier can finely slice the whole frequency range to alternatively select each band of interest.

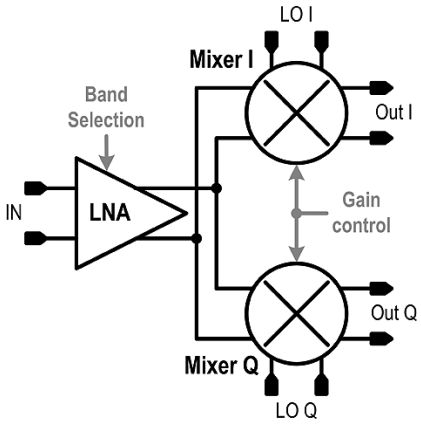

Fig. 5. Block diagram of the variable gain multiband front-end.

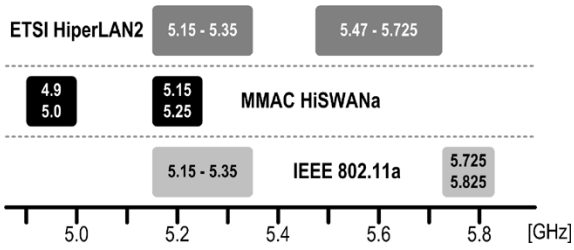

Fig. 6. WLAN scenario in the 5–6 GHz frequency range.

A. Multiband Feedback LNA

The chosen technology is amenable for a high level of integration, suggesting a differential implementation to improve common mode rejection of large signals coupled from digital section through the substrate. The schematic of the LNA is drawn in Fig. 7. The feedback network is realized by means of a capacitive divider, and $\alpha = C_1/(C_1 + C_2)$. Capacitance C_1 is chosen to maximize its impedance with respect to the load impedance, at resonance frequency. A limit to choosing a low C_1 value is the collector-base capacitance of the transistor which has to be a small fraction of the total feedback capacitance. Once C_1 is set, C_2 is determined by means of (3) to meet the input matching condition.

In this design C_1 and C_2 are 100 fF and 1.1 pF, respectively. The current source of Fig. 1 realizes a high impedance in presence of an injected signal. In the actual implementation, high quality, 15 nH surface mount inductors ($L_{\rm SMD}$) are used instead. The 6 mA LNA quiescent current is set and controlled in feedback. The biasing network is drawn in gray in Fig. 7.

As discussed, the multiband features of the amplifier are determined by the multiband properties of the LNA load. An electronically programmable resonance frequency *LC* load is realized by means of a differential inductor ($L_{\rm load}$) in parallel with a bank of three switched capacitors, binary weighted. The eight possible switch configurations select the eight different bands to cover the whole frequency range of interest. A low resistance of the switch, when on, is required not to degrade the load quality factor, while in the off-state the switch is required to realize a minimum capacitance. Actually, a tradeoff between the on resistance and drain-to-bulk parasitic capacitance exists in a classic

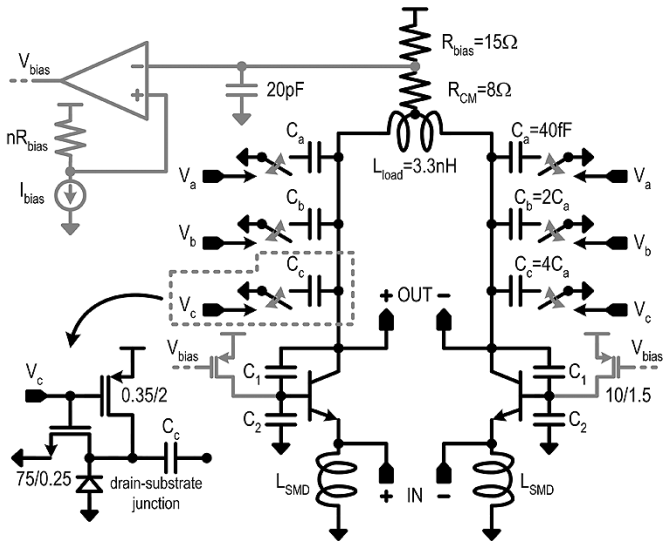

Fig. 7. Schematic of the feedback LNA.

single-MOS device implementation. To minimize, for given resistance, the parasitic capacitance we have chosen an NMOS and a PMOS device connected in series, as shown in Fig. 7. The PMOS is a 0.35 μm/2 μm aspect ratio device, a small fraction of the NMOS one (75 μm/0.25 μm) and serves the purpose of providing a path to $V_{\rm dd}$ when the switch is off. In this way, the NMOS drain-to-bulk parasitic diode capacitance can be reduced by a factor of 2 due to the larger applied reverse voltage.

To improve the common mode rejection, the $R_{\rm CM}$ resistor reduces the load quality factor for common mode signals while not affecting differential signals.

Simulations provide the following: 23 gain, 1.6 dB NF, 0 dBm IIP3, and 30 dB CMRR, roughly constant in each band. To keep the noise figure of the quadrature demodulator particularly low ($\sim$ 2 dB), a quite high gain has been selected making the output stage the primary limit to the LNA IIP3.

B. Variable Gain Mixer

Besides low noise, WLAN standards ask for highly linear RF front-ends. This makes also the mixer design challenging. A front-end IIP3 higher than -12 dBm is required [21]. Given the LNA gain, this requirement translates in a $+11$ dBm mixer IIP3. As shown in Fig. 8, a CMOS pseudo-differential transconductor ($W/L = 50$ μm/0.25 μm) is preferred over a bipolar solution because of the MOS devices higher linearity. The low transconductance gain (11.7 mS with 5 mA biasing current) requires a low noise switching stage, making bipolar devices preferable due to the lower noise. The transconductance stage shows a trade-off between noise and linearity. Nonetheless, increasing the biasing current improves both parameters, though at the expense of current consumption. A high biasing current in the switching stage is not as beneficial because, though increasing the stage IIP3 [22], it also increases the noise contribution [23]. For this reason, we run the two stages at different current levels. In particular, a PMOS current boosting stage is introduced to allow a lower biasing current in the switching pairs. Moreover, the inductor $L_{\rm quad}$, resonating with the parasitic capacitance at

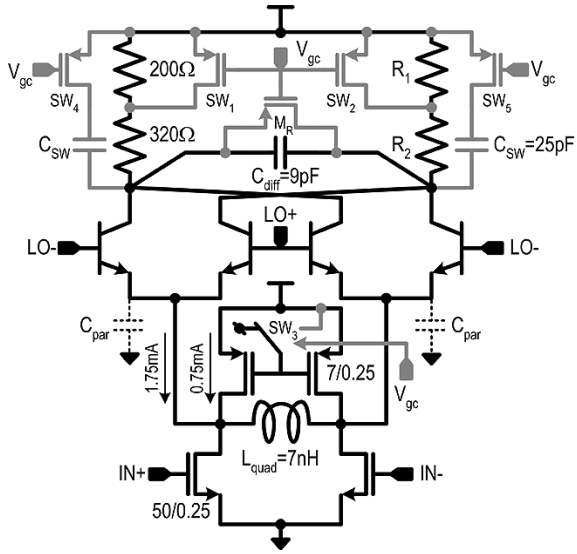

Fig. 8. Variable gain mixer schematic.

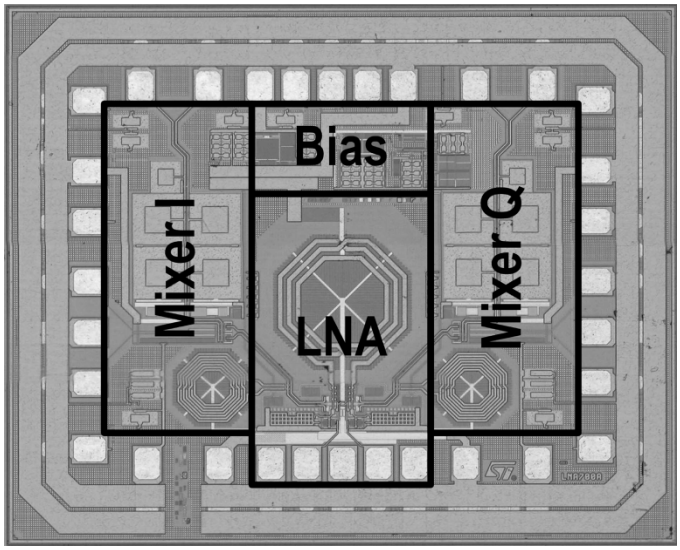

Fig. 9. Die micrograph.

the common source nodes ($C_{\rm par}$) at local oscillator (LO) fundamental frequency, reduces the switching pairs third-order nonlinearities [22]. The resulting IIP3 increase is more than 3 dB. In addition, the switching devices noise contribution is lowered (by about 10% from simulations), due to the high impedance at RF frequency [24]. A resistive load minimizes the flicker noise contribution. The output capacitance $C_{\rm diff}$, together with load resistors, realizes a 12 MHz low-pass transfer function. Simulations provide 8.5 dB gain, 2.6 nV/$\sqrt{\rm Hz}$ equivalent input referred noise voltage spectral density and $+14$ dBm IIP3.

As shown in gray in Fig. 8, a variable gain feature is realized in the mixer. The variable gain control node V_{gc} is connected to five switches and drives a variable resistor, operating as follows:

- Switch $\rm SW_1$ and $\rm SW_2$ together with transistor $\rm M_R$ biased in linear region reduce the output resistive load decreasing the gain by 11 dB. To maintain the output pole cut off frequency at 12 MHz, the capacitors $C_{\rm SW}$ are connected to the mixer output nodes to compensate the resistance reduction.
- To keep the dc output voltage at the same level in both gain configurations, the increase in the output current in low-gain mode is balanced by the resistance reduction from $R_1 + R_2$ to R_2.
- The PMOS current boosting stage is turned off, all the available biasing current flows in the switching pairs, increasing the downconverter IIP3 by 3.5 dB.

In low gain conditions simulations show -2.5 dB gain, 3.2 nV/$\sqrt{\rm Hz}$ equivalent input referred noise voltage spectral density, and $+17.5$ dBm IIP3. In both gain configurations the current consumption is 5 mA and the LO power is 0 dBm (referred to 50 Ω).

IV. Experimental Results

The front-end has been fabricated by STMicroelectronics (BiCMOS7G technology). Test chips are housed in a 36-pin QFN plastic package and soldered on dedicated double side RF boards, realized in a ROGERS4003 0.020-inch-thick substrate ($\varepsilon_{\rm r} = 3.38$, $\tan\delta = 0.027$). External 180° hybrid couplers (30057 Anaren) are used for RF input and LO signals to provide the single-ended-to-differential conversion. 50 Ω strip lines, optimized by means of EM simulations, lead the differential signals from the SMD connectors to the package inputs.

Fig. 9 shows the die micrograph. The RF inputs are at the bottom of the device while the quadrature LO signals are 90° shifted with respect to RF and symmetrically provided. All the inductors are integrated spirals. Patterned ground shields are used to increase their quality factor. To minimize common-mode signals, induced by parasitic bondwire inductances, multiple pads are dedicated to ground and $V_{\rm dd}$ connections. Moreover, large on-chip bypass capacitors freeze the supply voltage to ground. The die area, including bond pads, is 1.6 mm^2, with the core cell occupying only 0.85 mm^2. Notice that the chosen LNA, requiring less inductors than the inductively degenerated counterpart, saves area. All the pads are ± 2 kV Human Body Model (HBM) electrostatic discharge (ESD) protected.

The input reflection coefficients have been tested by means of an Anritsu 37347C vector network analyzer, and Fig. 10 reports the measured S11. The eight curves are obtained by all the different combination of the switches. The front-end input is well matched to the 50 Ω driving source between 4.6 and 5.9 GHz, i.e., the IEEE 802.11a, HiperLAN2, and HiSWANa bands are covered with wide margins. Fig. 11 shows the measured gain as function of the RF input frequency, with an LO frequency 500 kHz apart. The LO power is 0 dBm. Input matching and gain alignment is very good. Finely slicing the overall band allows keeping the receiver gain high. In this case, it is constant at 31.5 dB in each band. When the variable gain control is activated the gain reduction is 11 dB. Fig. 12 reports the front-end frequency transfer function in both gain modes, for the third (out of the eight) band. Gain measurements demonstrate an optimum agreement with simulation predictions.

Fig. 13 shows the output band in the two modes of operation. There is a difference in the output pole frequencies. In particular, in high gain mode, the pole is located at 10.5 MHz instead

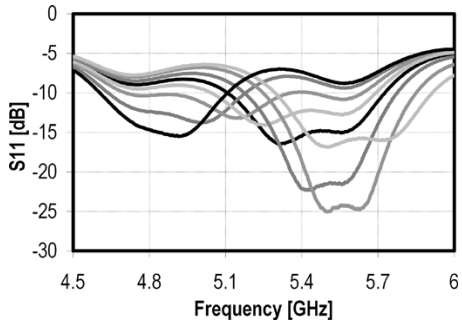

Fig. 10. Measured input matching coefficient versus frequency in all eight switch configurations.

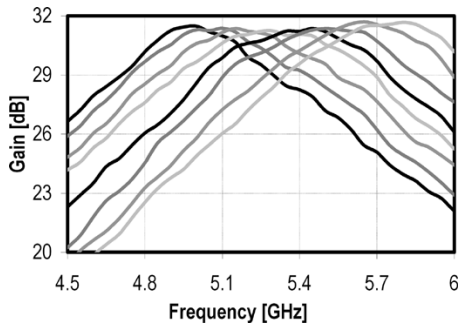

Fig. 11. Measured front-end gain versus input frequency with 500 kHz output frequency offset in all eight LNA configurations.

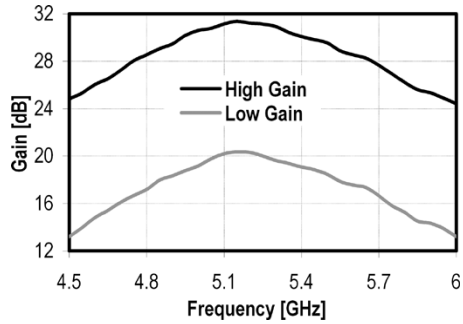

Fig. 12. Measured front-end transfer function versus input frequency with 500 kHz output frequency offset in high and low gain mode (in the third band).

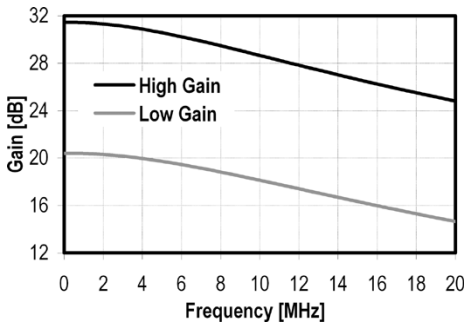

Fig. 13. Measured output band in high and low gain mode.

of 12 MHz. Being the in-band gain exactly as simulated, this difference is attributed to a capacitance C_{diff} higher than designed. The output dc voltage differs by less than 30 mV between the two gain modes.

The I and Q accuracy is verified on the downconverted output signals in the two paths, in all the eight bands and in both gain modes. The maximum measured gain mismatch is lower than 0.3 dB.

Noise figure is evaluated by means of an HP346B noise source. At receiver output a high-speed low-distortion differential line amplifier (MAX4146) converts the differential I and Q mixer output to single-ended signal, drives the 50 Ω input instrument, and raises the front-end output noise enabling measurements on HP8564E spectrum analyzer. The noise figure is evaluated in each band and the maximum value is 2.5 dB. A minimum 2.3 dB value is measured, but 0.2 dB are considered within the measurement setup error. In minimum gain condition, the NF raises to 2.9 dB.

Third-order inter-modulation distortion is evaluated injecting two tones at 20 MHz and 40.5 MHz offset from the LO frequency. The resulting IIP3 is −9.5 dBm in high gain mode and −6 dBm in low gain mode. These values are almost constant in all the 8 bands. The front-end minima IIP2, determined applying two tones at 40 MHz and 40.5 MHz from LO frequency, are +23 dBm and +31 dBm in high and low gain mode, respectively. The chip draws 16 mA from 2.5-V voltage supply. Table I summarizes the front-end measured results.

TABLE I
FRONT-END PERFORMANCE SUMMARY

	High gain mode	Low gain mode
Voltage Gain [dB]	31.5	20.5
NF [dB]	2.5	2.9
IIP3 [dBm]	-9.5	-6
IIP2 [dBm]	23	31
I&Q Matching [dB]	0.3	
Voltage Supply [V]	2.5	
Current [mA]	16	
Die Area [mm^2]	1.6	
Technology	0.25μm SiGe BiCMOS	

V. CONCLUSION

The feasibility of a feedback-based low noise amplifier able to operate up to multiple GHz has been demonstrated. Multiband operations are achieved by simply switching the LNA load, since the peak gain and input matching frequencies are aligned. Moreover, when compared to the widely used inductively degenerated LNA, the adopted topology shows a higher dynamic range for the same power consumption. In this work, WLAN standards in the 5–6 GHz range have been targeted but extension to 2.4 GHz portion is straightforward. Furthermore, the proposed solution looks attractive for the growing wireless ultra-wideband (UWB) technology [27] where several adjacent, equally spaced bands, in the 3–10 GHz range, accommodate

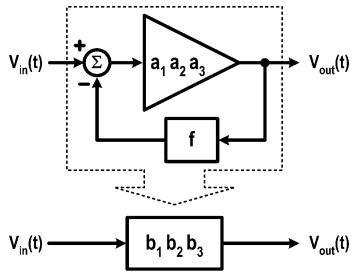

Fig. 14. Effect of negative feedback on an amplifier transfer function.

the signal and minimization of costly, area hungry integrated *LC* filters is mandatory.

APPENDIX

Referring to the block diagram of Fig. 14, the relations between the input-output power series coefficients in open loop ($a_{\rm i}$) and closed loop ($b_{\rm i}$) configuration are given by [25]

$$\begin{cases} b_1 = \frac{a_1}{1+a_1 f} \\ b_2 = \frac{a_2}{(1+a_1 f)^3} \\ b_3 = \frac{a_3 \cdot (1+a_1 f) - 2a_2^2 f}{(1+a_1 f)^5} \end{cases} \tag{A1}$$

in which f is the feedback factor.

To determine $\mathrm{IIP3_{OL}}$ we observe that a local feedback, due to the degeneration resistor R_S, exists around the transistor and the loop gain is given by $g_m R_S$ [26]. The coefficients of the I-V exponential characteristic of the bipolar device are

$$\begin{cases} a_1 = \frac{I_C}{V_T} = g_m \\ a_2 = \frac{1}{2} \cdot \frac{I_C}{V_T^2} = \frac{1}{2V_T} \cdot g_m \\ a_3 = \frac{1}{6} \cdot \frac{I_C}{V_T^3} = \frac{1}{6V_T^2} \cdot g_m \end{cases} \tag{A2}$$

and, according to (A1)

$$\begin{cases} b_1 = \frac{g_m}{1+g_m R_S} \\ b_2 = \frac{1}{2} \cdot \frac{g_m}{(1+g_m R_S)^3} \\ b_3 = \frac{g_m}{6V_T^2} \cdot \frac{1-2g_m R_S}{(1+g_m R_S)^5}. \end{cases} \tag{A3}$$

Reminding that

$$\mathrm{IIP3} = \frac{2}{3} \cdot \left| \frac{b_1}{b_3} \right| \cdot \frac{1}{R_S} \tag{A4}$$

equation (8) follows.

Equation (A3) also represent the input–output coefficients of the forward block of the voltage–voltage feedback LNA. Considering that the loop gain at resonance is $a_1 f = (\alpha \cdot g_m R_p)/(1 + g_m R_S)$

$$\begin{cases} b_1 = \frac{1}{2R_S} \\ b_2 = \frac{1}{16 V_T g_m^2 R_S^3} \\ b_3 = \frac{g_m \cdot \left(3 - 4g_m^2 R_S^2 - g_m R_S\right)}{6V_T^2 (1+g_m R_S)(2g_m R_S)^5} \end{cases} \tag{A5}$$

where we have substituted $R_S = 1/g_m + \alpha \cdot R_p$.

From (A5), (9) follows.

ACKNOWLEDGMENT

The authors would like to thank D. Arrigo, F. Torrisi, M. Paparo (STMicroelectronics), and R. Castello (Università di Pavia) for fruitful discussions and valuable suggestions, and M. Bonaventura and R. Sciuto (STMicroelectronics) for technology access and layout.

REFERENCES

[1] J. Ryynanen, K. Kivekas, J. Jussila, L. Sumanen, A. Parssinen, and K. Halonen, "A single-chip multimode receiver for GSM900, DCS1800, PCS1900, and WCDMA," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp. 594–602, Apr. 2003.

[2] M. Hotti, J. Kaukovuori, J. Ryynanen, K. Kivekas, J. Jussila, and K. Halonen, "A direct conversion RF front-end for 2-GHz WCDMA and 5.8-GHz WLAN applications," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2003, pp. 45–48.

[3] E. Duvivier, G. Puccio, S. Cipriani, L. Carpineto, P. Cusinato, B. Bisanti, F. Galant, F. Chalet, F. Coppola, S. Cercelaru, N. Vallespin, J. C. Jiguet, and G. Sirna, "A fully integrated zero-IF transceiver for GSM-GPRS quad-band application," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2249–2257, Dec. 2003.

[4] S. Wu and B. Razavi, "A 900-MHz/1.8-GHz CMOS receiver for dual-band applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2178–2185, Dec. 1998.

[5] V. Aparin, P. Gazzerro, J. Zhou, B. Sun, S. Szabo, E. Zeisel, T. Segoria, S. Ciccarelli, C. Persico, C. Narathong, and R. Sridhara, "A highly-integrated tri-band/quad-mode SiGe BiCMOS RF-to-baseband receiver for wireless CDMA/WCDMA/AMPS applications with GPS capability," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 1, Feb. 2002, pp. 234–235.

[6] R. Magoon, A. Molnar, J. Zachan, G. Hatcher, and W. Rhee, "A single-chip quad-band (850/900/1800/1900 MHz) direct conversion GSM/GPRS RF transceiver with integrated VCO's and fractional-n synthesizer," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1710–1720, Dec. 2002.

[7] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[8] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2003.

[9] Adiseno, M. Ismail, and H. Olsson, "A wide-band RF front-end for multi-band multistandard high-linearity low-IF wireless receivers," *IEEE J. Solid-State Circuits*, vol. 37, no. 9, pp. 1162–1168, Sep. 2002.

[10] P. Rossi, A. Liscidini, M. Brandolini, and F. Svelto, "A 2.5 dB NF direct-conversion receiver front-end for HiperLAN2/IEEE802.11a," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 1, Feb. 2004, pp. 102–103.

[11] D. J. Allstot, X. Li, and S. Shekhar, "Design considerations for CMOS low-noise amplifiers," in *Proc. IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, Jun. 2004, pp. 97–100.

[12] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *IEEE Trans. Microwave Theory Tech.*, vol. 50, no. 1, pp. 288–301, Jan. 2002.

[13] G. Girlando and G. Palmisano, "Noise figure and impedance matching in RF cascode amplifiers," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 46, no. 11, pp. 1388–1396, Nov. 1999.

[14] K. L. Fong and R. G. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 548–555, Apr. 1998.

[15] K. L. Fong, "High-frequency analysis of linearity improvement technique of common-emitter transconductance stage using a low-frequency-trap network," *IEEE J. Solid-State Circuits*, vol. 35, no. 8, pp. 1249–1252, Aug. 2000.

[16] V. Aparin and L. E. Larson, "Linearization of monolithic LNA's using low-frequency low-impedance input termination," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2003, pp. 137–140.

[17] A. Liscidini, M. Brandolini, P. Rossi, F. Torrisi, and F. Svelto, "Design methodology of feedback-LNA's for GHz applications," in *Proc. Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sep. 2004.
[18] *Part11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High Speed Physical Layer in the GHz Band*, IEEE Std 802.11a/D7.0-1999.
[19] *Broadband Radio Access Networks (BRAN); HIPERLAN Type 2 Technical Specification; Physical (PHY) Layer*, ETSI, 1999.
[20] *Broadband Mobile Access Communication System (HiSWANa)*, ARIB STD-T70.
[21] I. Vassiliou, K. Vavelidis, T. Georgantas, S. Plevridis, N. Haralabidis, G. Kamoulakos, C. Kapnistis, S. Kavadias, Y. Kokolakis, P. Merakos, J. C. Rudell, A. Yamanaka, S. Bouras, and I. Bouras, "A single-chip digitally calibrated 5.15-5.825-GHz 0.18 μm CMOS transceiver for 802.11a wireless LAN," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2221–2231, Dec. 2003.
[22] M. T. Terrovitis and R. G. Meyer, "Intermodulation distortion in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 35, no. 10, pp. 1461–1473, Oct. 2000.
[23] H. Darabi and A. A. Abidi, "Noise in RF-CMOS mixers: A simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 15–25, Jan. 2000.
[24] H. Sjoland, A. Karimi-Sanjaani, and A. A. Abidi, "A merged CMOS LNA and mixer for WCDMA receiver," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 1045–1050, Jun. 2003.
[25] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits Syst. II: Analog Digit. Signal Process.*, vol. 46, no. 3, pp. 315–325, Mar. 1999.
[26] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed: Wiley.
[27] MultiBand OFDM Physical Layer Proposal, IEEE 802.15-04/0122r4 [Online]. Available: http://www.ieee802.org/15/pub/TG3a.html

Paolo Rossi (S'02) was born in Milan, Italy, in 1975. He received the Laurea degree (*summa cum laude*) and the Ph.D. degree in electrical engineering and computer science from the University of Pavia, Pavia, Italy, in 2000 and 2004, respectively. During his studies, he worked on CMOS and BiCMOS RF front-end circuits for wireless transceivers, with particular focus on the analysis and design of LNAs and mixers for multistandard applications.

He is currently with Maxim Integrated Products (Standard Products Business Unit), Rozzano, Italy.

Antonio Liscidini (S'99) was born in Tirano, Italy, in 1977. He received the Laurea degree (*summa cum laude*) in electrical engineering from the University of Pavia, Pavia, Italy, in 2002, where he is currently working toward the Ph.D. degree.

He was a summer intern at National Semiconductors, Santa Clara, CA, in 2003 studying poly-phase filters and CMOS LNA. His research interests are in the implementations of analog RF front-end in CMOS and BiCMOS technology, with particular focus on the analysis and design of LNAs for multistandard applications.

Massimo Brandolini (S'03) was born in Broni, Italy, in 1977. He received the Laurea degree (*summa cum laude*) in electrical engineering from University of Pavia, Pavia, Italy, in 2002, where he is currently working toward the Ph.D. degree in electrical engineering and computer science.

His major research interests include analog and RF IC design for wireless communications, in CMOS and BiCMOS technologies, with particular focus on RF front-ends for multistandard devices. In 2003, he was with Agere Systems, Allentown, PA, as an internship student, working on the design of a highly integrated CMOS FM transmitter.

Mr. Brandolini is a corecipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2003 Best Paper Award.

Francesco Svelto (S'94–M'98) received the Laurea and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 1991 and 1995, respectively.

From 1996 to 1997, he held a grant from STMicroelectronics to design CMOS RF circuits. In 1997, he was appointed Assistant Professor at the University of Bergamo, Italy, and in 2000, he joined the University of Pavia, where he is an Associate Professor. His current research interests are in the field of RF design and high-frequency integrated circuits for telecommunications.

Dr. Svelto has been a member of the technical program committee of the IEEE Custom Integrated Circuits Conference since 2000 and the Bipolar/BiCMOS Circuits and Technology Meeting (BCTM) since 2003, and the European Solid State Circuits Conference in 2002. He served as Guest Editor of the March 2003 special issue of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, of which he is currently an Associate Editor. He is a corecipient of the IEEE JOURNAL OF SOLID-STATE CIRCUITS 2003 Best Paper Award.