A 0.13 um CMOS Front-End for DCS1800/UMTS/802.11b-g with Multi-band Positive Feedback Low Noise Amplifier

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Abstract

This paper presents a fully-integrated CMOS front-end based on a direct conversion architecture for UMTS/ 802.11b-g and a low-IF at 100kHz for DCS1800. The two key building blocks are a multi-band low noise amplifier that uses positive feedback to improve its gain and a highly linear mixer.

The front-end, integrated in 0.13µm CMOS process, exhibits a minimum noise figure of 5.2dB, a programmable gain that can be varied from 13.5dB to 28.5dB, an IIP3 of more than -7.5dBm and an IIP2 better than 50dBm. The total current consumption is 20mA from a 1.2 V supply.

Keywords: multistandard, reconfigurable, CMOS receiver, LNA, positive feedback, high linearity mixer

Introduction

In the last years, the evolution of wireless communications has motivated a strong interest towards the development of multi-standard mobile terminals [1]. The merging of both cellular and 802.11b-g standards in a reconfigurable CMOS transceiver offers advantages in terms of cost and portability. The ability of sharing the hardware through the use of re-configurability represents one of the most important aspects in the design of this kind of terminal. This is especially important if combined with the possibilities offer by recent developments that have made available multi-band antenna and even tunable SAW filters [2]. In fact simply placing in parallel different independent transceiver chains not only enlarges the die area, but also increases the pin number and consequently the number of external components.

A very high level of hardware sharing is obtain in the solution proposed in Fig. 1, where no RF switches are needed and the number of external components and input pins is minimized. Within this scenario, the low noise amplifier (LNA) design can take two different directions: a wide-band approach capable to receive simultaneously all the different standards, or a re-configurable topology able to select the desired frequency [3], [4]. While a wide-band approach allows also a concurrent reception, a re-configurable topology, preserving frequency selectivity, improves the linearity of the receiver chain.

This paper presents a new topology of multi-band low noise amplifier based on positive feedback. The feedback loop allows an easily re-configurable input matching due to a partial reflection of the load to the input. In addition it provides enhanced current gain improving the receiver noise figure.

Based on this LNA, a zero/low-IF DCS/UMTS/802.11b-g front-end has been developed with the addition of two high dynamic range Gilbert cell mixers to perform the I and Q down-conversion. To the author's knowledge, this is the first CMOS front-end with reconfigurable narrow band input matching for cellular/802.11b-g standards ever reported.

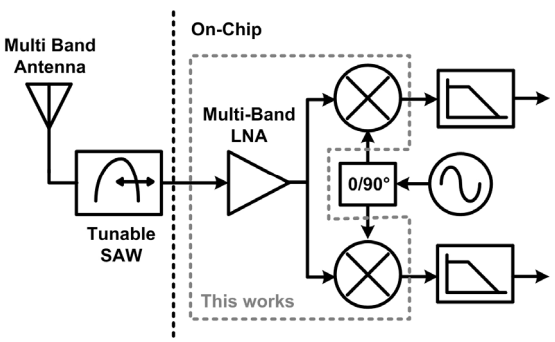

Fig. 1: Zero/Low-IF Multi Standard Front-End

The Positive Feedback Low Noise Amplifier

In the design of multi-band low noise amplifiers, where the input pins are shared for the different standards, the inductance degeneration approach does not appear very suitable. In fact the tuning of its narrow band is generally too noisy because realized at the input, where no signal amplification is present. To solve this problem a negative feedback built around a common base transistor and implemented with a capacitive divider can be used [4]. This correlates the output gain and the impedance matching so that the band of operation can be configured by tuning the load, introducing less noise.

Although such a solution guarantees an easy re-configurability, it suffers from low gain, having a unity current gain and a large parasitic capacitances at the output node due, in part to the kind of feedback network used, that reduce the load impedance at RF. This limitation is more significant when the LNA is implemented in pure CMOS than when a high f_T bipolar transistor is available. In the former case in fact to achieve a sufficient gm the input transistor must be very big which increases the total capacitance at the output node further reducing the achievable RF gain.

To overcome these limitations, the proposed topology uses a positive feedback realized with an active device. This both

produces a current gain greater than one and reduces the capacitive load present at the output of the amplifier (Fig. 2). To explain the basic idea we first consider a single-ended structure. Later-on the fully differential topology, which it the one that was actually integrated in the front-end, will be presented.

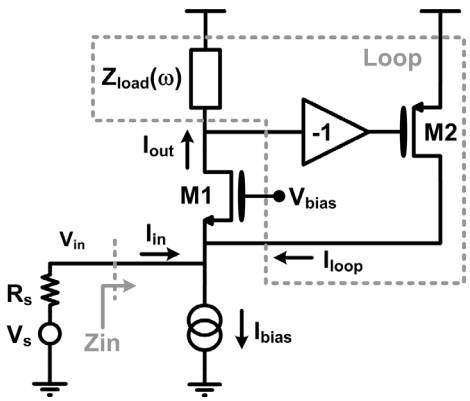

Fig. 2: Shunt-shunt positive feedback

A. Input Matching and Current Gain

In the circuit in Fig. 2 input matching is obtained by the combined effect of the input conductance of M1 and the contribution of the feedback current through M2. When a positive (entering) current I_{in} is injected in the input node, the loop produces a current I_{loop} proportional to I_{in} and in phase with it. This has the effect to increase the input impedance of the common base stage to which the positive feedback is applied as expressed in the following equation:

$$Zin = \frac{1}{gm_1}\frac{1}{(1-gm_2 Z_{load}(\omega))} = \frac{1}{gm_1}\frac{1}{(1-G_{loop})} \qquad (1)$$

where gm_1 and gm_2 are the transconductances of M1 and M2 respectively. The feedback used is positive (shunt-shunt) with a loop gain equal to $gm_2 Z_{load}(\omega)$. If $Z_{load}(\omega)$ is a tuneable LC tank, the input impedance (matching) becomes also tuneable.

The unique characteristics of this topology is that while both the simple common gate stage and the negative feedback common gate stage have a current gain necessarily equal to one, the positive feedback topology has no such a limitation. In fact, as shown in Fig.2, the output current of the LNA (I_{out}) can be expressed as the sum of the input current (I_{in}) and the loop current (I_{loop}) curried by M2, obtaining:

$$\frac{I_{out}}{I_{in}} = \frac{1}{(1-gm_2 Z_{load})} = \frac{1}{(1-G_{loop})} \qquad (2)$$

From (2) it appears that the current gain can be controlled by the loop gain, as was the case for the input impedance. A gain much larger than one can easily be obtained although, to keep a sufficient stability margin, even in worst case conditions, the multiplication factor should not be made too large.

B. Noise Figure

A common gate amplifier generally shows a worse noise figure (NF) compared to one based on a common source configuration. This characteristic is related to the input matching condition, which forces to use an input transconductance equal to 1/Rs. In our case (as for the negative feedback topology) the positive feedback adds a degree of freedom in the choice of the input transconductance producing a noise figure close to that of the inductively degenerated amplifier.

The noise of the new circuit will be computed considering, for simplicity, only the three main noise sources i.e. the thermal noise of the two transistors and the noise of the load. From the transfer functions of all noise sources, the NF can be written as:

$$NF = 1 + \frac{\gamma}{gm_1 R_s} + \gamma gm_2 R_s + \frac{(1+gm_1 R_s)^2}{gm_1^2 R_s Z_{load}} \qquad (3)$$

The second term in the equation represents the contribution of transistor M1 and it has the same expression as for a common gate amplifier. However, in this case, due to the positive feedback, gm_1 can be made larger (less noisy) than 1/Rs. In fact, in matching condition, i.e. Zin=Rs, from (1) follows that $gm_1 = 1/((1- G_{loop})Rs)$.

The third term represents the noise introduced by the feedback. Because transistor M2 injects noise directly at the input, its transconductance has to be minimized to reduce noise. Since, for a given loop gain, i.e. $gm_2 Z_{load}$, reducing gm_2 forces to increase, in a corresponding way, Z_{load} this has also the effect to reduce the noise contributed from the load as shown in the fourth term of (3).

C. Multi-Band Differential Structure

The actual LNA used in the multi-standard front-end receiver is shown in Fig.3.

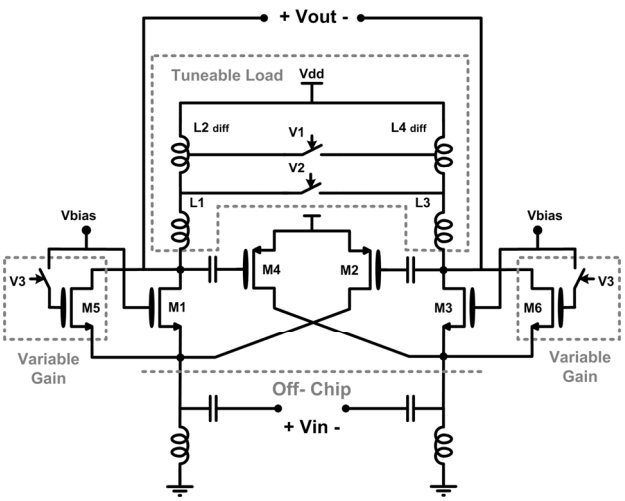

Fig. 3: Differential LNA structure

The positive feedback is easily implemented in a differential structure. In fact using transistors M4-M2 to close the loop around the common gate input stage the sign inversion is obtained by simply crossing their drains. The current source shown in Fig. 1 is implemented through a large inductor (choke) placed off chip. Its value must be high enough to

present a high reactance at the working frequencies in order not to load the input node.

In this topology, the multi-band capabilities comes from the output load that, partially reflected back to the input, produces an input impedance (matching) with the same frequency behavior as the voltage gain. In this case, the load is made-up of an LC tank whose value can be reconfigured through two switches that short-out some sections of the integrated inductors. Tuning the inductance instead of the capacitance is preferred to maintain a high impedance at the resonance frequencies to reduce the noise.

Within the amplifier a variable gain function is also implemented. This is necessary to prevent saturations in the presence of a strong received signal. It is realized by control signal V3 that cuts-off part of the input stage transistors reducing the input transconductance. In addition in the low gain mode, the feedback network is disabled through a control circuit not shown in Fig. 3. In this case to preserve the correct input matching gm_1 (gm_3) is chosen to be equal to 1/Rs.

The Mixer

The schematic of the mixer used in the multi-standard front-end is shown in Fig. 4. The topology is a classical Gilbert's cell where the switching pairs and the load have been folded. Its key features are the possibility of reconfiguration and the introduction of several linearization techniques especially with respect to second order distortion.

The input transconductor, composed of transistors M1-M4, is low frequency degenerated by the current sources M5-M6 for high IIP2 while, at radio frequency, the two capacitors C1 ground the sources, improving IIP3 and noise [5].

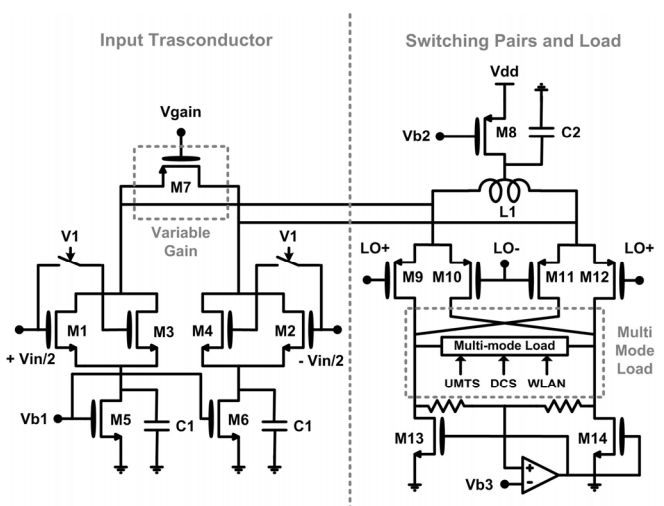

Fig. 4: The high IIP2 Mixer

The different standards considered impose different target in the transconductor design. For example, while DCS1800 requires the lowest noise, UMTS and 802.11b-g need the highest IIP3 tolerating, however, a higher noise [6]. For this reason, the width of the input transistors, and consequently their gm, is made higher in the DCS1800 mode of operation. This is done turning-on switch V1 (Fig. 4).

As in the low noise amplifier, also in the mixer a variable gain feature is implemented. To this end p-MOS transistor M7 is placed in parallel to the switching pairs to divert away from the load, when turned-on, part of the RF current injected by the input transconductor.

The switching pairs are composed by p-channel transistors M9-M10 and M11-M12. An LC filter is inserted between the two common sources both to enhance linearity and to reduce noise [5]. The parasitic capacitors at the switching pairs sources are in fact responsible for performance degradation in terms of noise, second-order and third-order distortion. The differential inductor L1 resonates with the parasitic capacitors, improving switching pair noise and IIP3, while capacitor C2 de-couples the pairs at radio frequency, making the filtering solution effective also for IIP2.

A multi-mode RC load, composed by a bank of differential resistors and capacitors, sets the desired gain and the cut-off frequency at the output node in each mode of operation. Finally, a common-mode feedback loop sets the DC voltage at the output node.

Experimental Results

A prototype version of the font-end was integrated in a standard 0.13 um CMOS technology, and was extensively characterized. The chip, with an active area of 1.5 mm^2, has a power consumption of 24mW (20mW in low gain mode) and is enclosed in a TQFP48 package (Fig. 5).

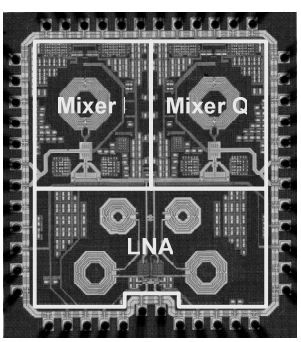

Fig. 5: Die Microphotograph

Fig. 6 and Fig. 7 show the S11 at the input node and the front-end voltage gain respectively for the three different mode of operation in which the front-end can be configured.

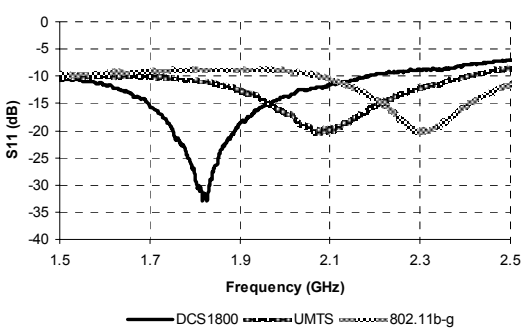

Fig. 6: Input Matching

As expected tuning the amplifier's load has the effect to reconfigure (shift it in frequency) both the gain and the input matching. The curves shown in Fig.7 have been obtained by sweeping (over a frequency range that cover the three bands of interest) both the LO and the frequency of the RF input

signal with a constant offset of 10kHz between them. The peak gain is different in the three configurations to match the specifications of the corresponding standard. In particular the 802.11b-g requires a lowest gain among the three.

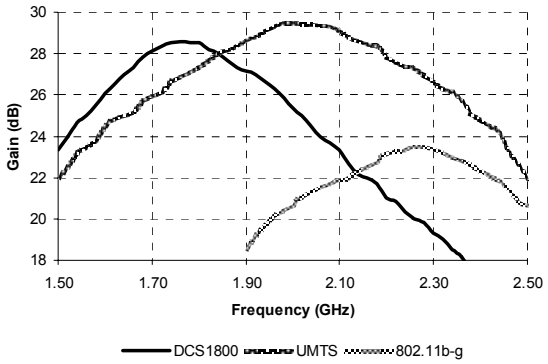

Fig. 7: RF Gain

The in-band frequency response for the three supported standards is reported in Fig. 8 for the case of maximum gain. The correct cut-off frequency for each standard i.e. 550kHz for DCS1800, 4.5MHz for UMTS and 8.6MHz for the 802.11b-g is set programming the mixer load. On the other hand the overall gain can be reduced by 15dB acting on the LNA (6dB) and on the mixer (9dB). In the low gain configuration the LNA power consumption is reduced by 4mW.

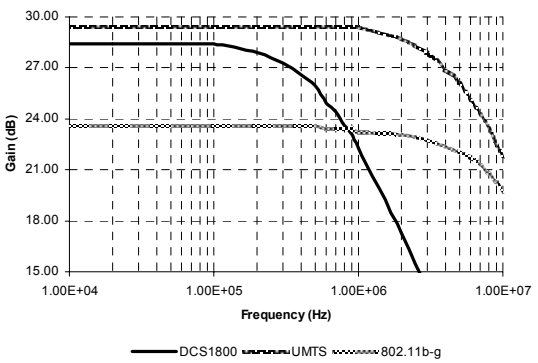

Fig. 8: In-Band Gain

The performances of the receiver are summarized in Table 1. In high gain mode the noise figure is 5.2dB, 5.6dB and 5.8dB for the three standards while the minimum IIP2 and IIP3 are 50dBm and -7.5dBm respectively and corresponds to the DCS1800 case.

The parasitic introduced by the interconnections between the LNA and the mixers due to a not well organized layout degrades the performance of the receiver with respect to simulation. In particular the parasitic capacitance slightly shifts the resonance frequencies of the LNA's tank while the parasitic resistance reduces by over 3dB the LNA gain. This increases the contribution of the mixer to the front-end noise resulting in a degradation of the overall noise figure. To compensate partially this effect, the bias current in the mixer's quads was reduced, exchanging part of the high mixer linearity in favor of a lower noise. Nonetheless, the achieved performances in all settings are comparable to that of state of the art single standard CMOS receivers and still sufficient to satisfy the required specifications. Still a re-layout is presently under way with the intention to recover the original target.

TABLE I
MEASURED FRONT-END PERFORMANCES

	DCS1800	UMTS	802.11b-g
Gain (dB)	13.5 - 28.5	14.5 - 29.5	8.4 - 23.4
Noise Figure (dB)	5.2	5.6	5.8
IIP2 (dBm)	50	51	54
IIP3 (dBm)	-7.5	0	-4.8
Power Dissipation (mW)		20 / 24	
Supply Voltage (V)		1.2	

Conclusion

A CMOS multi-standard front-end receiver based on a positive feedback multi-band LNA and a high linearity mixer has been presented. The LNA has a tunable narrow band input matching. This allows to have a single input for all the standard supported, without renouncing to the frequency selectivity. Moreover the positive feedback improves the gain of the common gate stage resulting in a better noise figure for the overall front end. The use of a high IIP2 and IIP3 mixer allows the implementation of a zero/low-IF architecture that, avoiding the need for an off-chip filter after the LNA, goes towards the goal of a very compact and cheap universal mobile terminal.

Acknowledgement

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