# A 0.13 $\mu$m CMOS Front-End, for DCS1800/UMTS/802.11b-g With Multiband Positive Feedback Low-Noise Amplifier

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***Abstract*—This paper presents a fully integrated CMOS receiver front-end based on a direct conversion architecture for UMTS/802.11b-g and a low-IF architecture at 100 kHz for DCS1800. The two key building blocks are a multiband low-noise amplifier (LNA) that uses positive feedback to improve its gain and a highly linear mixer. The front-end, integrated in a 0.13 $\mu$m CMOS process, exhibits a minimum noise figure of 5.2 dB, a programmable gain that can be varied from 13.5 to 28.5 dB, an IIP3 of more than −7.5 dBm and an IIP2 better than 50 dBm. The total current consumption is 20 mA from a 1.2 V supply.**

***Index Terms*—CMOS, direct conversion, feedback amplifier, high linearity, low-noise amplifier (LNA), mixer, multiband, multistandard, positive feedback, RF receiver.**

## I. Introduction

IN RECENT YEARS, the evolution of wireless communications has motivated a strong interest toward the development of multistandard mobile terminals [1]. In particular, the convergence of cellular and wireless local-area networks (WLANs) is becoming more and more attractive since it offers the possibility of cost savings for the users through the use of WLAN as access points for lower cost wide-area connections. This creates a strong interest toward the merging in a single handheld terminal of both cellular and 802.11b-g standards in a compact and economical way. Within this framework, a natural choice is to use a standard CMOS technology also for the RF front-end as a first step toward a single-chip version of the complete transceiver. Furthermore, the ability of sharing the hardware through the use of reconfigurability represents one of the most important aspects in the design of this kind of terminal, given the potential reduction in the form factor, cost, and power consumption that it can produce. In fact, simply placing in parallel several independent transceiver chains not only enlarges the die area, but also increases the pin count (and consequently the number of external components) and in some cases can also increase the power consumption. The advantages of a single reconfigurable transceiver chain become even more significant when combined with the possibilities offered by recent developments that have made available multiband antennas and even tuneable SAW filters [2].

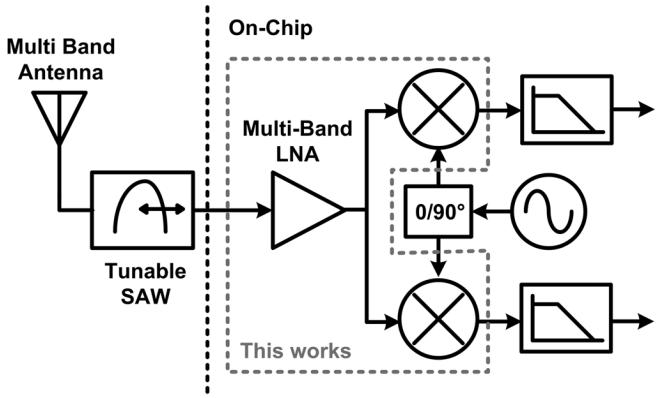


Fig. 1. Proposed compact zero/low-IF multistandard front-end.

Consistently with the above scenario, a very high level of hardware sharing is obtained with the solution proposed in Fig. 1, where no RF switches are needed and the number of external components and input pins is minimized.

Within this architecture, the low-noise amplifier (LNA) design can take two different directions: either a wideband topology capable of simultaneously receiving all the different standards, or a reconfigurable one able to select only the desired frequency [3], [4]. While a wideband approach allows the concurrent reception of more than one signal band, a reconfigurable one, preserving frequency selectivity, improves the immunity of the receiver from out-of-band interferers, although at the cost of allowing only one signal band to be received at one time.

This paper presents a new topology of multiband reconfigurable LNA based on positive feedback. The feedback loop allows to easily reconfigure the frequency interval in which the LNA is matched to the signal source thanks to a partial reflection of the load to the input. In addition, the use of a shunt positive feedback configuration provides enhanced current gain compared with other feedback topologies, thereby improving the overall receiver noise figure.

Based on this LNA, a zero/low-IF DCS/UMTS/802.11b-g front-end has been developed which also includes two high-dynamic-range Gilbert cell mixers that perform the I and Q

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down-conversion. A zero-IF architecture has been chosen for the UMTS and 802.11b-g standards since it results in a overall simplification of the receiver, while a low-IF architecture has been used for DCS primarily to reduce the problem of 1/f noise. To the authors' knowledge, this is the first CMOS front-end with reconfigurable narrowband input matching for cellular/802.11b-g standards ever reported.

The paper is organized as follows. In Section II, the positive feedback topology used in the LNA is first explained in an intuitive way, then its input matching, gain, noise, and linearity characteristics are analyzed in greater detail. In Section III, the multistandard receiver is described, including a detailed description of both the tuneable LNA and the high-linearity mixer. In Section IV, a complete set of experimental measurements carried out on a 0.13 $\mu$m CMOS prototype are reported. Finally, in Section V some conclusions are drawn.

## II. Positive Voltage-Current Feedback

In the design of multiband LNAs, where the input pins are shared among the different standards, the inductance degeneration approach does not appear to be the most suitable. In fact, the tuning of its narrowband matching network is generally too noisy because it is realized at the input, where no signal amplification is present.

On the other end, the common-gate topology seems to be more appropriate for a tuneable or a wideband single-input LNA [4], [5]. The main problem of this solution, however, is the absence of any degree of freedom in the choice of the transistor transconductance that becomes uniquely defined in matching condition. This has the effect of limiting the LNA performance in terms of noise and gain [6].

The introduction of a feedback loop around the input transistor adds a degree of freedom to the design. In the paper by Rossi *et al.* [7], the use of negative feedback around a common-base stage reduces the noise and correlates the input impedance to the LNA load by the use of a capacitive divider. This last characteristic allows easy reconfigurability of the amplifier with very little noise degradation. Although very attractive for reconfigurable applications, this solution suffers from low gain, having both a unity current gain and large parasitic capacitances at the output node (due in part to the kind of feedback network used) that reduces the load impedance at RF. This limitation is more significant when the LNA is implemented in pure CMOS compared to the BiCMOS implementation used by Rossi *et al.* [7] since in the former case the input transistor must be very large to achieve a sufficient $gm$, further increasing the capacitive load seen by the output.

In the circuit presented here, to increase the gain, a current feedback (positive) path (provided by M2) has been inserted in parallel with the input of the common-gate stage, as shown in Fig. 2. In this way, when a current $I_{\rm in}$ is injected in the input node, the loop produces a current $I_{\rm loop}$ proportional to $I_{\rm in}$ and in phase with it. As a consequence, the output current of the amplifier becomes the sum of the current provided by the source and that injected by M2, making the current gain larger than 1.

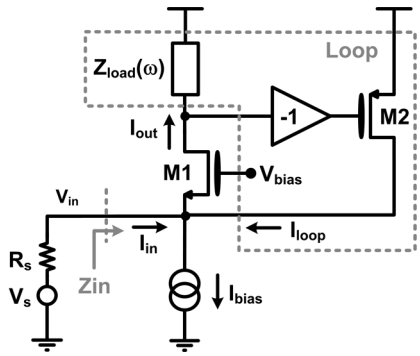


Fig. 2. Diagram of principle of positive feedback LNA.

To explain in more detail the characteristics of the new circuit, a single-ended structure is first utilized. Later, the fully differential topology, which is the one that was actually integrated in the realized prototype, will be presented.

### A. Input Matching and Gain

The shunt–shunt positive feedback provided by M2 has the effect of increasing the input impedance of the pure common-gate stage. Referring to Fig. 2, the feedback theory is used to determine $Z_S(\omega)$, i.e., the impedance seen between the voltage source terminal and ground, which is the sum of the source resistance $R_s$ and the LNA input impedance $Z_{\rm in}(\omega)$. The loop gain and the input impedance of the LNA need to be evaluated considering the effect of the source resistance $R_s$ that, loading the input of the amplifier, introduces a loss in the loop. Starting from the open-loop impedance $Z_{\rm OL} = R_s + 1/gm_1$, the closed-loop impedance will be given by [8]

$$Z_S(\omega) = Z_{OL}\frac{1}{(1 - G_{\rm loop}(\omega))} \tag{1}$$

where

$$G_{\rm loop}(\omega) = \frac{R_s \cdot gm_1}{1 + R_s \cdot gm_1} gm_2 \cdot Z_{\rm load}(\omega) \tag{2}$$

with $gm_1$ and $gm_2$ being the transconductances of M1 and M2, respectively and $Z_{\rm load}(\omega)$ being the LNA load impedance. Inserting (2) in (1) gives the following result:

$$Z_S(\omega) = R_s + \frac{1}{gm_1\,(1 - gm_2 Z_{\rm load}(\omega))} \tag{3}$$

and thus

$$Z_{\rm in}(\omega) = \frac{1}{gm_1\,(1 - gm_2 Z_{\rm load}(\omega))}. \tag{4}$$

If $Z_{\rm load}(\omega)$ is a tuneable LC tank, the input impedance $Z_{\rm in}(\omega)$ becomes also tuneable and purely resistive at the load resonance

frequency $\omega_0$. The LNA can be matched to the source resistance at the frequency $\omega_0$ setting

$$gm_1 = \frac{1}{R_s\left(1 - gm_2 Z_{\text{load}}(\omega_0)\right)} = \frac{1}{R_s(1 - gm_2 R_p)} \quad (5)$$

where $R_p$ is the tank parallel resistance at $\omega_0$. Notice that the application of shunt feedback, which generally is used to decrease the input impedance of a stage, in this case has the effect of increasing it, having chosen a positive feedback type.

The simple common-gate stage and the negative feedback common-gate LNA have a current gain necessarily equal to 1 and thus a transconductance gain (defined as $Gm = i_{\text{out}}/v_s$) equal to $1/(2R_s)$, in matching condition [6], [7]. The positive feedback topology has no such limitation, in fact, its transconductance $Gm$ is

$$Gm = \frac{gm_1}{1 + gm_1 R_s\left(1 - Z_{\text{load}}(\omega) gm_2\right)}. \quad (6)$$

In matching condition, the value of $Gm$ becomes equal to $gm_1/2$, which can be made much larger than $1/(2R_s)$ by choosing a proper value for $gm_1$.

### B. Noise Figure

A common-gate amplifier generally shows a worse noise figure (NF) compared to one based on a common-source configuration [6]. This characteristic is related to the input matching condition, which forces to use an input transconductance equal to $1/R_s$. However, the use of the positive feedback (similarly to the case of using a negative feedback) adds a degree of freedom in the choice of the input transconductance, producing a noise figure close to that of the inductively degenerated amplifier [9].

Referring again to Fig. 2, the noise figure of the circuit will be computed considering, for simplicity, only the three main noise sources, i.e., the thermal noise of the two transistors (M1 and M2) and the noise of the load. Computing the transfer functions from all noise sources to the output node, the following expression for the NF (at the resonance frequency) can be obtained:

$$\text{NF} = 1 + \frac{\gamma}{gm_1 R_s} + \gamma gm_2 R_s + \frac{(1 + gm_1 R_s)^2}{gm_1^2 R_s \cdot R_p} \quad (7)$$

where $\gamma$ is the transistor channel thermal noise factor [6], $R_p$ is the load's impedance at the resonance frequency, and $R_s$ is the source impedance. The second term in the right-hand side of (7) represents the noise contributed by transistor M1 and it has the same expression as for a common-gate amplifier. However, in this case, due to the positive feedback, $gm_1$ can be made larger than $1/R_s$ while still ensuring matching conditions, as explained in the previous section. This results in a lower noise compared with the common-gate case.

The third term represents the noise introduced by the feedback transistor M2. Consistently with the intuition, transistor M2 injects noise directly at the input, its transconductance has to be small to have a low noise. The fourth term in the equation represents the noise contributed by the load. If $gm_1 R_s \gg 1$ this term becomes approximately equal to $R_s/R_p$. Notice that increasing $R_p$ (i.e., increasing the quality factor of the resonant load) reduces the noise contributed by the load but also the noise of M2, since it results in a reduction of $gm_2$ [see (2)].

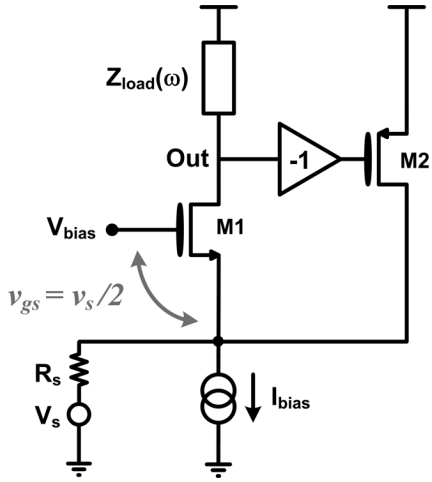


Fig. 3. Effect of the positive feedback on the input transistor $v_{gs}$ modulation.

### C. Linearity

The LNA distortion is influenced mainly by two factors: the additional current path provided by M2 (a nonlinear element) and the effect of positive feedback on both the gate-source voltage swing across M1 and on its DC bias point.

The effect of the nonlinear characteristic of M2 on the voltage-to-current conversion can be considered negligible, provided that the transistor is biased with a large overdrive compared with the signal that modulates its gate; this condition is usually verified even with a low bias current, having to insure that M2 has a sufficiently small transconductance to make its noise contribution negligible as shown by (7).

If the feedback current path is considered linear, the only remaining source of distortion is the voltage-to-current characteristic of the input transistor M1. As shown in Fig. 3, the gate-to-source signal appearing across the input transistor must be equal to $v_s/2$ in order to satisfy the input matching condition; this suggests that the final IIP3 of the amplifier is a function only of the bias point set for M1.

The analytical expression for the amplifier IIP3 can be found starting from Sansen's theory [10] as done by Rossi *et al.* [7]. Considering the transistor in strong inversion [10], the IIP3 for the LNA as a function of the DC overdrive voltage of transistor M1 ($V_{ov}$) becomes

$$\text{IIP3} = \left|\frac{16 V_{ov}^2 (2 + \theta V_{ov})^2}{3 R_s}\right| \quad (8)$$

where $\theta$ approximately models the cumulative effect of source series resistance, mobility degradation due to the vertical field, and velocity saturation [11]. For a minimum channel length device in the 0.13 $\mu$m used technology, $\theta$ was estimated to be 1.6 $\text{V}^{-1}$. Notice that (8) corresponds to the IIP3 expression for

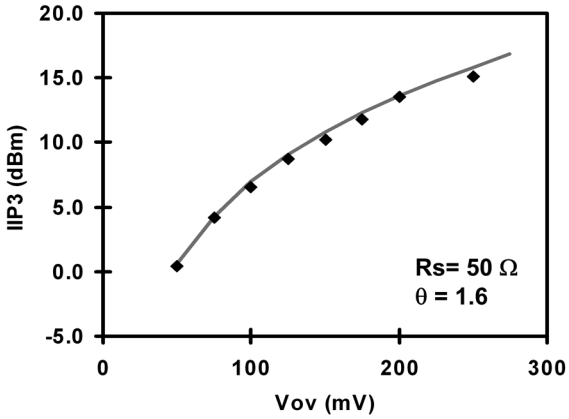


Fig. 4. IIP3 as a function of the input transistor voltage overdrive: equation (7). Simulations (dots) are also reported. ($R_s = 50\ \Omega$, $\theta = 1.5$).

a common-gate LNA. A comparison between theory and simulation is reported in Fig. 4.

Although (8) gives the correct information on the nonlinear behavior of the amplifier, expressing the IIP3 as a function of the DC current flowing in the transistor can be more useful in the design of the amplifier when a constraint in the power consumption is imposed on the design. From the matching condition given in (4) and using the MOS equations [11], the following relationship between the bias current $I_d$, the loop gain and $V_{ov}$ can be derived:

$$V_{ov} \cong I_d R_s (1 - G_{\text{loop}}). \tag{9}$$

Inserting (9) in (8) gives

$$\text{IIP3} \cong \left| \frac{16 R_s}{3} (1 - G_{\text{loop}})^2 I_d^2 \left(2 - \theta R_s I_d (1 - G_{\text{loop}})\right)^2 \right|. \tag{10}$$

Equations (9) and (10) show that, for a given current consumption, increasing the loop gain reduces the overdrive and consequently the linearity. This behavior can be explained considering that increasing the loop gain means also increasing the current gain, and, for a fixed bias current, this produces a larger modulation (in percentage) of the DC bias current of the input device.

## III. Multistandard Receiver Design

The receiver front-end presented is tailored to DCS1800, UMTS, and wireless LAN 802.11b-g standards, and consists of a multiband LNA and two I and Q mixers. A single reconfigurable input for all the standards considered minimizes the number of pins and external components, leading to a very compact solution.

To maximize performance, the direct conversion architecture is used for the standards with a wider bandwidth, such as UMTS and WLAN 802.11.b-g, while for the DCS1800, given its narrower bandwidth, a low-IF (at 100 kHz) architecture is preferred in order to reduce the flicker noise contribution.

### A. Multiband Feedback LNA

The LNA that was implemented in the actual multistandard front-end receiver is shown in Fig. 5. It uses a fully differential structure to improve its rejection to common-mode interferences. In a fully differential architecture, the positive feedback is easily implemented using transistors M4–M2 to close the loop around the common-gate input stage, with the sign inversion being obtained by simply crossing the MOS drains. To keep a safe stability margin, the value of the $gm_2 Z_{\text{load}}$ product at the resonance frequencies is chosen equal to 1/2 which corresponds to a value of 40 mS for $gm_1$.

In the actual circuit, the current source shown in Fig. 2 is implemented by a large inductor (choke) placed off chip. Its value must be high enough to have a high enough reactance at the working frequencies in order not to load the input node.

The multiband capability comes from the fact that the output load is partially reflected back to the input. Hence, the load represents one of the key elements of the LNA design. In this case, a narrowband approach has been chosen, with a tunable LC load that selects alternatively the band of interest. The three different bands (at 1.8, 2.1, and 2.4 GHz) are selected, tuning the inductance instead of the capacitance to maintain high impedance at resonance frequencies in all the configuration in order to reduce the noise as shown by (7). The total capacitance $C$ at the output node limits the maximum value of the load inductance $L$ at 2.4 GHz, thus, increasing the inductance to set the lower frequency configurations avoids the reduction of $R_p$. These arguments neglect the effect of the finite on-resistance of the switches, which tends to degrade the inductor $Q$. However, this effect is very small thanks to the deeply scaled CMOS technology available (0.13 $\mu$m). The tuning is realized by switches controlled by signals V1 and V2 that short out some sections of the integrated inductors (Fig. 5).

Within the amplifier, a variable gain function is also implemented to prevent saturations in the presence of a strong received signal. The LNA gain can be reconfigured by modifying the input transconductance as suggested by (6). The control signal V3, shown in Fig. 5, is used to reduce the input transconductance, switching off part of the input transistors (M5 and M6) (in this way also reducing the current consumption). This tuning operation is realized in such a way that it does not affect the DC voltage overdrive of the input stage, so that the linearity of the amplifier remains approximately equal to that achieved in the high-gain mode, as described by (8). In particular, the lowest possible value corresponds to setting the input transconductance equal to $1/(2R_s)$ and is obtained by opening the feedback loop, thereby operating the LNA as a common-gate amplifier.

### B. High-Linearity Multistandard Mixer

The challenge in the design of the multistandard mixer is due to the extremely critical performance to be satisfied in each mode of operation. Signals belonging to DCS1800 are translated to a low-IF of 100 kHz to significantly reduce the 1/f noise contribution with respect to a direct conversion implementation. Concerning linearity, an IIP2 as high as +70 dBm is needed in the AM suppression test [12], while +7 dBm IIP3 is sufficient. On the other hand, UMTS asks for a higher IIP3 (+10 dBm) and

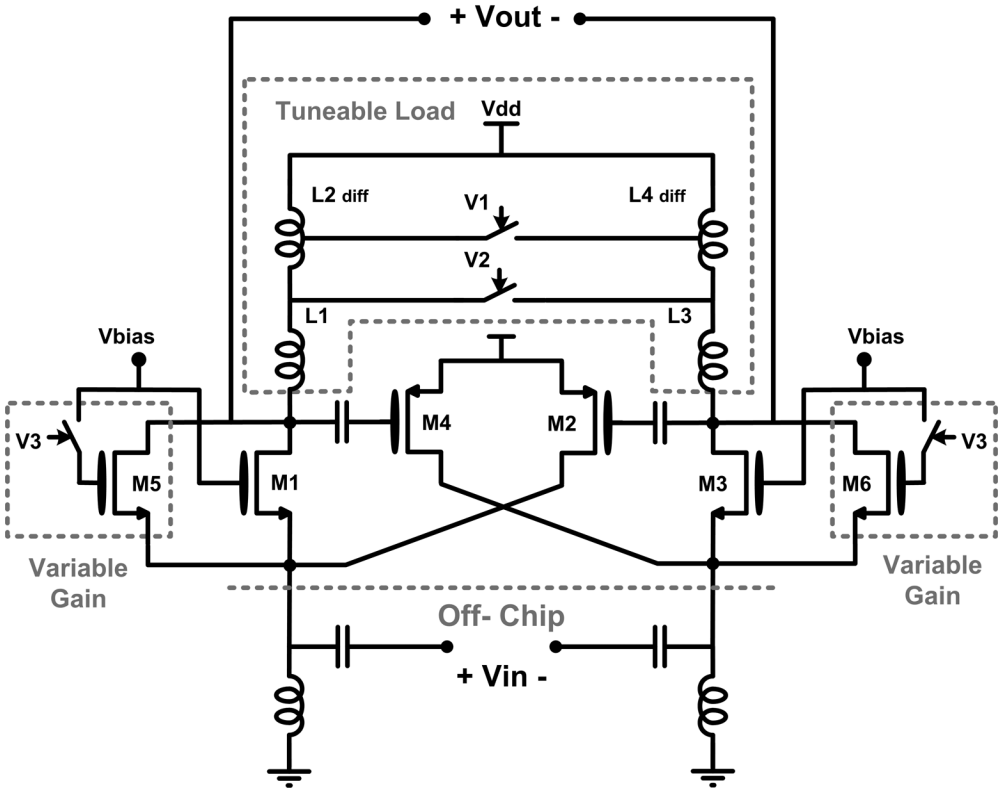


Fig. 5. Fully differential multiband positive feedback LNA.

for an IIP2 similar to that required by the DCS1800 mode of operation. UMTS signals are downconverted to zero-IF, but their wide signal band (1.92 MHz) alleviates the 1/f noise problem. For the mixer, the easiest case is probably found in the IEEE802.11b/g mode. Although the signal bandwidth is very wide due to the multicarrier modulation adopted (OFDM), some care must be used to ensure that the 1/f noise does not significantly affect the signal associated with the first subcarrier. Nonetheless, the noise requirement remains less stringent than for the DCS1800 case. The required IIP3 is in the order of +10 dBm, while +60 dBm IIP2 is sufficient. The starting point for the multistandard downconverter design is the prototype described in a previous work [13], where the tough UMTS requirements were met by means of ad hoc design techniques. Adding a reconfiguration capability to each section of such a down-converter leads to the multistandard circuit drawn in Fig. 6. The input transconductor, composed of transistors M1–M4, is low-frequency degenerated by the current sources M5–M6 for high IIP2, while, at radio frequency, the two capacitors $\mathrm{C_{RF}}$ ground the sources, improving IIP3 and noise. Switches SW1 and SW2 control the RF MOSFET's width, in order to properly adjust the input devices $gm$ and, in turn, the IIP3 and noise performance while maintaining the bias current constant. The highest $gm$ is set in the DCS1800 mode, while in UMTS and IEEE802.11b/g a higher overdrive is chosen to meet the tougher IIP3 requirements. In order to achieve sufficient dynamic range with a 1.2 V supply, the switching pairs have been folded. An LC filter is inserted between the two common sources, both to enhance linearity and to reduce noise [13]. The parasitic capacitors at the switching pair sources are responsible for performance degradation in terms of both noise and linearity. The differential inductor L1 resonates with the parasitic capacitors, improving switching pair noise and IIP3, while capacitor $\mathrm{C_{MID}}$ decouples the pairs at radio frequency, making the filtering solution effective also for IIP2. Notice that the pMOS current source M8 adds only common-mode noise, which is greatly rejected by the differential topology, resulting in a negligible noise penalty. A multimode RC load, composed by a bank of differential resistors and capacitors, sets the desired gain and the cut-off frequency at the output node in each mode of operation. The 15 dB gain required in UMTS mode is lowered to 12 dB in the DCS1800 mode and to 10 dB in the IEEE802.11b/g mode by means of programmable resistors. The 600 kHz pole required by DCS1800 is obtained by means of high density poly-well capacitors. In the other standards, MIM capacitors have been used to exploit their superior linearity. A common-mode feedback loop sets the DC voltage at the output node. As in the LNA, also in the mixer a variable gain feature is implemented to cope with large amplitude signals in each possible standard. To this end, pMOS transistor M7 is placed in parallel to the switching pairs to divert away from the load, when turned on, part of the RF current injected by the input transconductor. A 9 dB gain reduction is sufficient to handle strong signals in each standard. The downconverter is biased at 5 mA current.

## IV. Experimental Results

The front-end has been fabricated in STMicroelectronics standard 0.13 $\mu$m CMOS technology (H9RFCMOS). The chip is encapsulated in a TQFP48 plastic package and soldered on a dedicated double-sided RF board, realized in a ROGERS4003

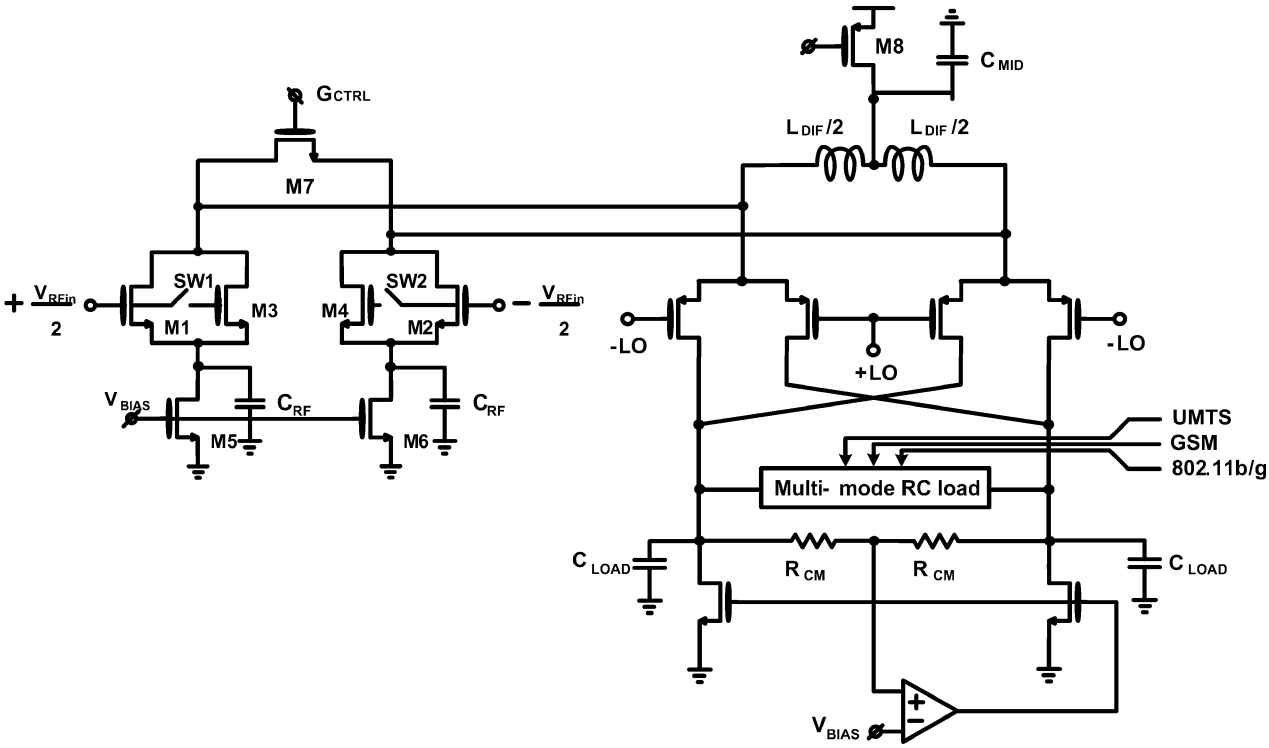


Fig. 6. High-linearity multistandard mixer.

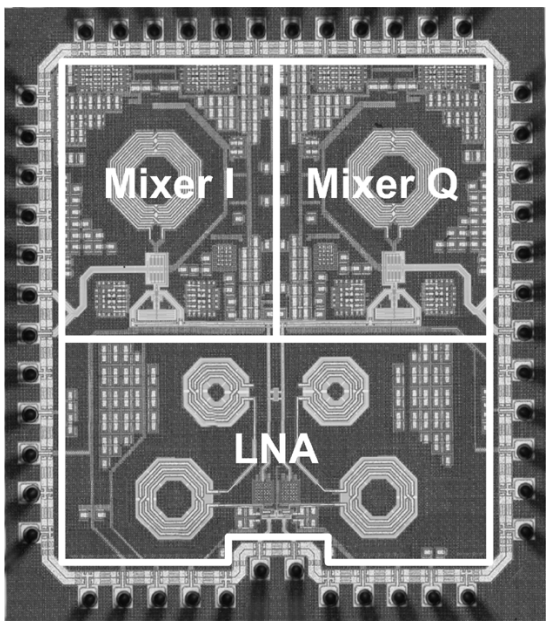


Fig. 7. Die micrograph.

0.020-inch-thick substrate ($\varepsilon r = 3.38, \tan\delta = 0.027$). External 180° hybrid couplers (30057 Anaren) were used both at the RF and at the LO input to implement the single-ended-to-differential conversion. 50 Ω strip lines, optimized by means of EM simulations, carry the differential signals from the SMD connectors to the package inputs.

The die micrograph is reported in Fig. 7. The RF inputs are located at the bottom of the device with the signal lines running vertically, while the quadrature LO signals are placed symmetrically and oriented at 90° with respect to the RF signal lines to reduce coupling among them. All the integrated inductors used are of the spiral type with ground shields to increase their quality factor. To minimize common-mode signals, induced by parasitic bondwire inductances, multiple pads with multiple bonding are used for ground and voltage supply connections. Moreover, large on-chip bypass capacitors are used to filter the noise on the supply voltage with respect to ground. The chip has an active area of only 1.5 mm$^2$ and all the pads used are electrostatic discharge (ESD) protected.

The input reflection coefficient has been tested by means of an Anritsu 37347C vector network analyzer. Fig. 8 and Fig. 9 report the module and the Smith Chart representation of the S11, respectively. The three different bands are obtained acting only on the control signals V1 and V2, without any additional tuning of the external component. From the Smith Chart, it is possible to appreciate the effect of the loop on the input impedance, which increases when gain is developed at the output of the amplifier. As expected, the tuning in frequency of this gain provides a frequency variable input matching. The front-end is well matched for the DCS1800 and UMTS standards band, while a slight shift toward lower frequency appears for the WLAN configuration. This behavior is caused by an inaccurate estimation of the parasitic that has affected both the matching and the gain of the amplifier.

Fig. 10 shows the gains for the three standards as a function of the RF input frequencies, measured while keeping a relative LO frequency offset of 100 kHz. The alignment in frequency between the input matching (Fig. 8) and the gain (Fig. 10) is very good. The gain of the three different configurations can be

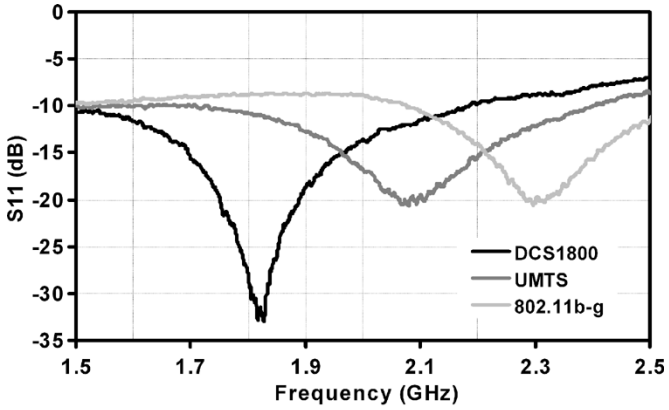


Fig. 8. Measured input matching coefficient S11 versus frequency in all three switch configurations.

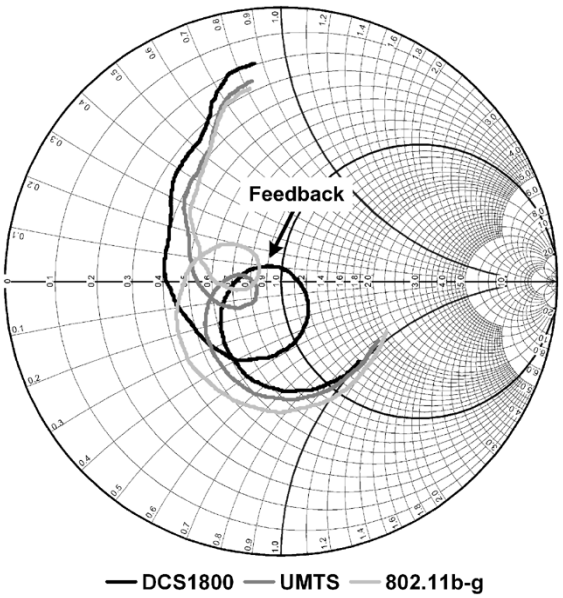


Fig. 9. Measured input matching coefficient S11 over Smith chart in all three switch configurations.

changed to satisfy the specification of each standard, in particular for the UMTS configuration the maximum gain, of 29.5 dB, is obtained. The gain in each band is set acting on the load of the LNA and the mixers. Furthermore, a capacitive divider placed between the amplifier and the mixer reduces the gain for the UMTS and the WLAN standards to relax the linearity specification of the mixer. However, in this condition, to compensate this gain reduction in order to still meet the global gain specs, the mixer reconfigures its output load and its corresponding gain.

The overall in-band gain of the front-end is reported in Fig. 11 for the three standards. The reconfigurable mixer's load provides different output pole frequencies for each standard, i.e., 550 kHz for DCS1800, 4.5 MHz for UMTS, and 8.6 MHz for the 802.11b-g. Independently of the standard chosen, the overall gain can be reduced by 15 dB acting on the LNA (6 dB) and on the mixer (9 dB). Fig. 12 reports gain measurements in the two extreme settings of the variable gain feature for the UMTS standard. In the low-gain configuration the LNA, power consumption is reduced by 4 mW.

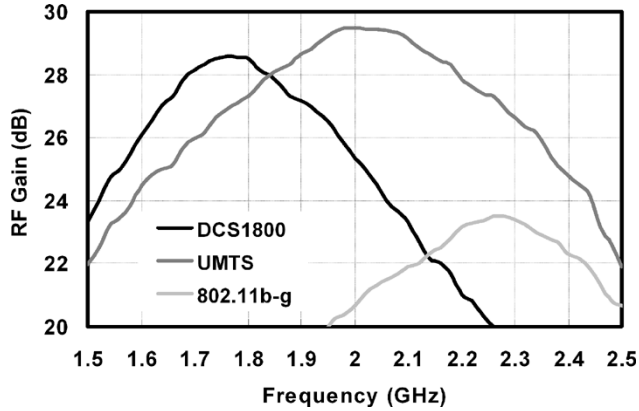


Fig. 10. Measured front-end gain versus input frequency with 100-kHz output frequency offset in all three LNA configurations.

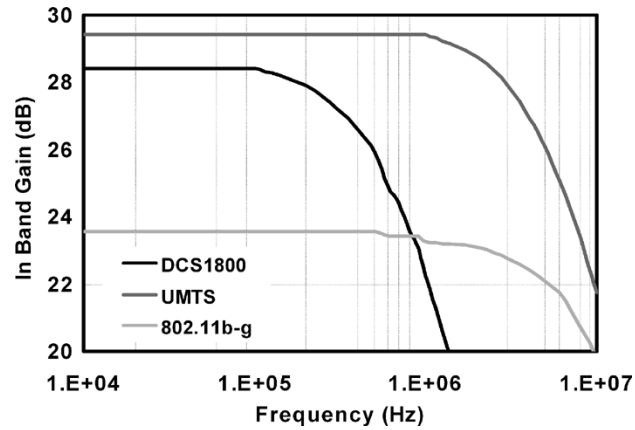


Fig. 11. Measured output band in high-gain mode.

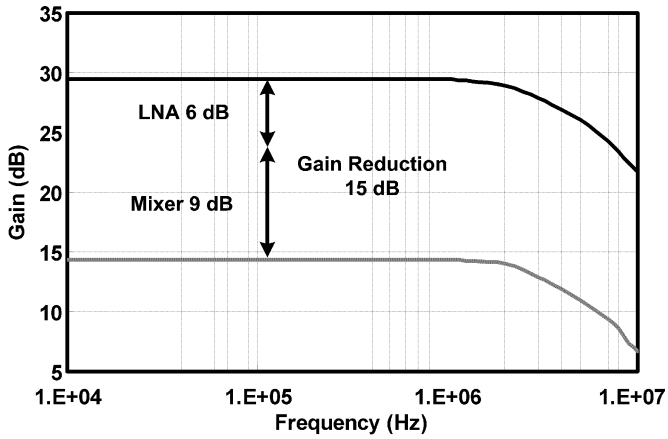


Fig. 12. Variable gain measure for the UMTS mode.

The noise figure was evaluated by means of an HP346B noise source. At the receiver output, a high-speed low-distortion differential amplifier (MAX4146) was used to convert the differential mixer output signal to a single-ended format, drive the measurement equipment's 50 $\Omega$ input ports, and raise the front-end output noise above the sensitivity level of the HP8564E spectrum analyzer that is used to capture its frequency content. The noise figure evaluated in each band gives the following results: 5.2 dB for DCS1800, 5.6 dB for UMTS,

TABLE I
FRONT-END PERFORMANCE SUMMARY

| | DCS1800 | UMTS | 802.11b-g |
|---|---|---|---|
| Gain[dB] | 13.5-28.5 | 14.5-29.5 | 8.4- 23.4 |
| Noise Figure [dB] | 5.2 | 5.6 | 5.8 |
| IIP2 [dBm] | 50 | 51 | 54 |
| IIP3 [dBm] | -7.5 | 0 | -4.8 |
| Power Dissipation [mW] | 20 / 24 | | |
| Supply Voltage [V] | 1.2 | | |
| Die Active Area [$mm^2$] | 1.5 | | |
| Technology | 0.13 μm CMOS | | |

and 5.8 dB for 802.11b-g. Several parasitic effects associated with the interconnections between the LNA and the mixers due to a not-well-organized layout degrades the performance of the receiver with respect to simulation. In particular, the parasitic resistance between the LNA and the mixer reduces by over 3 dB the LNA gain, increasing the input-referred noise contributed by the mixer, degrading the receiver noise figure. Nonetheless, the achieved performance in all settings is still comparable to that of state-of-the-art single-standard CMOS receivers and sufficient to satisfy the required specifications. Still, a relayout has been performed with the intention of recovering the original target specifications.

The third-order inter-modulation distortion was evaluated by injecting two tones at the proper frequencies for each standard, i.e., 800 and 1600 kHz for DCS1800, 130 and 65 MHz for UMTS, and 20 and 40 MHz for 802.11b-g. The three IIP3s obtained are −7.5 dBm, 0 dBm, and −4.8 dBm, respectively. The front-end minima IIP2, using a single tone at the following frequencies: 6 MHz for DCS1800, 130 MHz for UMTS, and 20 MHz for 802.11b-g, are 50 dBm, 51 dBm, and 54 dBm, respectively. All the measurement results are summarized in Table I.

## V. CONCLUSION

A CMOS multistandard front-end receiver based on a positive feedback multiband LNA and a high-linearity mixer has been presented. A new topology narrowband tuneable LNA allows to use a common input for all the standards considered, while preserving frequency selectivity. The use of positive feedback improves the gain compared to all of the other common-gate LNA topologies, resulting in a better noise figure for the overall front-end. Furthermore, the high- linearity mixer allows the implementation of a zero/low-IF architecture that, avoiding the need for an off-chip filter after the LNA, goes toward the goal of a very compact and cheap universal mobile terminal.

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