26.2 A 5.4mW GPS CMOS Quadrature Front-End Based on a Single-Stage LNA-Mixer-VCO

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In the never-ending quest for vanishing power consumption in battery-powered radio ICs, a favored technique is current reuse across different functional blocks. A popular example is cascoding the Gilbert mixer on top of the input stage of the LNA in a receiver front-end, while less frequent is stacking VCO and mixer [1]. A further development takes advantage of the fact that a Gilbert mixer and a differential oscillator resemble each other very closely, since in both cases the differential-pair transistors behave like switches. As it happens, mixer and VCO can be merged into a single block, referred to as the self-oscillating mixer (SOM) [2]. However, if spectral purity demands the use of an LC-tank oscillator, an SOM approach is confronted with the need of handling at the same time the RF carrier and the downconverted signal band, which, in IC realizations, will be at low IF or even at baseband. Therefore, the SOM should provide enough gain at very low frequencies. Unfortunately, the LC-tank presents a negligible impedance for all reasonable IF choices. This difficulty disappears in the stacked LNA-mixer-VCO design (LMV cell, see Fig. 26.2.1) adopted in this work.

The VCO uses the traditional LC-tank topology with M3-M4 implementing the negative resistance. Although the sources of M3 and M4 are separated by the RC mixer load, capacitor C presents a very low impedance at the oscillation frequency, and the VCO works in the same way as if M3-M4 were a traditional common-source pair. The mixing operation is obtained by injecting the RF current signal into the double switching-pair structure made of transistors M1 to M4. The oscillator switches on alternatively M2-M3 and M1-M4, multiplying by +1 and -1 the RF current flowing through the RC load. While the resistance R senses the signal downconverted from RF to IF, the dc current is upconverted to RF and flows through C. Finally, the LNA (implemented by transistor M0) sets the dc bias, performs the V-I conversion, and ensures matching with the input signal source through the use of the well-known inductive degeneration technique.

It is worth remarking that the LMV structure enjoys the key feature of largely separating the different functions therein implemented, i.e. RF amplification, mixing, and LO generation, even while sharing the same bias current and often the same devices. This is possible because each device in the circuit plays a double role, one at RF and one at IF, without introducing conflicts between the two domains. For example, transistor M0 acts as an LNA at RF while providing the dc bias current to the VCO; the pair M3-M4 performs the mixing task over the resistance R at IF while contributing, together with the capacitance C, to the VCO operations at RF. Therefore, several apparently contrasting tasks are successfully merged: current reuse, multiple functionality without spurious interactions, device count reduction, and compatibility with a low supply voltage.

The front-end circuit is drawn in Fig. 26.2.2. The receiver is made of two cross-coupled LMV cells generating the quadrature paths, together with two baseband output buffers and a PLL used to lock the frequency of the oscillator. The current signal at the output of the mixers flows into a low-frequency virtual ground, realized with a super-cascode structure, and is finally collected as a voltage at the output of the buffers. The RF portion of the receiver is therefore operated in the current domain while voltage amplification occurs in the IF portion. Although this choice is not required for the LMV to perform down-conversion, the use of a virtual ground at the mixer outputs reduces the sensitivity to parasitic capacitances between mixer outputs and ground, enabling a more robust control of the conversion gain. Furthermore, moving the whole voltage gain out of the LMV stack reduces the minimum supply voltage required for proper operations. As a consequence, the circuit in Fig. 26.2.2 is fully functional at 1.2V supply. On the other hand, it must be appreciated that the lack of voltage gain in front of the baseband buffers tends to increase the contribution of these stages to the overall NF.

The LMV quadrature scheme is shown in detail in Fig. 26.2.3. Quadrature operation is straightforwardly achieved via the standard cross-coupling of the two VCOs through the additional differential pairs M5-M6 and M5Q-M6Q. This does not interfere with the rest of the LMV and is yet another proof of the robustness and versatility of the cell. It should be noticed that the additional pairs do not significantly affect the total power consumption. This is because the NF of the front end is not appreciably deteriorated even for large departures from ideal LO quadrature, therefore, the bias current in the additional pairs can be set at only 20% of the bias current in the oscillators. Since the LNA acts as a bias current generator to the VCO, its flicker noise can severely impair the close-in phase noise of the VCO; therefore, an additional low-frequency degeneration is added through transistor MB. In this way, dimensions and aspect ratio of the M0 can be chosen for optimum RF performance, avoiding any trade-off with the oscillator design.

The front-end is fabricated in a 0.13μm CMOS process. Figure 26.2.4 shows the chip micrograph. All pads are ESD protected and the active die area is 1.5mm^2. Only three integrated inductors are used, resulting in a modest area occupation. To improve reliability, thick-gate MOS transistors are used in both VCO and mixer, although this is not strictly necessary when the minimum supply voltage (1.2V) is used in the RF part. With standard gate oxide devices, the supply voltage can be lowered to 1.0V. Figure 26.2.5 shows the measured S_{11} for the circuit, displaying a good input matching at the GPS frequency. A plot of the gain at baseband, measured with an LO frequency of 1.6GHz, is shown in Fig. 26.2.6; the gain is as high as 36dB, with a roll-off caused by a dominant pole at 10MHz. The NF integrated over the IF band (3 to 5MHz) is 4.8dB. The IIP3 is –19dBm while the P_{1dB} is –31dBm. The VCO phase noise, measured at the output of the front end, is -104dBc/Hz at 1MHz offset frequency; the phase error between the I and Q paths is lower than 5°, good enough to avoid a deterioration of the overall NF. The quadrature front-end with the output stages draws a total of 4.5mA from 1.2V (this excludes the PLL, not optimized for use in GPS receivers). A summary of the most relevant measurements results is given in Fig. 26.2.7.

Acknowledgments:
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References:
[1] J. van der Tang, D. Kasperkovitz. "A 0.9-2.2GHz Monolithic Quadrature Mixer Oscillator for Direct-Conversion Satellite Receivers," *ISSCC Dig. Tech. Papers*, pp. 88-89, Feb., 1997.
[2] M. Ghanevati, A. S. Daryoush."A Low-Power-Consuming SOM for Wireless Communications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 47, no. 7, pp. 1348-1351, July, 2001.

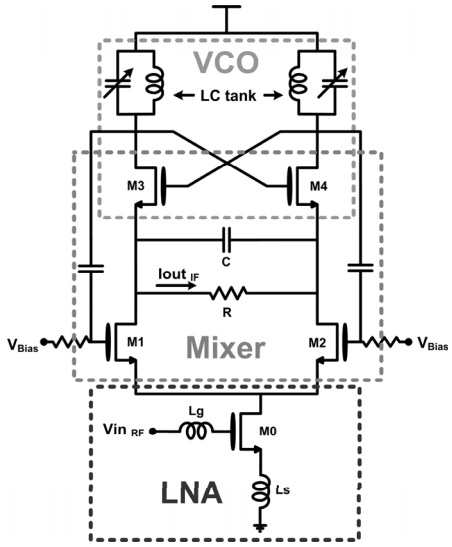


Figure 26.2.1: LNA-mixer-VCO cell.

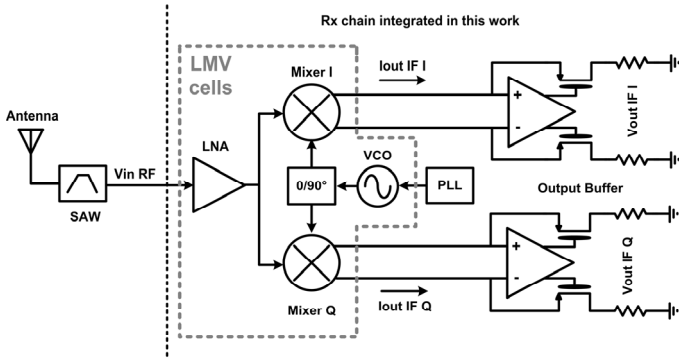


Figure 26.2.2: Quadrature GPS front-end.

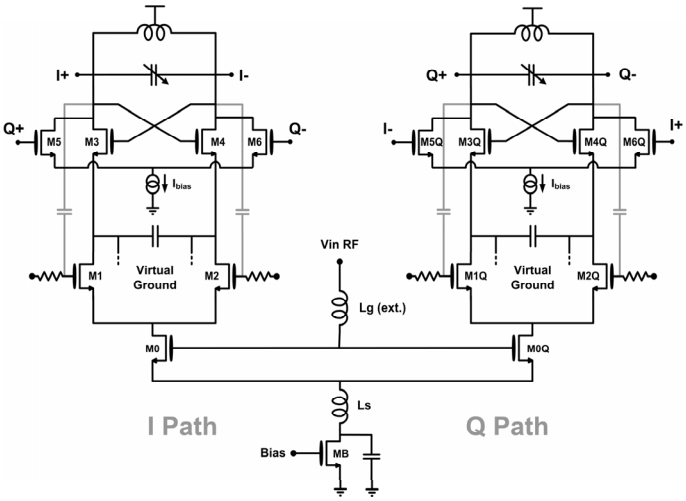


Figure 26.2.3: LMV cells in quadrature.

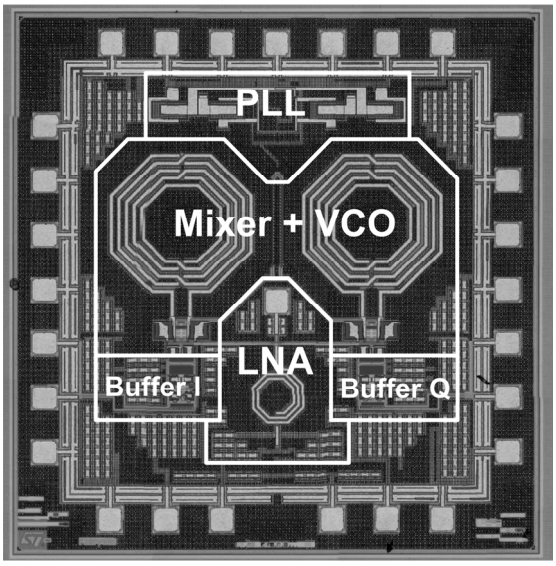


Figure 26.2.4: Chip micrograph.

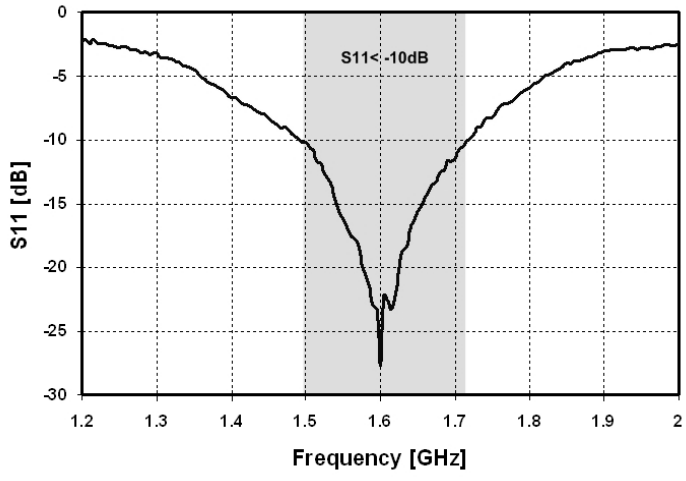


Figure 26.2.5: Input-matching measurement.

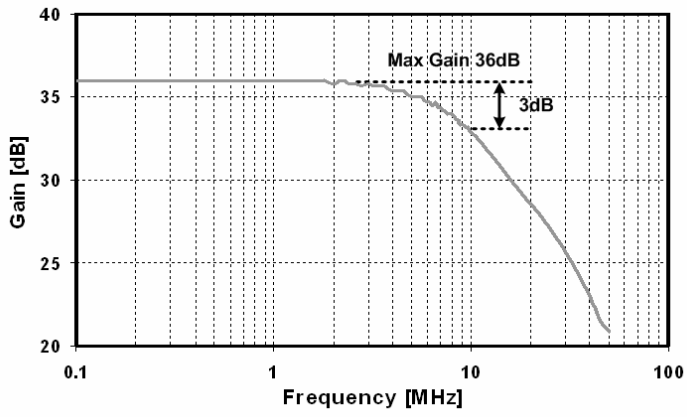
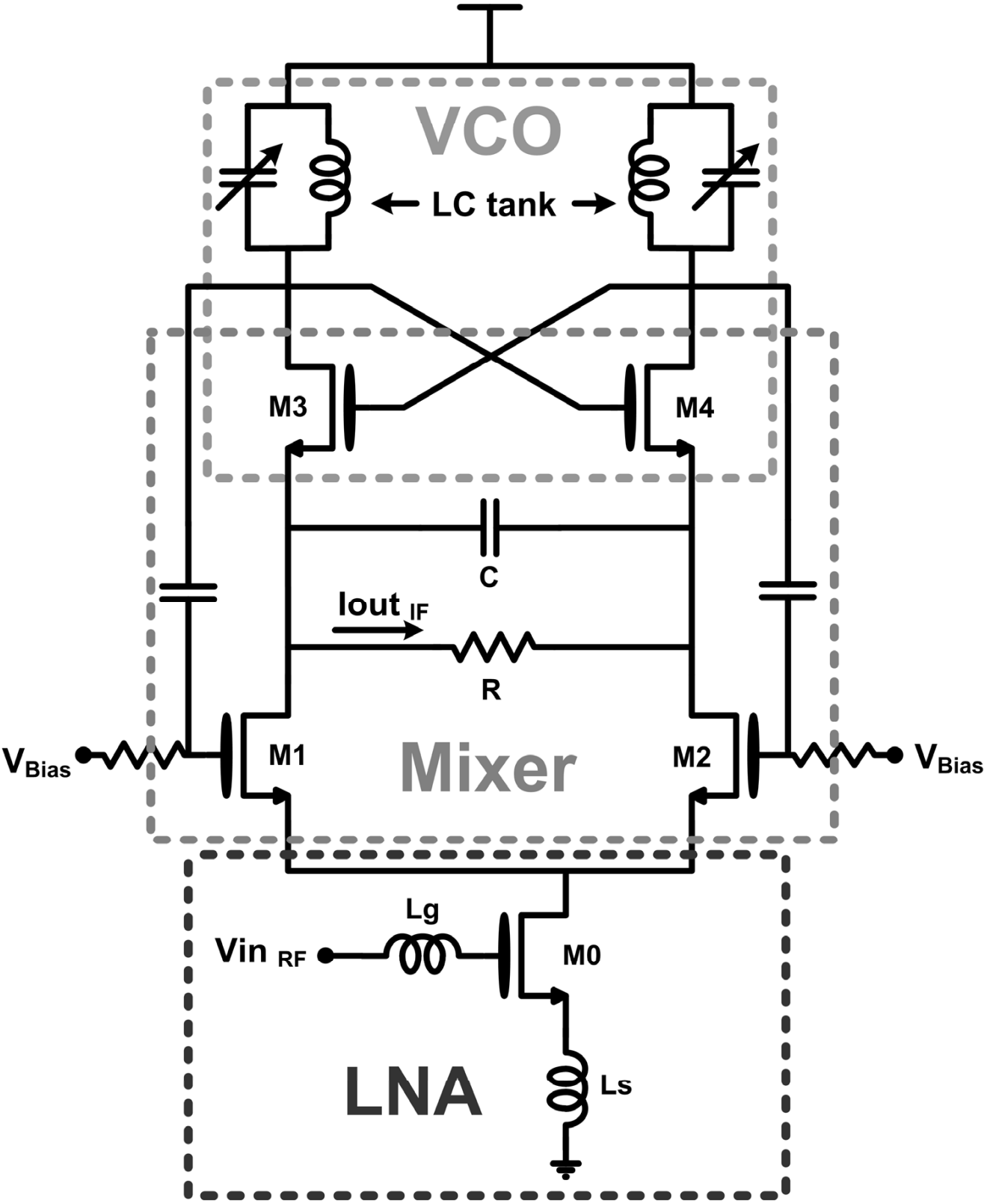


Figure 26.2.6: Output gain.

Gain	36	dB
NF (from 3 to 5MHz)	4.8	dB
IIP3	-19	dBm
P_{1dB}	-31	dBm
S_{11} Matching < -10dB	1.5 - 1.7	GHz
Phase Noise @ 1MHz	-104	dBc/Hz
LO leakage at input	-55	dBm
Current consumption (PLL excluded)	4.5	mA
Supply Voltage	1.2	V

Figure 26.2.7: Measured performance.



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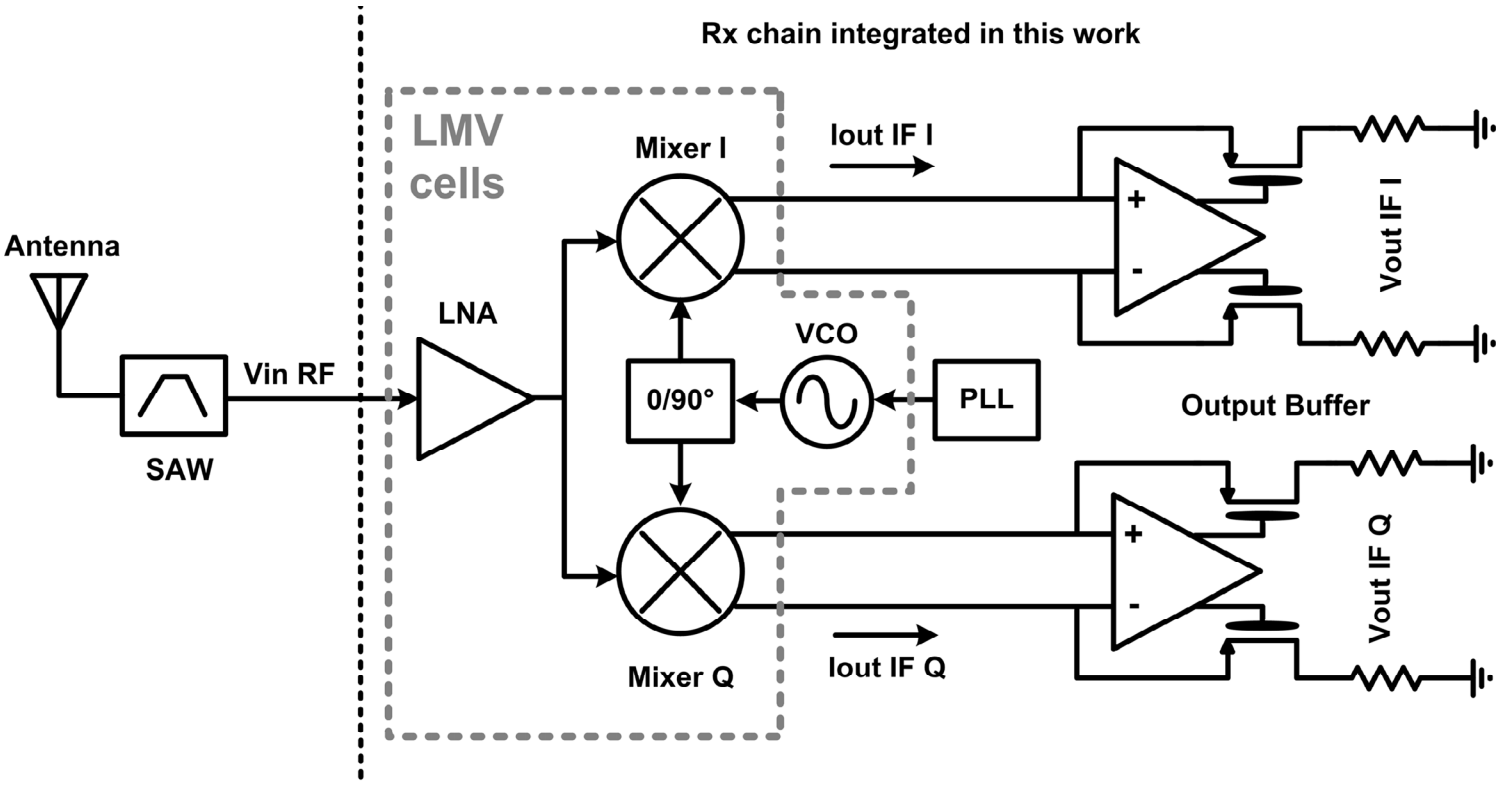


Figure 26.2.2: Quadrature GPS front-end.

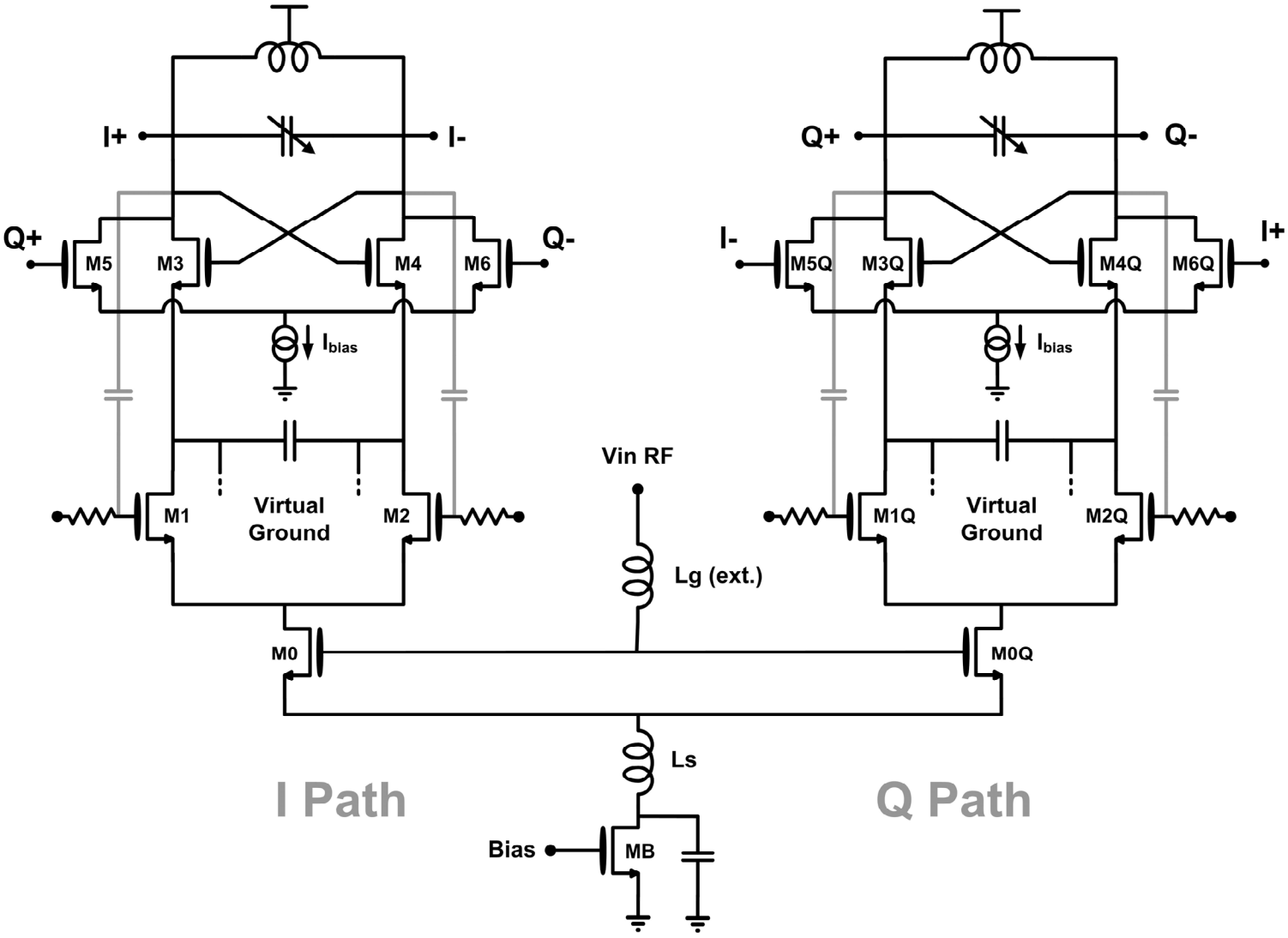
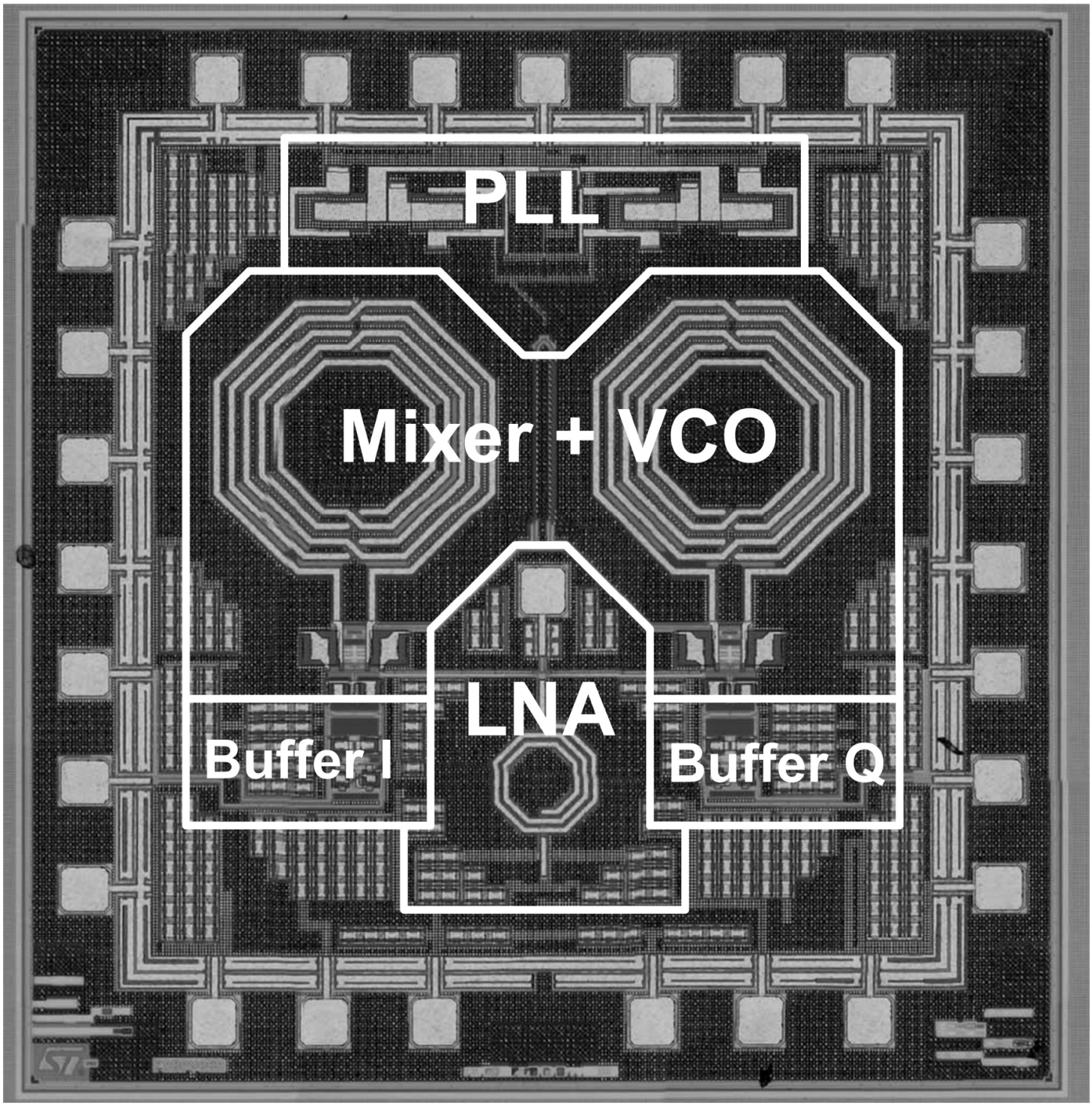


Figure 26.2.3: LMV cells in quadrature.



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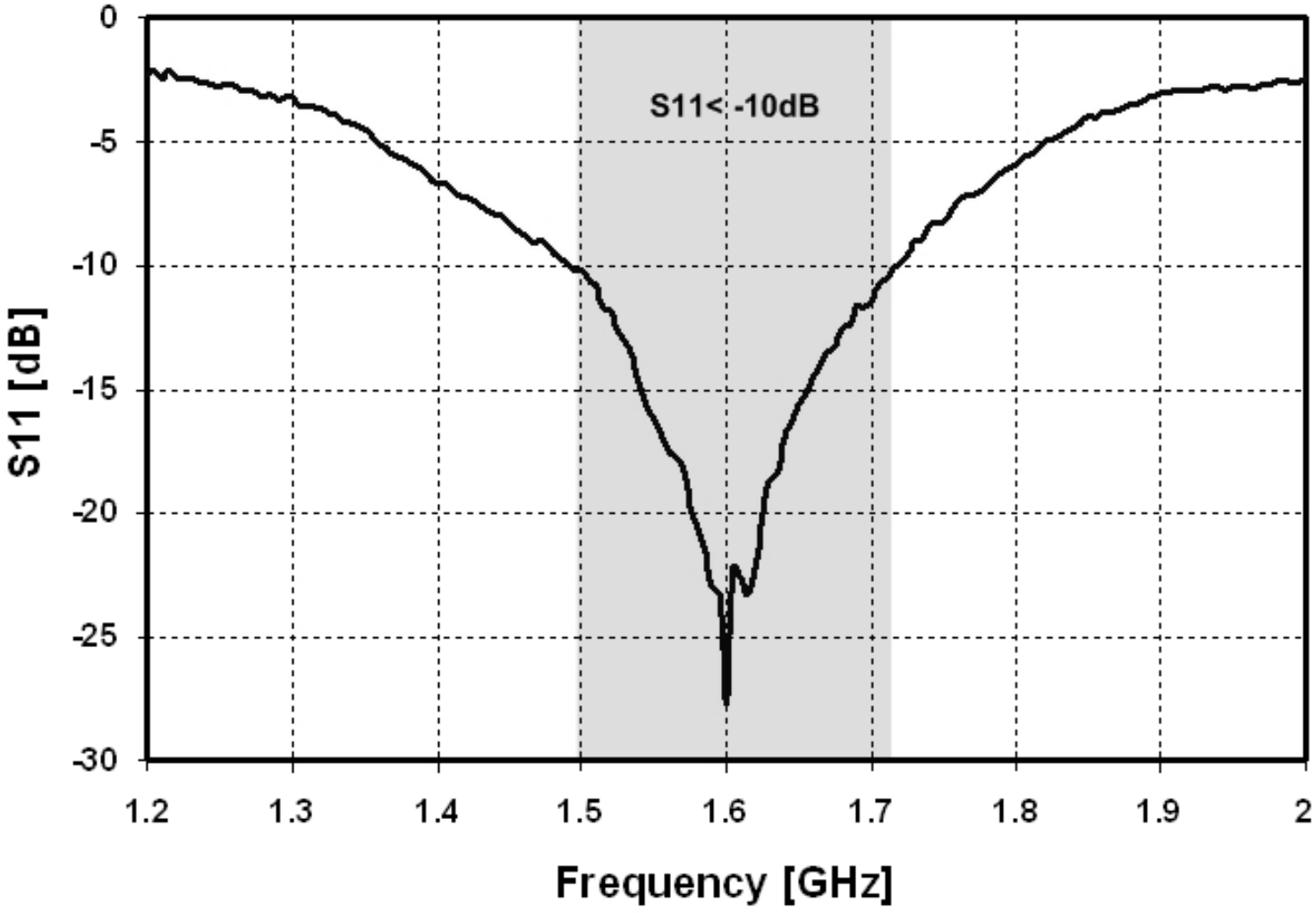

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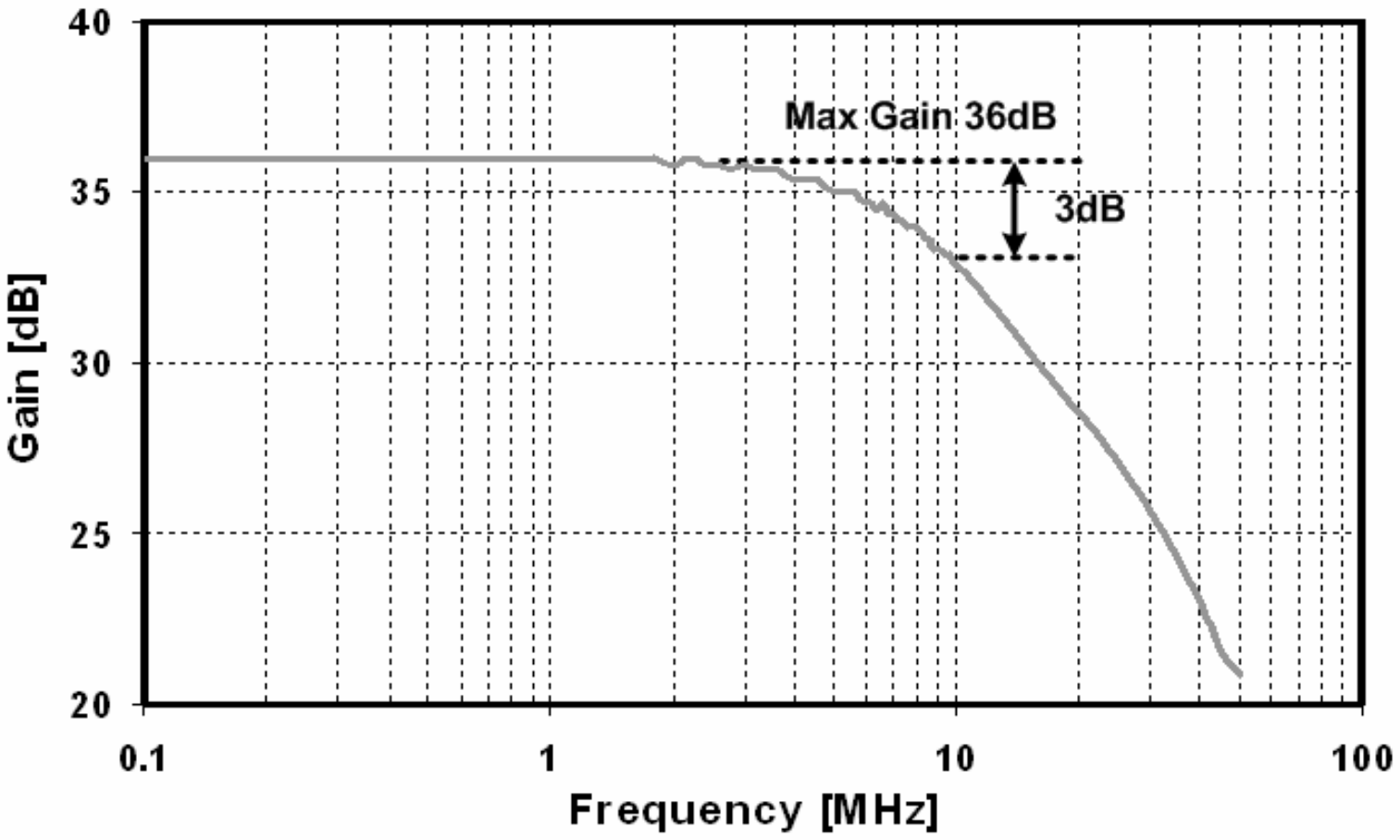

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