Single-Stage Low-Power Quadrature RF Receiver Front-End: The LMV Cell

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***Abstract*—This paper presents the first quadrature RF receiver front-end where, in a single stage, low-noise amplifier (LNA), mixer and voltage-controlled oscillator (VCO) share the same bias current. The new structure exploits the intrinsic mixing functionality of a classical *LC* tank oscillator providing a compact and low-power solution compatible with low-voltage technologies. A 0.13-μm CMOS prototype tailored to the GPS application is presented. The experimental results exhibit a noise figure of 4.8 dB, a gain of 36 dB, an IIP3 of -19 dBm with a total power consumption of only 5.4 mW from a voltage supply of 1.2 V.**

***Index Terms*—Current reuse, GPS receiver, *LC* tank oscillator, low-IF architecture, low power, low voltage, RF receiver, self-oscillating mixer (SOM).**

I. Introduction

GLOBAL POSITIONING system (GPS), sensor networks and radio frequency identification (RFID) systems can be considered the killer applications for ultra-low-power CMOS low-cost transceivers, tailored to large-scale diffusion [1]–[5]. However, while sensors and RFID transceivers trade off performance with longer battery life, GPS receivers still need high dynamic range especially when coexistence with cellular handset is wanted [4].

In this never-ending quest for vanishing power consumption in battery-powered radio ICs without renouncing to high performance, a favored technique seems to be current reuse across different functional blocks. A popular example is cascoding the Gilbert mixer on top of the input stage of the low-noise amplifier (LNA) in a receiver front-end, while less frequent is stacking voltage-controlled oscillator (VCO) and mixer [5], [6]. A further development takes advantage of the fact that a Gilbert mixer and a differential oscillator resemble each other very closely, since in both cases the differential-pair transistors behave like switches. As it happens, the mixer and VCO can be merged into a single block, referred to as the self-oscillating mixer (SOM) [6], [7]. However, if spectral purity demands the use of an *LC* tank oscillator, a SOM approach is confronted with the need of handling at the same time the RF carrier and the downconverted signal, which, in IC realizations, will be at low IF or even at baseband. The SOM should therefore provide enough gain at very low frequencies where, unfortunately, the *LC* tank presents a negligible impedance.

In this paper, a new RF front-end receiver topology merging LNA, mixer, and VCO in a single stage is presented. The structure, called the LMV cell, performs RF amplification, mixing, and local oscillator (LO) generation while sharing the same bias current and the same devices among all the blocks of the RF front-end, resulting in a very low-power, small-area solution. Although the merging of several building blocks is generally associated with a reduced flexibility, in this case the LMV cell preserves the possibility of easy insertion in a conventional phase-locked loop (PLL) for quadrature LO generation.

Based on the LMV cell, an RF front-end receiver for GPS application has been developed [8]. The receiver includes a single-ended low-noise amplifier, a couple of quadrature mixers, a couple of output buffers that sense the downconverted signal through a virtual ground and amplify it using an *RC* load, and the PLL. As a result, the solution obtained requires less than 3 mW for the RF part (LNA, mixer, and VCO).

The paper is organized as follows. In Section II, the traditional *LC* tank oscillator is analyzed, deriving from it two new self-oscillating mixer topologies. In Section III, the low-noise amplifier is introduced, completing the LMV cell. In Sections IV and V, the LMV cell transfer function is analyzed, discussing the main loss mechanisms in order to motivate the current-mode output topology adopted. In Section VI, the GPS receiver front-end design is described. Finally, a complete set of experimental measurements carried out on a 0.13-μm CMOS prototype are reported and some conclusions are drawn.

II. *LC*-Tank Oscillator Topology as a Mixer

A conventional *LC* tank oscillator, as the one shown in Fig. 1, intrinsically performs the mixing functionality since any RF signal in the VCO bias current is down-converted by the switching pair M1–M2. This occurs through the same mechanism by which the DC current of M0 is up-converted to the LO frequency. The mixing property of this structure is exploited in transmission where the *LC* tank oscillator is used as up-converter in direct modulation architectures [9]. Nevertheless, when this topology is used as a down-converter, the high-Q *LC* tank attenuates the low-frequency signal, preventing any IF amplification (Fig. 1).

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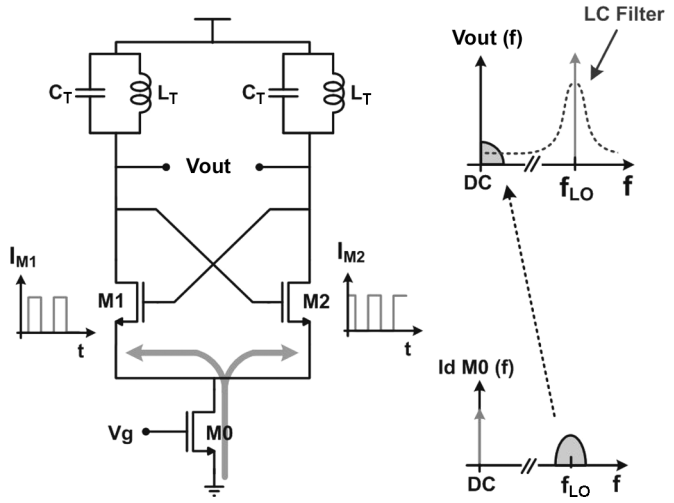


Fig. 1. *LC* tank oscillator as a mixer.

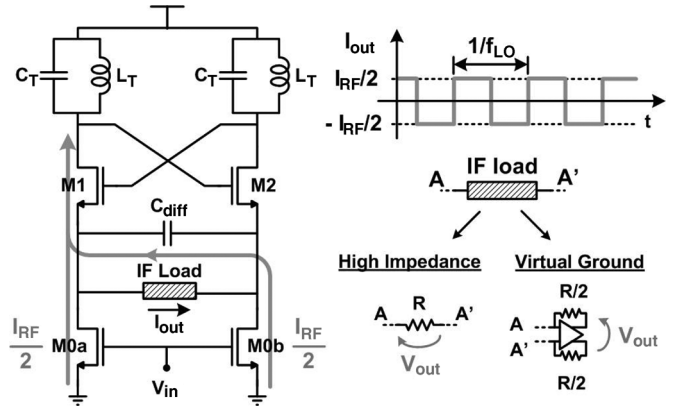


Fig. 2. Bias splitting self-oscillating mixer.

Attempting to sense the downconverted signal at the output of the VCO unavoidably degrades the oscillator phase noise, therefore, the idea is to read it at the sources of M1 and M2 as shown in Fig. 2. The idea is to split the bias current generator M0 (working as a transconductor for the input signal) in two transistors M0a and M0b, substituting the short circuit between the sources of M1 and M2 with the capacitance $C_{\rm diff}$ that closes the loop at RF while presenting a high impedance at IF. The capacitance $C_{\rm diff}$ degenerates transistors M1 and M2 and its value must satisfy the following condition in order to not reduce significantly the loop gain:

$$2\pi f_{\rm LO} C_{\rm diff} \gg gm_{1,2} \tag{1}$$

where $f_{\rm LO}$ is the oscillation frequency and $gm_{1,2}$ are the transconductance of M1 and M2. Notice that at RF (when the $C_{\rm diff}$ may be considered a short circuit) the structure is exactly the same as a traditional *LC* tank oscillator, preserving the tuning capability and, therefore, the possibility to be used in traditional PLL architectures.

Starting from this modified topology, the downconverted signal can be read at the sources of M1–M2 by an IF load (Fig. 2). In the first half of the LO period, when M1 is closed and M2 open, the signal injected by M0a ($I_{\rm RF}/2$) flows directly into M1, while the signal coming from M0b flows through the IF load. In the second half of the period, when M2 is closed, the $I_{\rm RF}/2$ current injected by M0a flows through the IF load. As reported in Fig. 2, the total input current $I_{\rm RF}/2$ is multiplied by a square wave and sensed at the output without perturbing the local oscillator since the IF load degenerates transistors M1–M2 only at low frequencies. This solution, named *bias splitting SOM*, can use either a high-impedance load to provide voltage gain at its IF output or a virtual ground load that shorts out the sources of M1 and M2 also at low frequencies. The choice of the IF load will be discussed in detail in Section IV, where all parasitic elements will be taken in account.

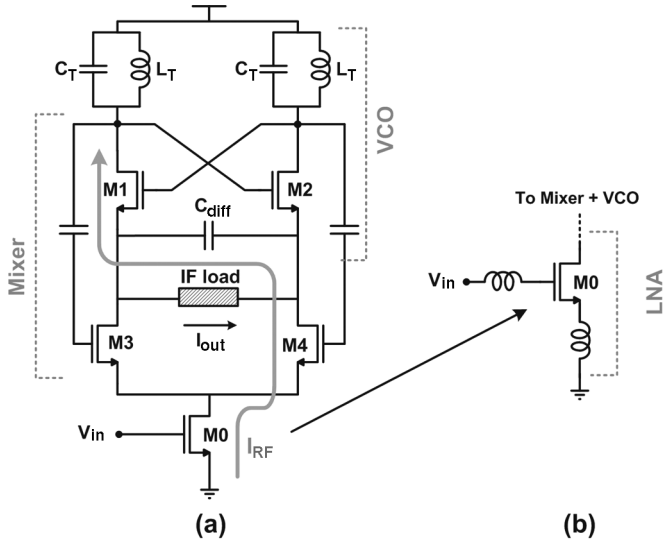


Fig. 3. Double switching pair self-oscillating mixer and LMV.

The ideal conversion gain of the *bias splitting SOM* is only $1/\pi$, since only half of the total RF current injected by M0a and M0b flows alternatively through the IF load. The conversion gain can be doubled by introducing an additional switching pair M3–M4 between the input transconductor M0 and the original switching pair M1–M2, as shown in Fig. 3(a). M3 and M4 are driven by the LO signals in opposite phase than M1–M2. In this way, all the signal current flows through the IF load, giving a conversion gain equal to $2/\pi$. The price paid is a slight increase of the voltage supply required by the new topology of self-oscillating mixer, called *double switching pair SOM*.

III. LMV Cell

The LNA can be inserted in a *double switching pair SOM* without requiring any additional active device by transforming M0 into an inductive degenerated LNA as shown in Fig. 3(b). In this way, a single cell merges all the main blocks of an RF front-end, realizing the LNA-mixer-VCO (LMV) cell. Although three transistors are stacked, the minimum voltage supply required is equal to only one threshold plus three overdrive voltages, maintaining compatibility with low-voltage technologies. The LNA, mixer and VCO are not simply stacked but share the same devices that play a double role, one at RF and one at IF, without introducing conflicts between the two domains. For example, transistor M0 acts as an LNA at RF, while providing the DC bias current to the VCO, or similarly M1–M2 perform

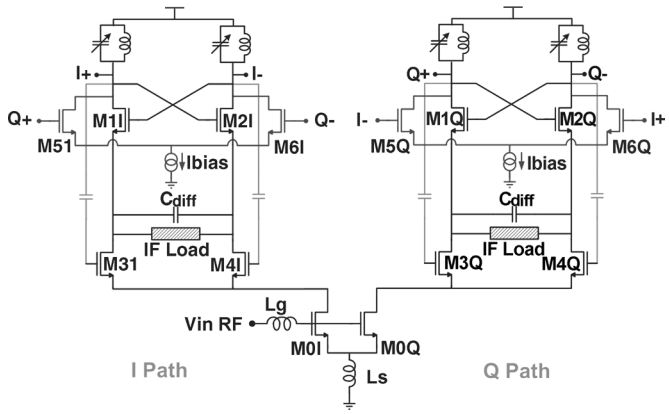


Fig. 4. LNA's low-frequency degeneration for LMV cell phase noise reduction.

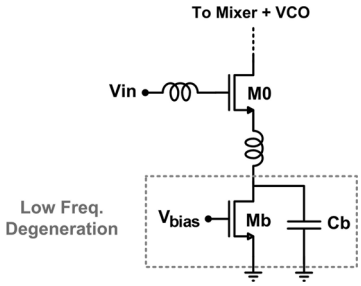


Fig. 5. Quadrature LMV scheme.

the mixing task while contributing, together with the capacitance $C_{\rm diff}$, to the VCO operation at RF. Therefore, several apparently contrasting tasks have been successfully merged: current reuse, multiple functionality without spurious interactions, device count reduction, and compatibility with a low supply voltage.

The versatility of the LMV cell allows it to be used in a quadrature RF front-end and to be inserted in traditional PLL architectures. This is possible because at RF the merged structure looks exactly as a traditional *LC* oscillator. As shown in Fig. 4, quadrature operation is straightforwardly achieved via the standard cross-coupling of two VCOs through the additional differential pairs M5–M6 and M5Q–M6Q (Fig. 4) [11]. This does not interfere with the rest of the LMV and is yet another proof of the robustness of the cell.

When several blocks are merged into a single one, necessarily the number of the degrees of freedom is reduced. In this case, there is a design trade-off between LNA and VCO in the choice of the aspect ratio of M0, which is, at the same time, the VCO bias generator and the core of the low-noise amplifier. In particular, to optimize the LNA NF and to reduce RF losses, M0 should have minimum channel length (L) and small width (W) [10]. On the other hand, the flicker noise injected by M0 degrades the VCO phase noise and, for this reason, a large $L \times W$ is needed. To avoid this trade-off, a low-frequency degeneration can be introduced, attenuating the 1/f noise injected by M0 into the VCO (Fig. 5).

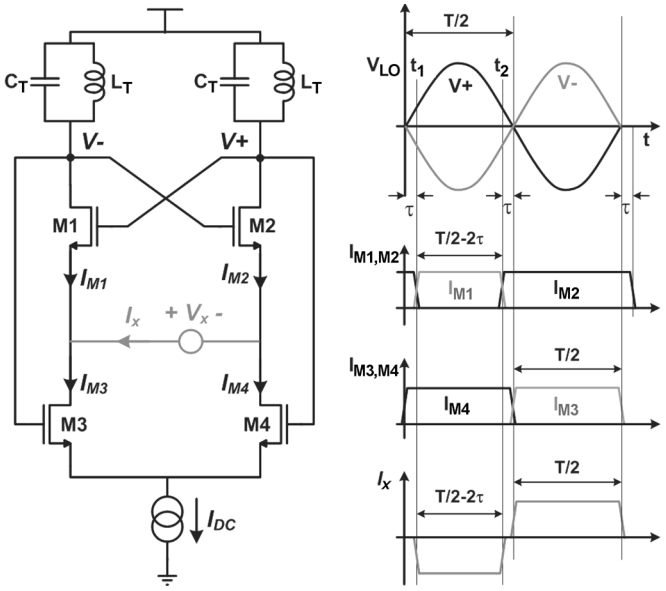


Fig. 6. Voltage gain upper bound. (a) Circuit for the calculus. (b) Currents waveforms.

IV. Loss Mechanisms

The analysis proposed in this section will address the main differences between the two possible IF loads reported in Fig. 2, compatible with the LMV cell. In the following, we will refer to the *voltage* LMV if a high-impedance IF load is considered and to the *current* LMV if the IF load is implemented through a virtual ground. Although the voltage solution reduces its noise contribution to the overall NF, providing voltage gain in front of the IF chain, it will be shown that it suffers from an intrinsic limitation which poses an upper bound to the achievable voltage conversion gain. Moreover, it is much more sensitive to the parasitic capacitors present at the IF nodes than the current solution.

A. Gain Upper Bound of Voltage LMV

Even when the RF current is completely downconverted (with a conversion gain equal to $2/\pi$), the voltage solution suffers from an undesired low-frequency equivalent resistance appearing at the sources of M1–M2 that limits the maximum achievable voltage gain.

Referring to Fig. 6, this resistance value can be computed by evaluating the current flowing through a test voltage applied at the output of the cell. Assuming for all transistors hard switching operation (i.e., $V_{\rm LO}$ much larger than the DC-overdrive), if $v_x = 0$ all the devices switch when $V_{\rm LO}^{+} = V_{\rm LO}^{-}$, therefore the drain currents are square waves with 50% duty cycle and a peak amplitude equal to $I_{\rm DC}$. Applying $v_x > 0$ at the source of M1–M2 modifies the duty cycle of the current flowing through them but has no effect on M3 and M4 (Fig. 6). The switching instants for M1 and M2 are solutions to the following equation:

$$V_{\rm LO} sin(2\pi f_{\rm LO} t) = -V_{\rm LO} sin(2\pi f_{\rm LO} t) + v_x \qquad (2)$$

where $V_{\rm LO}$ and $f_{\rm LO}$ are the oscillation amplitude and frequency, respectively. For $v_x \ll 2\ V_{\rm LO}$, (2) gives

$$t_1 = \tau \approx \frac{v_x}{4\pi f_{\rm LO} V_{\rm LO}}, \quad t_2 \approx \frac{T}{2} - \tau \qquad (3)$$

where $T = 1/f_{\rm LO}$ is the LO period. The current through the voltage source is given by $I_{\rm M1} - I_{\rm M3}$ and is plotted in Fig. 6. Its average value is

$$\overline{i_x} = \frac{-I_{\rm DC} \cdot (T/2 - 2\tau) + I_{\rm DC} \cdot (T/2)}{T} = \frac{I_{\rm DC}}{2\pi V_{\rm LO}} v_x. \quad (4)$$

From (4), the equivalent resistance is given by

$$R_x = \frac{v_x}{\overline{i_x}} = \frac{2\pi V_{\rm LO}}{I_{\rm DC}} = 4\omega_{\rm LO} L_T Q \quad (5)$$

where the last simplification is valid if the oscillator works in current limited regime since $V_{\rm LO} = 2\omega_{\rm LO} L_T Q I_{\rm DC}/\pi$ [9]. Due to the limited Q of integrated inductors, the parasitic elements and the tuning requirements that limit the value of L_T, this effect cannot be neglected when using a voltage-mode solution.

B. Gain Loss Due to Parasitic Capacitors

The parasitic capacitors connected between the IF nodes and ground (mainly due to the parasitic elements of transistors M1–M4 and, possibly, to the input capacitors of the amplifier used to sense the IF nodes) limit the conversion gain of both the voltage and current LMV solutions. Their impact is, however, considerably different in the two cases.

The analytical derivation of the transfer function in the presence of capacitances at the output is difficult since the structure is time-variant, preventing a simple investigation in the frequency domain. To simplify the analysis, it can be noticed that assuming the transistor M0 of Fig. 3 working as an ideal current source, the drain current of the transistor pair M3–M4 is given by

$$\begin{cases} I_{M3} = \dfrac{I_{M0}}{2}\left(1 + sign\left(cos(\omega_{\rm LO} t)\right)\right) \\ I_{M4} = \dfrac{I_{M0}}{2}\left(1 - sign\left(cos(\omega_{\rm LO} t)\right)\right) \end{cases} \quad (6)$$

These equations show that the total current through M3 and M4 can be decomposed as the sum of two portions with the same peak amplitude $I_{\rm M0}/2$: a common-mode one and a differential one multiplied by $sign(cos(\omega_{\rm LO} t))$. Hence, the *double switching pair SOM*, drawn in Fig. 3, can be transformed in the "parallel" of two *bias splitting SOM* as shown in Fig. 7, whose current sources inject a common-mode signal at RF and a differential one at $\omega_{\rm RF} - \omega_{\rm LO}$. Based on this equivalent model, the losses due to the parasitic capacitances both at low frequency and at RF are now discussed.

The signal loss for the low-frequency current components Fig. 7(a) can be computed using a switched-capacitor approach. Assuming the transistors act like switches driven by a signal at $\omega_{\rm LO}$, M3 and M4 redistribute the charge injected in the capacitances $C_{\rm par}$, producing an equivalent resistance in parallel with the IF load equal, in the worst case to $1/2C_{\rm par} f_{\rm LO}$ (as explained in Appendix I), that introduces a loss if a high-impedance load is chosen (voltage solution). On the contrary, the current solution is immune to this mechanism because in this case the IF load shows an impedance close to zero and all the input differential current flows into the virtual ground resulting in a conversion gain close to $1/\pi$. A more detailed analysis is reported in Appendix I.

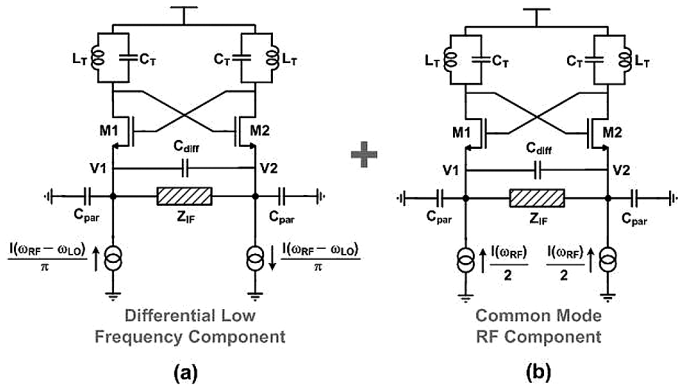


Fig. 7. Loss mechanisms. (a) Low-frequency components. (b) RF components.

The study of the losses due to the parasitic capacitances $C_{\rm par}$ is completed analyzing the common-mode portion of the equivalent circuit shown in Fig. 7(b). In this case the parasitic capacitances are in parallel to the input current sources that inject a signal at RF. The resulting loss is, at first order, independent from the IF load (differential) used (current or voltage mode approach).

Considering the two phenomena at low and high frequencies, the voltage-mode configuration appears more sensitive to the parasitic capacitances because it experiences losses in both cases. On the contrary, independently of the value of $C_{\rm par}$, the current solution has a conversion gain of at least $1/\pi$ since it has negligible losses at low frequency.

The presence of a fundamental upper bound on the achievable gain and the major sensitivity to the parasitic elements of the voltage solution have motivated the choice of a current-mode LMV cell for the design of the GPS front-end. In the next section, the analytical expression for the current-mode LMV cell conversion gain will be derived.

V. Current-Mode LMV Cell Conversion Gain

As discussed in the previous section and in Appendix I, when a current solution is used, the only loss mechanism is the one associated with the RF common-mode input signal represented in Fig. 7(b). If a current approach is used to sense the down-converted signal, the circuit can be simplified since, to a first approximation, the presence of both capacitance $C_{\rm diff}$ and the virtual ground shorts out the sources of M1 and M2 at all frequencies.

Referring to Fig. 8, assuming transistors M1–M2 are in the triode region with a negligible on-resistance, since $V1(t) = V2(t)$, $I_{\rm p1}(t) = I_{\rm p2}(t)$ and the current that flows through the virtual ground is

$$I_{\rm IF}(t) = \frac{1}{2}\left[I_{\rm M1}(t) - I_{\rm M2}(t)\right]. \quad (7)$$

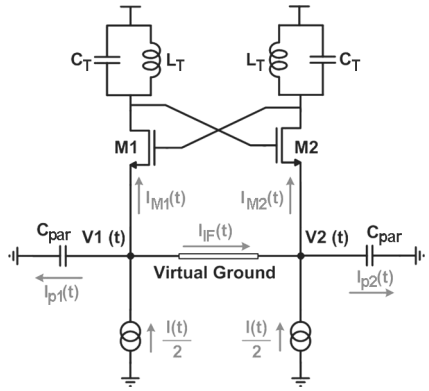


Fig. 8. Current-mode LMV cell.

Assuming full current switching, $I_{\rm M1}$ and $I_{\rm M2}$ can be rewritten as

$$\begin{cases} I_{\rm M1}(t) = [I_{\rm M1}(t) + I_{\rm M2}(t)] \cdot \frac{1}{2}\left[1 + sign\left(cos(\omega_{\rm LO}t)\right)\right] \\ I_{\rm M2}(t) = [I_{\rm M1}(t) + I_{\rm M2}(t)] \cdot \frac{1}{2}\left[1 - sign\left(cos(\omega_{\rm LO}t)\right)\right] \end{cases}. \tag{8}$$

Inserting (8) in (7), the $I_{\rm IF}$ current becomes

$$I_{\rm IF}(t) = \frac{1}{2}\left[I_{\rm M1}(t) + I_{\rm M2}(t)\right] sign\left(cos(\omega_{\rm LO}t)\right) \tag{9}$$

showing that the downconverted current $I_{\rm IF}$ is given by the total current flowing into M1 and M2 multiplied by a squared wave. $I_{\rm M1}(t) + I_{\rm M2}(t)$ has only RF components and can be obtained by partitioning the input signal current between the capacitances $C_{\rm par}$ and the impedance shown by the switching pair M1–M2, given by $Z_{\rm tank}(\omega_{\rm RF})/2$, where $Z_{\rm tank}(\omega_{\rm RF})$ is the L_TC_T tank impedance (see Appendix II). As a consequence, the frequency domain expression for $I_{\rm M1}(t) + I_{\rm M2}(t)$ is given by

$$I_{M1+M2} = I(\omega_{\rm RF})\frac{1}{1 + j\omega_{\rm RF}C_{\rm par} \cdot Z_{\rm tank}(\omega_{\rm RF})}. \tag{10}$$

From (10) and (9), the down-converted current becomes

$$I_{\rm IF} = \frac{1}{\pi}\frac{1}{1 + j\omega_{\rm RF}C_{\rm par} \cdot Z_{\rm tank}(\omega_{\rm RF})} I(\omega_{\rm RF} - \omega_{\rm LO}). \tag{11}$$

Notice that this represents only the output current due to the common-mode component of the input signal. To obtain the total conversion gain the contribution of the differential component, given by $I(\omega_{\rm RF} - \omega_{\rm LO})/\pi$, has also to be added giving a total output current of

$$I_{\rm IF} = \frac{1}{\pi}\frac{2 + j\omega_{\rm RF}C_{\rm par} \cdot Z_{\rm tank}(\omega_{\rm RF})}{1 + j\omega_{\rm RF}C_{\rm par} \cdot Z_{\rm tank}(\omega_{\rm RF})} I(\omega_{\rm RF} - \omega_{\rm LO}). \tag{12}$$

The DC conversion gain, corresponding to $\omega_{\rm RF} = \omega_{\rm LO}$, is given by

$$I_{\rm IF} = \frac{1}{\pi}\frac{2 + j\omega_{\rm LO}C_{\rm par} \cdot \omega_{\rm LO}L_TQ}{1 + j\omega_{\rm LO}C_{\rm par} \cdot \omega_{\rm LO}L_TQ} I(\omega_{\rm RF} - \omega_{\rm LO}) \tag{13}$$

where $\omega_{\rm LO}L_TQ$ is the impedance shown by the *LC* tank at resonance. Notice that from (13) for $C_{\rm par} = 0$, the gain is equal to $2/\pi$, while it has a minimum value of $1/\pi$ for a very high $C_{\rm par}$.

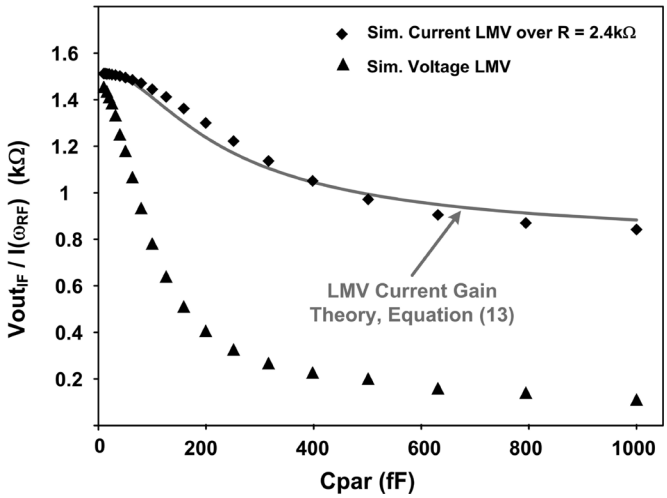


Fig. 9. Simulations of current-mode and voltage-mode gain as function of $C_{\rm par}$.

To validate (13) and to gain quantitatively insight on the parasitic effects previously discussed, Fig. 9 reports simulations of the conversion gain versus the value of $C_{\rm par}$ for the voltage and current LMV cells. M0 is replaced in both cases by an ideal current source. Moreover the BSIM3v3 device models have been modified in order to make negligible the intrinsic device parasitic capacitances, leaving the possibility of placing a well-defined explicit $C_{\rm par}$.

The *LC* tanks are made of 5 nH inductors showing a quality factor of about 13. The tank resonate at 1.57 GHz leading to a tank parallel resistance of $R_T \approx 650\,\Omega$. The voltage LMV cell does not make use of an explicit IF load resistor because, due to its intrinsic gain limitation, the topology provides an equivalent resistance, shunting the IF nodes, close to $4R_T$. The virtual ground for the current LMV cell is implemented with a 50 dB gain opamp and 1.2-kΩ feedback resistors.

Simulations of Fig. 9 confirm the superior immunity to $C_{\rm par}$ of the current LMV topology. In fact, while the conversion gain of the voltage solution drops rapidly, leading to a tolerable $C_{\rm par}$ much less than 200 fF, the current LMV cell can drive grounded capacitors up to 1 pF. Equation (13) is also compared with simulated results showing excellent agreement over the whole range of $C_{\rm par}$ considered.

VI. Ultra-Low-Power GPS RF Front-End Design

The block diagram of the integrated quadrature GPS front-end receiver is reported in Fig. 10. The receiver is made of two cross-coupled LMV cells generating the quadrature paths, inserted into a PLL together with two baseband output buffers. The signal current down-converted at a low IF of 4 MHz, flows into a low-frequency virtual ground, realized with a super-cascode topology, and is finally collected as a voltage at the output of the buffers. The RF portion of the receiver is therefore operated in the current domain, while voltage amplification occurs only at baseband. As already explained, the use of a virtual ground at the mixer outputs reduces the sensitivity to parasitic capacitances, moreover, moving the whole voltage gain out of the LMV stack allows the

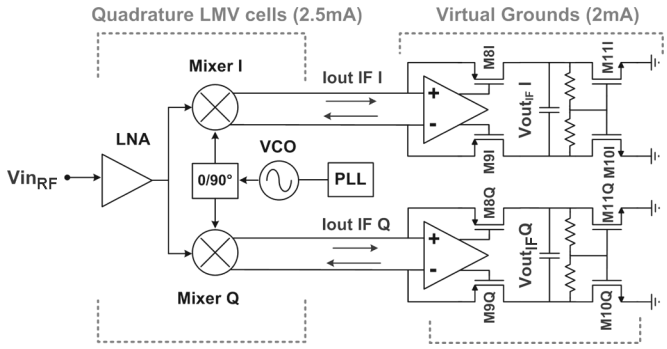


Fig. 10. Complete RF front-end based on low-IF architecture for GPS receiver.

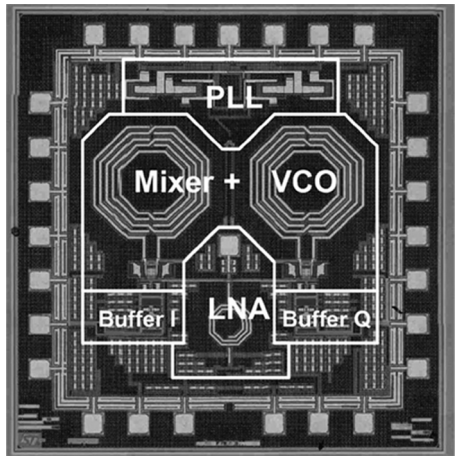


Fig. 11. Die micrograph.

reduction of the minimum supply voltage required for proper operations. On the other hand, the lack of voltage gain in front of the baseband buffers tends to increase the contribution of these stages to the overall noise figure.

Quadrature operation is straightforwardly achieved via the standard cross-coupling of the two VCOs reported in Fig. 4. It should be noticed that the additional pairs do not significantly affect the total current consumption. This because in GPS receivers the noise figure of the front-end is not appreciably deteriorated even for large departures from ideal quadrature LO [12], and therefore the bias current in the additional pairs can be set at only 20% of the oscillators bias current to achieve a phase error lower than five degrees. The additional low-frequency degeneration reported in Fig. 5 has been added to reduce the LO phase noise. In this way, dimensions and aspect ratio of the M0 have been chosen for optimum RF performance.

A. Output Virtual Ground

The virtual short-circuit is provided by an operational amplifier and the pMOS cascode pair M8–M9 shown in Fig. 10. In this way, the amplifier drives high-impedance nodes, as opposed to a more traditional solution based on resistive feedback. In addition, a self-biased active load M10–M11 is preferred to a simple resistive load, because of reduced DC voltage swing. A common-mode feedback loop is used to bias the output stages: cascode transistors M8–M9 are spilling current from the oscillator core, therefore the bias point is determined with great accuracy.

In the amplifier, the input differential pair is the most critical element in terms of noise. The use of a long channel device would be preferred in order to reduce 1/f noise and boost the gain, while the input capacitive load must be kept as low as possible since it contributes to $C_{\rm par}$ at the output of the LMV cell. In fact, the capacitive load at the input of the operational amplifier not only decreases the LMV gain, but reduces the equivalent resistance at the opamp virtual ground through a switched-capacitor effect similar to what occurs in a current-mode passive mixer that amplifies the virtual ground noise [13], [14].

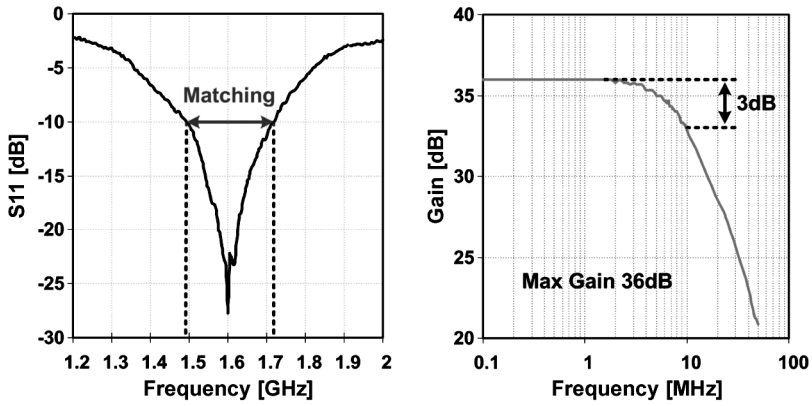
VII. Experimental Results

The front-end chip micrograph, fabricated in a 0.13-μm CMOS process is shown in Fig. 11. All pads are ESD protected and the active die area is 1.5 mm^2. Only three integrated inductors are used, resulting in a modest area occupation. To minimize common-mode signals, induced by parasitic bond wire inductances, multiple pads with multiple bonding are used for ground and voltage supply connections. Moreover, large on-chip bypass capacitors (around 200 pF) are used to filter the noise on the supply voltage with respect to ground. The RF input is located in the middle of the die to minimize the capacitance at the gate of the inductive degenerated amplifier. To improve reliability, thick gate oxide MOS transistors have been used in both VCO and mixer, although this is not strictly necessary when the minimum supply voltage (1.2 V) is used in the RF part. With typical technology parameters, the supply voltage can be lowered to 1 V while maintaining proper operation.

The die was bounded on a dedicated single-side RF board, realized with FR4 substrate, where 50-Ω strip lines, optimized by means of EM simulations, carry the input signals from the SMA connectors to the die.

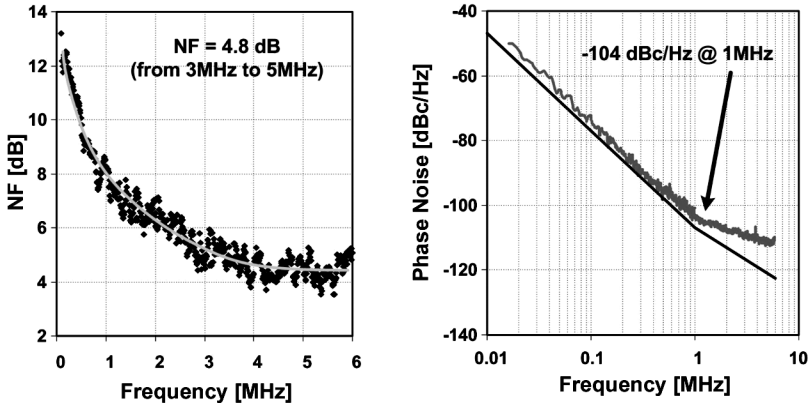
The input reflection coefficient has been tested by means of an Anritsu 37347C vector network analyzer. Fig. 12(a) shows the measured S_{11} for the circuit, displaying a good input matching at the GPS frequency. A plot of the voltage gain versus frequency at baseband, obtained using a differential load of 1.2 kΩ, is shown in Fig. 12(b). The gain is close to 36 dB and rolls off at about 10 MHz where the filter pole is placed.

The noise figure was evaluated by means of an HP346B noise source. At the receiver output, a high-speed low-distortion differential amplifier (MAX4146) was used to convert the differential IF output signal to a single-ended format, drive the measurement equipment 50-Ω input ports, and raise the front-end output noise above the sensitivity level of the HP8564E spectrum analyzer which is used to capture its frequency content. The noise figure (NF) measure is reported in Fig. 13(a). The NF integrated over the IF band (3 to 5 MHz) is 4.8 dB with the 1/f corner at 1.2 MHz. From simulations, the LNA and the baseband are the first two noise contributors for the thermal and flicker noise, respectively. This is due to the fact that, as previously explained, the finite output impedance of the LMV cell amplifies the input-referred noise of the operational amplifier.



(a) (b)

Fig. 12. (a) Input matching and (b) in-band gain measurements.



(a) (b)

Fig. 13. (a) Noise figure and (b) phase noise measurements.

The IIP3 is −19 dBm, while the 1-dB compression point is −31 dBm. The VCO phase noise versus frequency is shown in Fig. 13(b). It is equal to −104 dBc/Hz at 1-MHz offset frequency. The dominant contribution comes from the flicker noise of the cross-coupling and from the LNA transistors. The phase error between the I and Q paths is less than 5 degrees, enough to avoid a deterioration of the overall noise figure due to imperfect image rejection [12]. The quadrature front-end with the output stages draws a total of 4.5 mA from 1.2 V (this excludes the circuits used to close the PLL loop that are not optimized for use in a GPS receiver).

A summary of the most relevant measurements and a comparison with the state of the art is reported in Table I. In particular, the solution proposed (also including the PLL) represents the less onerous in terms of power consumption. It can be seen how the closer power dissipation can be reached by decreasing the receiver performance [15] or through a partial current reuse [5].

VIII. Conclusion

Two new self-oscillating mixer architectures (*bias-splitting* and *double-switching pair SOMs*), derived from the *LC* tank topology, have been presented. Furthermore, starting from the *double-switching pair* solution, a single-stage RF front-end has been developed sharing the same bias, for the first time, between the LNA, mixer, and VCO. With the LMV cell, several apparently contrasting tasks have been successfully merged: current reuse, multiple functionality without spurious interactions, device count reduction, and compatibility with a low supply voltage. The flexibility of the cell has been demonstrated, proposing different design strategies based on both voltage and current output, and realizing a very low-power GPS RF quadrature front-end.

Appendix I

As shown in Fig. 7(a), the parasitic capacitors of transistors M1–M4 $(C_{\rm par})$ are connected between the output nodes and ground and discharged at each period by M1–M2. This parasitic effect leads to an additional equivalent resistance shunting the outputs nodes, which, once again, limits the maximum conversion gain of the voltage LMV cell.

To analytically capture this effect some simplifications have been introduced and drawn in Fig. 14(a). First, in order to distinguish between the intrinsic effect given by the *LC* tanks and previously derived, the oscillator loop is open and transistors M1 and M2 are driven with opposite phase sinusoids at the LO frequency. Moreover, it is still assumed transistors working as switches and a pair of resistances (R1, R2) are used instead of the *LC* tank. The difference arising from considering the whole *LC* tank will be discussed qualitatively later.

TABLE I
FRONT-END PERFORMANCE SUMMARY AND COMPARISON WITH GPS CMOS STATE OF THE ART

	[1]	[5]	[15]	**This Work**
Gain [dB]	(25)+60	(50)+80	(33)+60	36
NF [dB]	4	4	8.5	4.8
IIP3 [dBm]	n.a.	-15	n.a.	-19
1dB Comp. Point[dBm]	-28	n.a.	n.a.	-31
PN @ 1MHz [dBc/Hz]	-95	-107	-109	-104
LO leak. at input[dBm]	-66	n.a.	n.a.	-55
Technology	0.18μm	0.35μm	0.18μm	0.13μm
Total Power [mW]	**35**	**27**	**19**	**11***

***PLL power consumption included (5.6mW)**

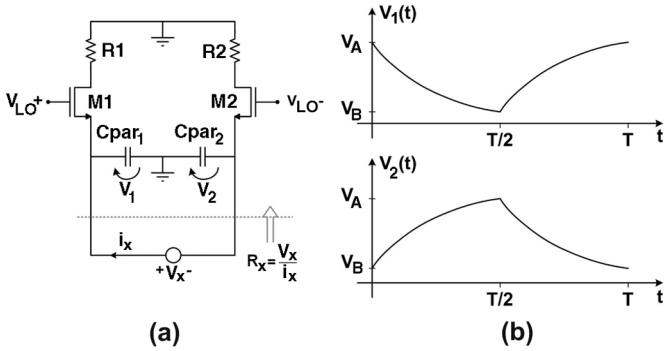


Fig. 14. Circuit for switched-impedance calculus and voltage waveforms.

Starting from the circuit in Fig. 14(a), the equivalent resistance is again calculated from the current flowing through a low-frequency test voltage, v_x, across the output nodes. When M1 is on and M2 is off, $C_{\rm par1}$ discharges on R1 while $C_{\rm par2}$ sinks charge from v_x. The opposite happens during the second half of the LO period, when M2 is on and M1 is off.

The voltage waveforms across the two capacitors, $V1(t)$ and $V2(t)$, are depicted in Fig. 14(b). For $0 < t < T/2$, when M1 is on and M2 off, the differential equation governing $C_{\rm par1}$ discharge is

$$\begin{aligned} C_{\rm par1}\cdot\frac{dV_1}{dt}+\frac{V_1}{R_1} &= C_{\rm par2}\cdot\frac{dV_2}{dt} \\ &= C_{\rm par2}\cdot\frac{d(v_x-V_1)}{dt} \\ &\simeq -C_{\rm par2}\cdot\frac{dV_1}{dt}. \end{aligned} \tag{A.1}$$

The last simplification is made under the assumption that v_x varies slowly with respect to the oscillation period. With $C_{\rm par1}=C_{\rm par2}=C_{\rm par}$ and $R1=R2=\omega_{\rm LO}L_T{\rm Q}=R_T$, the solution of (A.1) is given by

$$V_1(t)=V_A e^{-\frac{t}{2C_{\rm par}R_T}} \tag{A.2}$$

where V_A is the maximum capacitor voltage. Looking at Fig. 14(b), the minimum capacitor voltage V_B is

$$V_B=V_1\left(\frac{T}{2}\right)=V_A e^{-\frac{T}{4C_{\rm par}R_T}}=V_A e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}} \tag{A.3}$$

where $f_{\rm LO}$ is the local oscillator frequency. Since $V_A+V_B=v_x$, using (A.2) and (A.3) the minimum and maximum capacitors voltages can be expressed as a function of v_x, obtaining

$$V_A=\frac{1}{1+e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}v_x,\quad V_B=\frac{e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}{1+e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}v_x. \tag{A.4}$$

The total charge sunk from v_x, and dissipated on R in one oscillation period is $q=2C_{\rm par}(V_A-V_B)$. This leads to a net current, i_x, flowing through the voltage generator, with an average value of

$$\begin{aligned} \overline{i_x} &= q\cdot f_{\rm LO}=2C_{\rm par}f_{\rm LO}(V_A-V_B) \\ &= 2C_{\rm par}f_{\rm LO}\left(\frac{1-e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}{1+e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}\right)v_x. \end{aligned} \tag{A.5}$$

From (A.5), the equivalent resistance across the output nodes is equal to

$$R_x=\frac{v_x}{\overline{i_x}}=\frac{1}{2C_{\rm par}f_{\rm LO}}\left(\frac{1+e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}{1-e^{-\frac{1}{4f_{\rm LO}C_{\rm par}R_T}}}\right). \tag{A.6}$$

To validate the above equation, simulations of R_x are reported in Fig. 15. The diamond-dots curve refers to the circuit of Fig. 14(a) with $R_T=650\ \Omega$, $(W/L)_{\rm M1,M2}=160/0.28$ and $f_{\rm LO}=1.57$ GHz. The solid line plots (A.6), showing optimum agreement with simulations over the whole range of $C_{\rm par}$ considered. The case of a complete *LC* tank, made of 5-nH inductors with $\rm Q=13$, has been also verified through simulations (square-dots curve). The corresponding R_x is lower than the case of R_T only and (A.6) may be therefore used as an upper

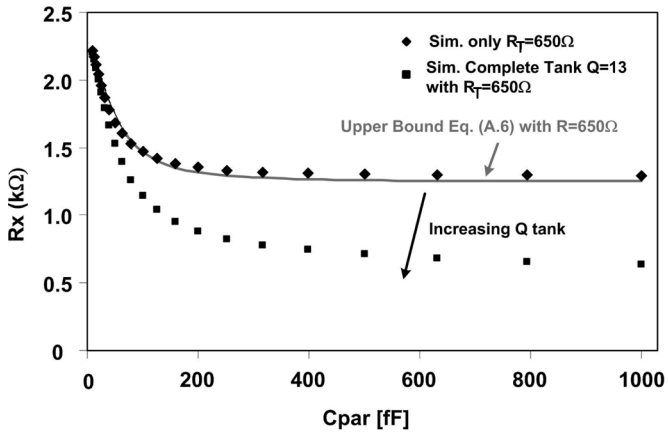


Fig. 15. Switched-impedance losses versus $C_{\rm par}$.

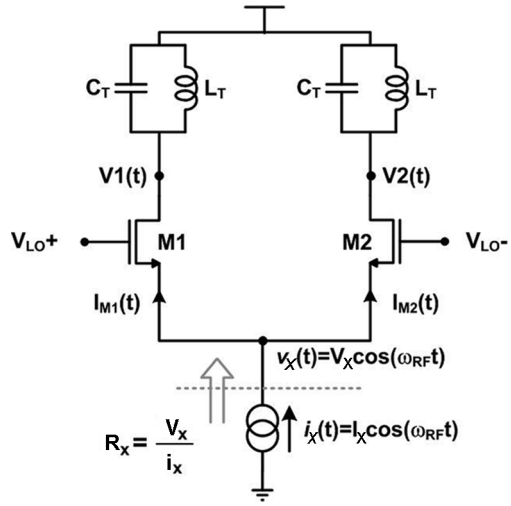


Fig. 16. Circuit for the calculus of RF impedance at the M1–M2 sources.

bound for this case. Intuitively, this is because also the tank capacitor and inductor contribute to $C_{\rm par}$ discharge. Notice in fact that, for fixed R_T, increasing the tank Q would require a lower inductance, eventually becoming a short circuit in the limit case of infinite Q. Equation (A.6) can be therefore also used as a lower bound for the loss resistance, R_x, for the complete *LC* tank simply by replacing $R_T = 0$.

APPENDIX II

In this Appendix, we want to evaluate the equivalent impedance at the sources of the switching pair M1–M2. As in Appendix I, the oscillator loop is considered open and transistors M1 and M2 driven with opposite phase sinusoids at the LO frequency $(\omega_{\rm LO})$ (Fig. 16). To calculate the equivalent impedance at $\omega_{\rm RF}$, it is convenient to use a current generator injecting a signal test (i_x) at $\omega_{\rm RF}$ close to $\omega_{\rm LO}$ and evaluating the voltage produced v_x.

The currents $I_{\rm M1}(t)$ and $I_{\rm M2}(t)$ follow the same law expressed by (7) and can be written as

$$\begin{aligned} I_{\rm M1}(t) &= I_x cos(\omega_{\rm RF}t)\cdot\frac{1}{2}\left[1+sign\left(cos(\omega_{\rm LO}t)\right)\right] \\ &= \frac{I_x}{2}cos(\omega_{\rm RF}t)+\frac{I_x}{\pi}cos\left((\omega_{\rm RF}\pm\omega_{\rm LO})t\right) \\ &\quad + \text{higher harmonics} \end{aligned} \tag{A.7}$$

$$\begin{aligned} I_{\rm M2}(t) &= I_x cos(\omega_{\rm RF}t)\cdot\frac{1}{2}\left[1-sign\left(cos(\omega_{\rm LO}t)\right)\right] \\ &= \frac{I_x}{2}cos(\omega_{\rm RF}t)-\frac{I_x}{\pi}cos\left((\omega_{\rm RF}\pm\omega_{\rm LO})t\right) \\ &\quad - \text{higher harmonics}. \end{aligned} \tag{A.8}$$

Even with a moderate quality factor, all the higher harmonics and the low-frequency term at $\omega_{\rm RF}-\omega_{\rm LO}$ are filtered out, leaving only the component close to $\omega_{\rm LO}$. As a consequence, the voltages $V1(t)$ and $V2(t)$ in Fig. 16 are

$$V1(t)=V2(t)=\frac{I_x}{2}cos(\omega_{\rm RF}t)Z_{\rm tank}(\omega_{\rm RF}) \tag{A.9}$$

where $Z_{\rm tank}(\omega_{\rm RF})$ is the value of the *LC* tank at $\omega_{\rm RF}$. The voltage $v_x(t)$ can be expressed as a function of $V1(t)$ and $V2(t)$ as

$$\begin{aligned} v_x(t) &= V1(t)\cdot\frac{1}{2}\left[1+sign\left(cos(\omega_{\rm LO}t)\right)\right] \\ &\quad + V2(t)\cdot\frac{1}{2}\left[1-sign\left(cos(\omega_{\rm LO}t)\right)\right] \\ &= \frac{V1(t)+V2(t)}{2}+\frac{V1(t)-V2(t)}{2} \\ &\quad \times sign\left(cos(\omega_{\rm LO}t)\right). \end{aligned} \tag{A.10}$$

To define the impedance in the frequency domain, the signal $v_x(t)$ has to be in the form $V_{\rm x}\cos(\omega_{\rm RF}t)$. Substituting (A.9) in (A.10), it can be obtained

$$v_x(t)=\frac{I_x}{2}cos(\omega_{\rm RF}t)Z(\omega_{\rm RF})=V_x cos(\omega_{\rm RF}t) \tag{A.11}$$

where $V_{\rm x}=Z_{\rm tank}(\omega_{\rm RF})I_{\rm x}/2$. Thus, the impedance Z at the sources of M1 and M2 can be written as

$$Z(\omega_{\rm RF})=\frac{V_x}{I_x}=\frac{Z_{\rm tank}(\omega_{\rm RF})}{2}. \tag{A.12}$$

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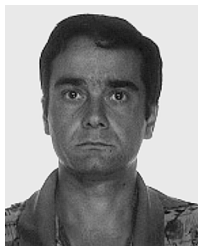

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