20.8 A 2.4 GHz 3.6mW 0.35mm² Quadrature Front-End RX for ZigBee and WPAN Applications

Antonio Liscidini, Marika Tedeschi, Rinaldo Castello

University of Pavia, Pavia, Italy

In the design of a single chip for wireless-sensor-network and WPAN applications (e.g., IEEE 802.15.4), the receiver sensitivity is generally sacrificed in favor of a vanishing power consumption and a low-cost solution [1]. There is a trade off between these two requirements, as the use of resonant loads offers high power efficiency while an inductor-free approach saves die area resulting in a cheaper design. Since an LC-oscillator topology is mandatory to achieve a minimal current draw, the reduction of the number of coils has to be done in the LNA, the mixer and the quadrature generator. In this work, starting from the LNA-Mixer and VCO (LMV) cell topology [2], a single-coil low-power receiver shares the bias current among all the RF blocks of the analog front-end. The receiver prototype chip consumes 3.6mW and has an active die area of 0.35mm². It is based on a low-IF architecture and includes a baseband variable-gain complex filter for channel selection (see Fig. 20.8.1) .

The circuit schematic of the single-coil quadrature LMV cell used for the RF front-end is shown in Fig. 20.8.2. The LNA (at the bottom of the stack) provides the DC bias and the quadrature RF signals, while the switching pairs of the I and Q paths (M2 to M5 and M6 to M9) perform the downconversion self-oscillating at the resonance frequency of the LC tank. The oscillation is sustained by M4-M5 and M8-M9 that are closed in positive feedback through capacitors C1 and C2 that show a very low impedance at the oscillation frequency. On the other hand, C1 and C2 represent a high impedance at IF frequency allowing the downconverted current signal to flow into the virtual ground of a transimpedance amplifier (TIA). The signal is finally converted into a voltage and collected at the TIA output (see Fig. 20.8.1). The TIA must show a low impedance over a sufficiently large bandwidth to ensure that no distortion terms are intermodulated in band in the presence of high-frequency blockers. For this reason, it is realized with the super-cascode structure. Compared to the previous solution [2], in the scheme reported in Fig. 20.8.2, the sum of the currents from I and Q paths flows into the same LC tank, saving area and producing the required LO amplitude with half of the bias current.

The circuit schematic of the LNA and the quadrature generator is shown in Fig. 20.8.3. The input matching is realized through an internal resistor R_{in} and a L-match network formed by the pad capacitance C_{pad}, the bond-wire and an external inductor. Although a resistive termination tends to increase the noise figure, this effect is mitigated by the resonant circuit at the input which provides a voltage gain at the gate of M0 boosting the LNA transconductance. Moreover, the narrow-band input matching network filters out blockers close to the double of the VCO oscillation frequency, avoiding any injection-locking phenomena.

As already stated, the quadrature generation is performed on the RF path instead of at the local oscillator level. This approach can appear disadvantageous in terms of SNR, however, it is preferred in an ultra-low-power receiver, because it is less onerous in terms of power consumption and die area [3]. In addition, the limited image rejection needed by this application relaxes the phase-matching requirement between I and Q paths. The quadrature generation is obtained by degenerating transistor M0 with capacitor C0 and sensing the Q signal at the source of M0 by an identical stage but operating in common-source mode thanks to the large value of the capacitor C1. While the 90° phase shift is guaranteed over a wide frequency range, the amplitude match is obtained only around the working frequency ω_0 set by $C0=gm/\omega_0$. Since the LNA acts also as the bias-current generator for the VCO, the low-frequency degeneration occurring in the quadrature scheme is used also to filter out the flicker noise contributed by M0 and M1 that could otherwise degrade the oscillator phase noise [2].

The channel selection is performed by a fully differential 3-stage variable-gain complex g_m-C filter, AC coupled at the output of the TIA to suppress DC offset and low-frequency noise. The complex poles are synthesized as shown in Fig. 20.8.4. In each stage, two g_m-C filters with a real transfer function are transformed into a complex one by adding an imaginary term realized by cross-connecting the transconductance g_{mIM} between the I and Q paths. The gain and the filtering profile depend on the ratios g_{mIN}/g_{mRE} and g_{mRE}/g_{mIM}, respectively, while the gain control and the calibration are obtained by changing the bias current of the transconductance stages. The I and Q path are finally combined as shown in Fig. 20.8.1.

The front-end is fabricated in a 90nm CMOS process. Figure 20.8.5 shows the chip micrograph. Only one integrated inductor is used, resulting in an active die area of 0.35mm² including the baseband filter. Figure 20.8.6 shows the filtering gain profile, where a maximum in-band (from 1 to 3MHz) gain of 75dB is achieved (35dB up to the TIA virtual ground). The I and Q paths matching assure a channel image rejection of 35dB, much better than the 4dB required by the standard, improving the receiver robustness [3]. The noise figure averaged over the band from 1 to 3MHz is around 12dB while the in-band IIP3 and IIP2 distortions (at maximum gain) are –12.5dBm and +12dBm, respectively. The VCO phase noise, measured at an offset of 3.5MHz from the carrier as defined by the ZigBee standard [3], is around –107.8dBc/Hz while the LO leakage at the input is below –60dBm. The total current draw is 3mA from a 1.2V supply, of which 2mA is used by the RF blocks and 1mA by the TIA and the baseband filters. In Fig. 20.8.7, the ZigBee specifications and the measurement results are reported. All targets have been met with considerable margin using a very small area and power consumption.

Acknowledgments:
The authors want to thank Andrea Baschirotto for fruitful discussion and Matteo Galli for the support in the setup of test equipment.

References:
[1] T. K. Nguyen, V. Krizhanovskii, J. Lee et al., "A Low-Power RF Direct-Conversion Receiver/Transmitter for 2.4-GHz-Band IEEE 802.15.4 Standard in 0.18-µm CMOS Technology," *IEEE Trans. Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4062-4071, Dec. 2006.
[2] A. Liscidini, A. Mazzanti, R. Tonietto et al., "Single-Stage Low-Power Quadrature RF Receiver Front-End: The LMV Cell," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2832-2841, Dec. 2006.
[3] W. Kluge, F. Poegel, H. Roller et al., "A Fully Integrated 2.4GHz IEEE 802.15.4 Compliant Transceiver for ZigBee Applications," *ISSCC Dig. Tech. Papers*, pp. 372-373, Feb. 2006.

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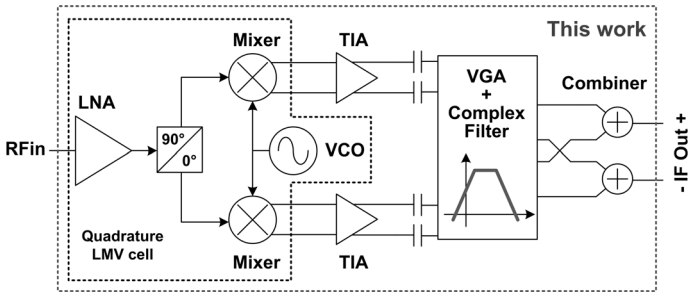

Figure 20.8.1: Block diagram of the receiver.

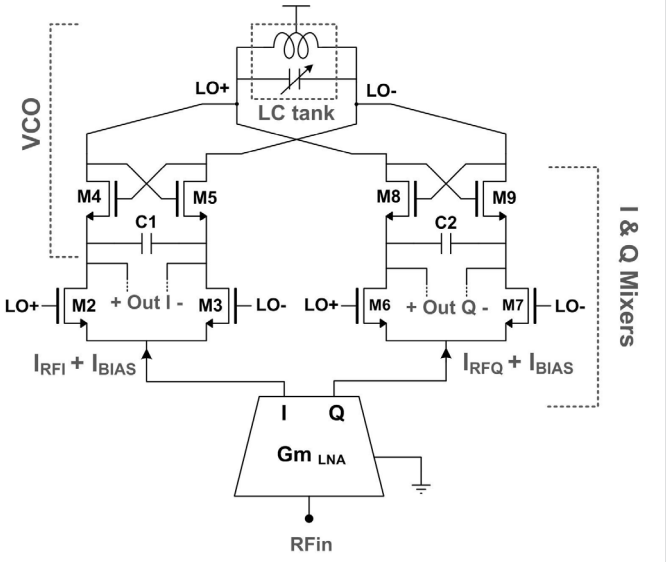

Figure 20.8.2: Single-coil quadrature LMV cell (bias not shown).

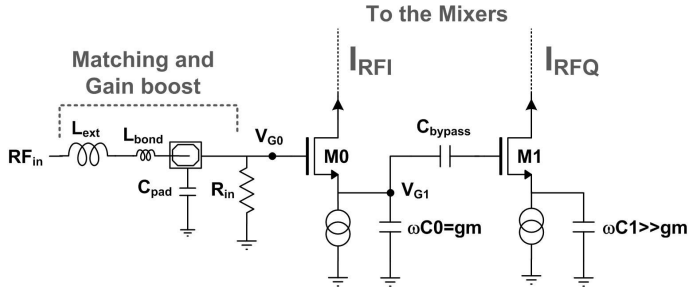

Figure 20.8.3: LNA and quadrature generation (bias not shown).

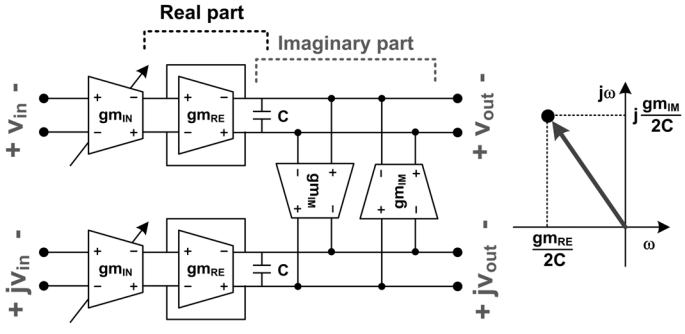

Figure 20.8.4: Block diagram of the g_m-C IF complex filter stage.

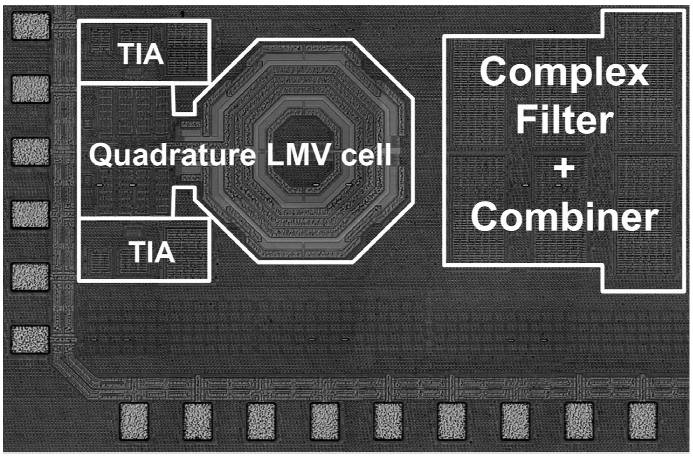

Figure 20.8.5: Chip micrograph.

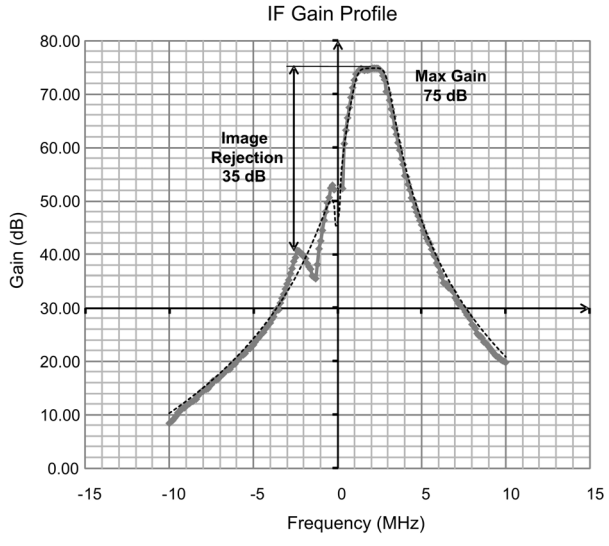

Figure 20.8.6: IF gain profile.

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Items	This Work	Specs*
Noise Figure	12 dB	<15.5 dB
Gain	75 dB	65 dB
Low IF Frequency	2 MHz	-
Image Rejection (adjacent channel)	35 dB	> 4 dB
IIP3 (high gain mode)	- 12,5 dBm	>-32 dBm
IIP2	12 dBm	>10.5 dBm
LO Phase Noise @ 3.5MHz of offset	- 107.8dBc/Hz	- 102 dBc/Hz
LO Leakage	- 60 dBm	-
S11	< -13 dB	< -10 dB
Power dissipation	3.6 mW	-
Chip Area	0.35 mm^2	-
Technology	90 nm	-

***From [3]**

Figure 20.8.7: Measured performance summary.

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