Analysis and Design of Configurable LNAs in Feedback Common-Gate Topologies

A. Liscidini, *Member, IEEE*, G. Martini, *Member, IEEE*, D. Mastantuono, *Student Member, IEEE*, and R. Castello, *Fellow, IEEE*

***Abstract*—A unified description of multiple feedback common-gate low-noise amplifiers (LNAs) is presented, providing analytical expressions for gain, noise figure, linearity, and stability conditions. Moreover, from the theory, a new methodology for LNA optimization is developed. This new approach, called *adaptive optimization*, uses the ability to reconfigure the feedback network to match the amplifier characteristics to the changing working conditions. Results of simulation of LNAs with different feedback types are shown, and they confirm the theory presented.**

***Index Terms*—Common gate, feedback amplifier, high linearity, low-noise amplifier (LNA), multiband, multistandard, negative feedback, positive feedback, reconfigurability.**

I. Introduction

CURRENT and future applications ask for reconfigurable portable terminals in a wide sense; the transceiver should adapt itself not only to different standards or frequency bands but also to different signal and blocker levels, with the constraint of minimum power consumption to increase battery life. Indeed, the usual approach to circuit design, based on worst case conditions, is not always the best choice in terms of the performance achievable under actual operating conditions. For example, in the case of a high-strength signal with low-strength blockers, the noise of the low-noise amplifier (LNA) and its nonlinearity could be downgraded by reducing the bias current without any appreciable degradation of the received signal, thus reducing overall power consumption.

The inductively degenerated amplifier, considered to be the state of the art for LNAs, appears to be increasingly inadequate to satisfy the new requirements of wide-band and easy reconfigurability asked by ultra-wide-band transceivers, universal mobile terminals, and software radios [1]–[3]. Indeed, in this topology to achieve wide-band or frequency reconfigurability implies a reduced quality factor of the input network that increases noise. Moreover, an adaptive power management of the LNA is difficult because input impedance match, noise, and linearity are strictly correlated [4].

To overcome these problems, alternative feedback structures based on common source configurations have been proposed in the literature [5], while common-gate amplifiers have been generally avoided because they are considered to be too noisy [4].

Manuscript received December 6, 2007. First published August 1, 2008; last published August 13, 2008 (projected). This work was supported by the Italian National Research Program PRIN 2005 under Project 2005093524. This paper was recommended by Associate Editor A. Demosthenous.

The authors are with the Università degli Studi di Pavia, 27100 Pavia, Italy (e-mail: antonio.liscidini@unipv.it; giuseppe.martini@unipv.it; daniele.mastantuono@unipv.it; rinaldo.castello@unipv.it).

Digital Object Identifier 10.1109/TCSII.2008.922431

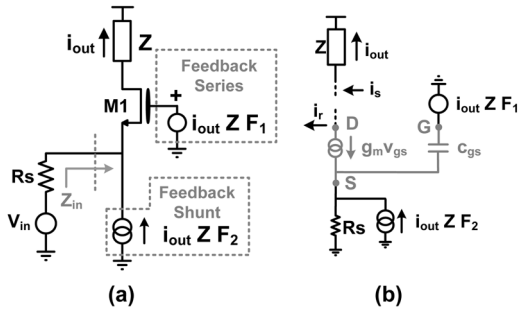

Fig. 1. (a) Multiple feedbacks around the common-gate stage. (b) Return ratio diagram.

Recently, the use of feedback [8], [9] around the common-gate stage for LNAs has been proposed, reconsidering the possibility to use such a structure even in high-performance front-ends.

In this paper, it will be shown how the new degrees of freedom provided by the use of feedback not only can improve the amplifier's performance but also offer a high level of reconfigurability that allows to exchange gain, noise, and/or linearity with power consumption. Furthermore, using a tunable narrowband amplifier with a single resonant load minimizes the complexity and the area of passive components.

The paper is structured as follows. In Section II, both series and shunt feedback networks closed around the common-gate topology are analyzed, providing a unified expression for input impedance and LNA matching condition. Successively, analytical expression for gain, noise, linearity, and stability conditions are derived, focusing on their fundamental limits. In Section III, a new design methodology that allows us to optimize the performance of the LNA by reconfiguring the feedback networks is presented. Finally, simulations results and conclusions are reported in Sections IV and V, respectively.

II. Common-Gate Multiple-Feedback Networks

The type of feedback configurations considered in the following analysis are reported in Fig. 1(a). In particular, F_1 is a voltage (series) feedback returned to the gate (negative for $F_1 > 0$), while F_2 represents a current (shunt) feedback returned to the source (positive for $F_2 > 0$). The output of the system is taken as the current flowing through the load Z, making the amplifier transfer function as a transconductance.

Contrary to the classical feedback description, based on the loop gain, the analysis will describe all circuit properties in terms of *return ratio* (RR) [10], [11]. This approach has been preferred because it provides a single expression for the input impedance, for both shunt and series feedback. In addition, the

return ratio allows us to study the amplifier stability in the presence of multiple feedback loops and to model bidirectional paths between input and output [12].

As explained in [10] and [11], the circuit is divided into two main parts [Fig. 1(b)]: the controlled device (in gray) and the feedback portion (in black). Neglecting the gate–source capacitance (assuming a transistor f_T much higher than the working frequency), RR has the following expression:

$$\mathrm{RR} = -\frac{i_r}{i_s} = \frac{g_m Z(s)}{1 + g_m Rs}(F_1 - F_2 Rs) \tag{1}$$

where g_m is the transistor's transconductance and Rs is the driving resistance. The first term in (1) represents the series feedback and the second one represents the shunt feedback. In addition, the source resistance Rs acts intrinsically as a series feedback for a common-gate topology, as it is a degeneration for the input transistor [8].

A. Input Impedance and Matching Condition

The input impedance of the multiple-loop LNA can be evaluated (independently of the feedback used) by the return ratio and the Blackman's formula [13] as

$$Z_{\mathrm{in}} = Z_{\mathrm{in_{open}}} \frac{1 + \mathrm{RR}|_{rs=0}}{1 + \mathrm{RR}|_{rs=\infty}} = \frac{1}{g_m} \frac{1 + F_1 Z(s) g_m}{1 - F_2 Z(s)} \tag{2}$$

where $Z_{\mathrm{in_{open}}}$ is the input impedance of the circuit with all of the loops broken, and it is equal to $1/g_m$. When $F_1 > 0$, the input impedance increases compared with the common-gate topology and the same is obtained for $F_2 > 0$. On the contrary, reversing the sign of the two feedbacks, the input impedance decreases.

Equation (2) hints at the possibility of reconfiguring the input impedance acting on F_1, F_2, and $Z(s)$. In particular, the dependence of Z_{in} on the load $Z(s)$ provides a way to obtain a narrowband configurable LNA by shaping in frequency the load impedance [8], [9]. A reconfigurable input-filtering profile is useful especially in multistandard system where both received and interferer signals change their frequency locations.

The LNA's matching condition is derived from (2) when $Z_{\mathrm{in}} = Rs$. This forces the transistor's transconductance to be

$$g_m = \frac{1}{Rs - (F_1 + F_2 Rs) r} \tag{3}$$

where R is the value of $Z(s)$ in the LNA passband. Notice that, since for a given R the couple (F_1, F_2) sets the value of the transconductance, the power consumption of the LNA is also uniquely defined.

The matching condition expressed by (3) imposes two bounds on the value of F_1 and F_2 as

$$\begin{cases} \frac{R}{Rs} F_1 + R F_2 < 1 \\ R F_2 < 1. \end{cases} \tag{4}$$

The first one is due to the finite value of the transistor's transconductance, while the second comes from the stability condition, as will be discussed in the next section. Since in-band input matching is required for proper operation, in the following we will assume that (3) is always verified.

B. Stability

Even for a multiloop topology, the amplifier stability can be evaluated from the gain/phase margin of the return ratio since there exists a single point that breaks all of the loops at the same time [12].

For $F_1 > F_2 Rs$, we have that $\mathrm{RR} > 0$ and the two feedbacks act like a single negative one. Two cases are possible:

1) *Negative feedback with* $0 < \mathrm{RR} < 1$. If $F_1 R < Rs$, we have $\mathrm{RR} < 1$ in band. If the maximum gain is obtained in the LNA working band (typical case), the amplifier is then unconditionally stable.
2) *Negative feedback with* $\mathrm{RR} > 1$. For these cases, the stability can be evaluated looking at the phase margin and can be guaranteed with a proper choice of $Z(s)$. For example, in reconfigurable narrowband LNA, the high selectivity provided by an *LC*-tank generally gives an adequate phase margin.

For $F_1 < F_2 Rs$, we have $\mathrm{RR} < 0$ and a positive feedback occurs. Again, two cases are possible:

3) *Positive feedback with* $-1 < \mathrm{RR} < 0$. In the presence of a positive feedback, the amplifier is stable if $\mathrm{RR} > -1$. This can be guaranteed setting $F_2 R < 1$ in (1), with a safe margin to take into account process variation. In Appendix I, the RR sensitivity to the main circuit parameters is computed.
4) *Positive feedback with* $\mathrm{RR} < -1$. In this case, the system is unstable.

C. Transconductance Gain

The common-gate amplifier usually suffers from a poor transconductance gain, here defined as Gm. This happens because the transistor is used as a simple input termination, so that its Gm is forced to be equal to $1/Rs$. When using feedback, the LNA gain is modified as follows:

$$Gm = \frac{i_{\mathrm{out}}}{v_{\mathrm{in}}} = \frac{1}{2Rs(1 - F_2 R)}. \tag{5}$$

If no feedback is used, (5) gives the gain of a common-gate stage, i.e., Gm equal to $1/2Rs$. The same result is obtained if only F_1 is used ($F_2 = 0$), since the current provided by the source goes directly to the output without any amplification. On the contrary, using F_2 the Gm can be modified as a consequence of adding a new current path at the input. Thus, when a high Gm is wanted, a shunt positive feedback should be used.

D. Noise Figure

Noise analysis is performed assuming noiseless feedback networks, accounting only for the noise sources arising from the gain device, plus thermal noise of the load (R for in-band signals in resonance condition). Under these assumptions, the noise figure is given by the following equation:

$$\mathrm{NF} = 1 + \frac{\gamma}{g_m Rs} + \frac{Rs}{R}\left(1 + \frac{1}{g_m Rs}\right) \tag{6}$$

where γ is the noise parameter of the MOSFET, usually ranging from 2/3 up to slightly more than 1. The second term on the

right-hand side of (6) accounts for the MOSFET channel noise, and the third term accounts for the load thermal noise.

The noise figure given by (6) does not explicitly depend on the amount of feedback applied; however, the presence of feedback changes the NF through a change in g_m according to (3) as shown in the following equation:

$$\mathrm{NF}_{\mathrm{match}} = 1 + \gamma\left(1 - \frac{R\cdot F_1}{Rs} - F_2 R\right) + \frac{Rs}{R}\left(2 - \frac{R\cdot F_1}{Rs} - F_2 R\right)^2 \quad (7)$$

where the dependence on feedback is explicit. The second and third terms in (7) have the same origin of the corresponding term in (6), while the noise figure of the simple common-gate LNA is given when F_1 and F_2 are set to zero. The noise figure can be higher or lower compared with the common-gate amplifier, depending on the sign of the feedbacks. In particular, for positive F_1 and F_2, $\mathrm{NF}_{\mathrm{match}}$ is lower than that for the common-gate one.

E. Linearity

Assuming the feedback networks are linear, the distortion depends on the transistor operating point and on the effects of the feedbacks on the gate–source voltage swing (V_{GS}) [9].

The two feedbacks act differently on V_{GS} to satisfy the matching condition. In particular, F_1 forces $V_{\mathrm{GS}} = V_{\mathrm{in}}/(2g_m Rs)$ while F_2 forces V_{GS} to be equal to $V_{\mathrm{in}}/2$. Therefore, for a given overdrive, only F_1 influences the amplifier linearity since F_2 does not affects the gate–source voltage swing. On the other hand, for a given bias current, the transistor overdrive is defined by (3) and the relationship $I/gm = V_{\mathrm{ov}}/2$ making the linearity dependent also on F_2.

The IIP3 for the three cases considered—simple common-gate (IIP3CG) series feedback (IIP3F1) and shunt feedback (IIP3F2)—have been computed using Sansen's theory [14] and the coefficients of the V–I transistor characteristic (in strong inversion) defined in [9], obtaining

$$\begin{cases} \mathrm{IIP3}_{\mathrm{CG}} = \left|\frac{16V_{\mathrm{ov}}^2(2+\theta V_{\mathrm{ov}})}{3Rs}\right| \\ \mathrm{IIP3}_{F1} = \mathrm{IIP3}_{\mathrm{CG}}\left|\frac{(1+G_{\mathrm{loop}})^4(1+\theta V_{\mathrm{ov}})^2}{1-(1+G_{\mathrm{loop}})(1+(1+\theta V_{\mathrm{ov}})^2)}\right| \\ \mathrm{IIP3}_{F2} = \mathrm{IIP3}_{\mathrm{CG}} \end{cases} \quad (8)$$

where θ is a fitting parameter. For a given overdrive voltage V_{ov}, the $\mathrm{IIP3}_{F1}$ is approximately equal to the $\mathrm{IIP3}_{\mathrm{CG}}$ time $|1 + \mathrm{Gloop}|^3$, since the modulation of the gate–source voltage is inversely proportional to the loop gain [8]. On the contrary, when F_2 is applied, IIP3F2 has the same expression as $\mathrm{IIP3}_{\mathrm{CG}}$, as predicted by the qualitative analysis. On the other hand, for a constant bias current, the proper overdrive (different in the three cases) should be used in each expression.

III. LNA and Adaptive Optimization

In the previous section, it was shown that, assuming constant overdrive, the two feedback networks control, respectively, one design parameter, without affecting the other one (i.e., F_1 acts on the linearity while F_2 on the gain). It follows that, acting on F_1 and F_2, the amplifier can be simply optimized to reach the desired performance. This flexibility leads to the development of a new design strategy which aims at satisfying different scenarios by reconfiguring the receiver in real time.

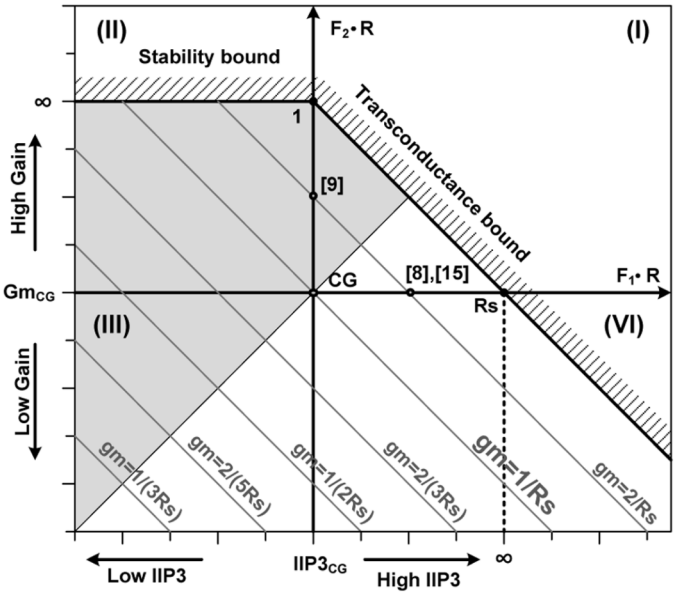

Fig. 2. Feedbacks plane: F_1, F_2 versus gain, IIP3, and g_m. Global positive feedback, $\mathrm{RR} < 0$ (gray zone).

A. Feedbacks Plane

For a given overdrive voltage, the equations derived in the previous sections allow to draw the diagram of Fig. 2. On this plot, the effects of $F_1 \cdot R$ and $F_2 \cdot R$ on Gm (5) and IIP3 (8) are shown explicitly, while the effect on NF follows indirectly through the value of g_m drawn on the figure in parametric form (6). In the figure, gain and IIP3 are normalized to those of the common-gate amplifier CG. The diagram is completed with the forbidden region derived from (4), i.e., the transconductance bound corresponding to a transistor g_m equal to infinity and the stability bound that imposes $F_2 \cdot R < 1$. In gray, the portion of the plane is shown where $F_2 Rs > F_1$, corresponding to an overall *positive stable* feedback as discussed previously.

By exploring all of the configurations in the plane $(F_1 \cdot R, F_2 \cdot R)$, it is possible to exchange performance with power consumption. In particular, when F_1 and F_2 are both positive, the amplifier properties are all improved as compared with the common-gate amplifier, at the cost of a larger power consumption. On the contrary, when F_1 and F_2 are both negative, a lower g_m is required, reducing power consumption, but also gain and linearity, and increasing the noise figure.

The diagram and the previous equations provide a methodology for the design of feedback common-gate LNA summarized in the following steps.

Step 1) Starting from a target noise figure NF and transconductance gain Gm, g_m and F_2 are set from (6) and (5), respectively.

Step 2) Then, the value of F_1 is unequivocally derived from the matching condition (3) or from the diagram in Fig. 2.

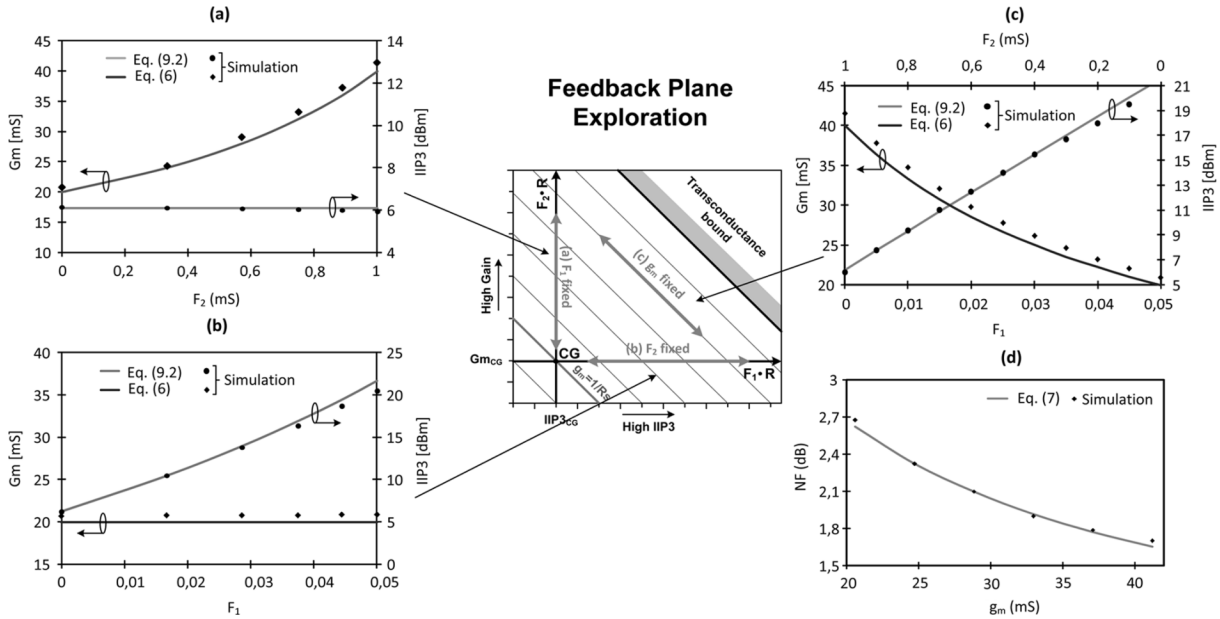

Fig. 3. Feedback reconfiguration theory versus simulations. (a) F_1 fixed. (b) F_2 fixed. (c) g_m fixed. (d) Noise figure versus MOSFET transconductance.

Step 3) Finally, the desired IIP3 can be obtained acting on $V_{\rm ov}$ by changing the transistor aspect ratio and bias current while keeping g_m constant.

In conclusion, to enhance system linearity, a series feedback has to be used, (see [8], [15] in Fig. 2), while, for a gain greater than the common gate one, a shunt positive feedback is needed (see [9] in Fig. 2).

B. Adaptive Optimization

Such a performance reconfiguration, obtained by acting on the feedback networks, suggests a new approach in the way the LNA is utilized within a wireless receiver which aims at satisfying in real time the required specifications by dynamically exploring the diagram of Fig. 2. We call this new approach *adaptive optimization* as opposed to the traditional static optimization that wants to satisfy always the worst case scenario although it has a low probability to be verified. Avoiding to the target worst case requirement, this new methodology goes towards significant power saving. Notice that using reconfiguration to follow the changes in environment condition can be done without corrupting the received signal, since the variations occur with time constants that are significantly longer than those of the signal.

Furthermore, reconfiguring the load impedance Z (by changing its frequency response) provides a way to shape the frequency selectivity of the amplifier [8], [9]. A dynamic input filtering profile is useful especially in multistandard system where both received and interferer signals change their frequency locations.

IV. Simulation Results

The theory presented has been verified through the simulations of a multiple feedback LNA in a 90-nm CMOS TSMC. The amplifier was simulated using a BSIM 4.0 transistor models, with a power supply of 1.2 V and an *LC* output load centered at 2 GHz with a resistance of 500 Ω at resonance. The results in Fig. 3 show good agreement with the theory under the assumptions defined in Section II (linear and noiseless feedback networks).

For a fixed voltage overdrive, the *feedback plane* has been explored along the axes and moving on an iso-g_m curve with $g_m = 40$ mS that corresponds to a constant power design (Fig. 3). As predicted by the theory, the transconductance gain Gm and IIP3 can be controlled separately [see Fig. 3(a) and (b)] while under the power constraint gain and linearity trade with each other [see Fig. 3(c)]. To complete the simulations, the LNA's noise figure dependency on the MOSFET transconductance g_m has been verified [Fig. 3(d)].

To evaluate the impact of the feedback nonidealities on the LNA performance, a possible implementation for F_1 and F_2 was considered (Fig. 4). F_1 is implemented by a noiseless capacitive divider while F_2 is implemented by a pMOS transistor pair. A cascode stage has been added to minimize the effect on F_1 of the finite output resistance and of the gate-to-drain parasitic capacitance of M1 (M4).

While the feedback network F_1 can still be considered linear and noiseless, the introduction of cascode M2 (M5) and the use of pMOS transistor M3 (M6) to implement F_2 affect the noise and linearity of the amplifier. However, if M3 (M6) is designed with a large overdrive and a small g_m, the extra noise and distortion introduced are small [9].

The reconfigurability of the system is obtained by acting on the capacitors and the pMOS bias. Table I reports the simulation results for the circuit in Fig. 4 for different power consumption (4–8 mW) and feedback configuration. The noise figure is about 0.5 dB higher compared with the results reported in Fig. 3 due to the additional noise sources. Although the IIP3 is about 4 dB lower compared with the theory (due to the nonidealities introduced), its trend as a function of F_1 and F_2 is correctly predicted. The maximum gain reaches 26 dB with a $Gm = 40$ mS and an equivalent $R = 500\ \Omega$ acting on F_2.

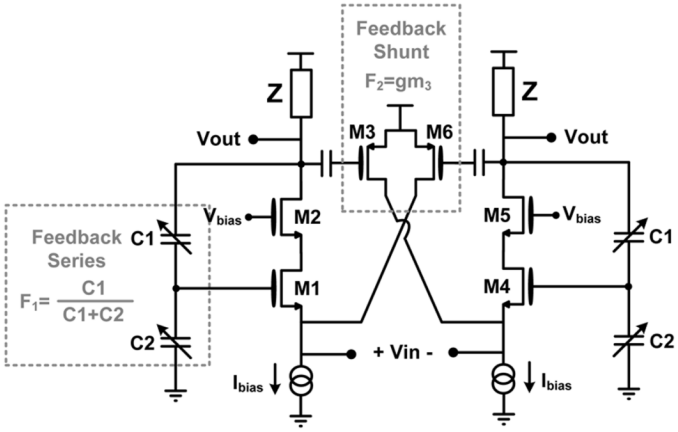

Fig. 4. Configurable double feedback LNA (bias not shown).

TABLE I
LNA PERFORMANCE

	Low Power	*High IIP3*	*High Gain*
Power (mW)	**4**	8	8
Gm (mS)	20	20	**40**
NF (dB)	3.4	**2.2**	**2.2**
IIP3 (dBm)	5	**16**	3
Gain (dB)	20	20	**26**

V. CONCLUSION

The analysis developed concentrates on the common-gate LNA topology and has shown the benefits that the feedback (positive or negative) can produce on it, i.e., noise figure reduction, linearity improvement, frequency response, and performance reconfigurability. Moreover, a new design approach called *adaptive optimization* has been introduced, where a dynamic performance reduction could produce a significant power saving. For example, in the case of a high-strength signal with low-strength blockers, the noise figure and nonlinearity can be degraded without affecting overall performance, reducing bias current and, consequently, the power consumption.

APPENDIX

The RR sensitivity to the a generic circuits parameter x can been defined as follows:

$$S_x^{\mathrm{RR}} = \frac{x}{\mathrm{RR}} \frac{\partial \mathrm{RR}}{\partial x}. \tag{9}$$

The RR sensitivities to g_m, F_1, F_2 were evaluated for $|\mathrm{RR}|$ close to unity, where a possible spread of the process could increase the gain causing instability. In particular, the following results were obtained:

$$S_{g_m}^{\mathrm{RR}} \frac{1}{1+g_m Rs} \tag{10}$$

$$S_{F_1}^{\mathrm{RR}} \frac{F_1}{F_1 - F_2 Rs} \overset{\mathrm{RR}\to 1}{\Longrightarrow} \cong F_1 \frac{g_m R}{1+g_m Rs} \tag{11}$$

$$S_{F_2}^{\mathrm{RR}} \frac{F_2 Rs}{F_1 - F_2 Rs} \overset{\mathrm{RR}\to 1}{\Longrightarrow} \cong F_2 Rs \frac{g_m R}{1+g_m Rs}. \tag{12}$$

The sensitivity of RR to the input transconductance $g)m$ is always lower than 1 and decrease as $g)m$ increases. On the other hand, (11) and (12) show that the sensitivity to F1 and F2 is lower than one choosing $|F_1 R| < Rs$ and $|F_2 R| < 1$, respectively. The latter condition is always verified in the first quadrant where all the performance (IIP3 and Gain, NF) are improved compare to the common gate. For all cases, the sensitivity to the load R is equal to 1.

REFERENCES

[1] S. Roy, J. R. Foerster, V. S. Somayazulu, and D. G. Leeper, "Ultrawideband radio design: The promise of high-speed, short-range wireless connectivity," *Proc. IEEE*, vol. 92, no. 2, pp. 295–311, Feb. 2004.

[2] E. Duvivier *et al.*, "A fully integrated zero-IF transceiver for GSM-GPRS quad-band application," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2249–2257, Dec. 2003.

[3] H. Hashemi and A. Hajimiri, "Concurrent multiband low-noise amplifiers-theory, design, and applications," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 1, pp. 288–301, Jan. 2002.

[4] D. K. Shaeffer and T. H. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, no. 5, pp. 745–759, May 1997.

[5] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Wide-band CMOS low-noise amplifier exploiting thermal noise canceling," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 275–282, Feb. 2004.

[6] S. Chehrazi, "A 6.5 GHz wide-band CMOS low noise amplifier for multi-band use," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2005, pp. 315–318.

[7] L. Xiaoyong, S. Shekhar, and D. J. Allstot, "Gm-boosted common-gate LNA and differential colpitts VCO/QVCO in 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.

[8] P. Rossi, A. Liscidini, M. Brandolini, and F. Svelto, "A variable gain rf front-end, based on a voltage-voltage feedback LNA, for multistandard applications," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 690–697, Mar. 2005.

[9] A. Liscidini, M. Brandolini, D. Sanzogni, and R. Castello, "A 0.13 μm CMOS front-end for DCS1800/UMTS/802.11b-g with multi-band positive feedback low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 981–989, Apr. 2006.

[10] H. W. Bode, *Network Analysis and Feedback Amplifier Design*. New York: Van Nostrand, 1945.

[11] P. J. Hurst, "A comparison of two approaches to feedback circuit analysis," *IEEE Trans. Education*, vol. 35, no. 3, pp. 253–261, Aug. 1992.

[12] P. J. Hurts and S. H. Lewis, "Determination of stability using return ratios in balanced fully differential feedback circuits," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 42, no. 12, pp. 805–817, Dec. 1995.

[13] R. B. Blackman, "Effect of feedback on impedance," *Bell Syst. Tech. J.*, vol. 23, pp. 269–277, Oct. 1943.

[14] W. Sansen, "Distortion in elementary transistor circuits,," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 3, pp. 315–325, Mar. 1999.

[15] G. Cusmai, M. Brandolini, P. Rossi, and F. Svelto, "A 0.18-um CMOS selective receiver front-end for UWB applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1764–1771, Aug. 2006.