Time to Digital Converter based on a 2-dimensions Vernier architecture

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***Abstract*— A novel 2-dimension Vernier Time to digital converter (TDC) is presented. The proposed architecture reduces drastically the number of delay stage required by linear TDCs minimizing the power consumption and the area of the design. A 7bits TDC prototype realized in 65nm CMOS technology is presented. The chip has a resolution of 4.8ps with a power consumption of 1.7mW at a conversion rate of 50Msps.**

I. Introduction

Time to digital converters are commonly used in a wide range of applications, especially in physic measurement setup, more recently they have appeared in digital frequency synthesizers for wireless communications [1]. In such kind of applications, the time resolution provided by self-loaded inverters not always satisfies the requirements and thus new solutions based on Vernier algorithm and others interpolation techniques were investigated [2-7].

The scheme of a classic Vernier TDC is shown in Fig. 1[2]. The converter is realized starting from two delay lines formed by stages with a delay of τ_1 and τ_2 so that τ_1-τ_2=Δ, where Δ is the TDC resolution. The two lines are connected to a series of flip-flops which stores a 1 or a 0 depending if the rising edge of the reference arrives before or after that of the signal one. Actually, a signal edge, which lags a reference edge by $n\Delta$ at the input of TDC, will be lined up with it after n stages producing a thermometric code at the flip-flop outputs. (Fig. 1). In practice, such kind of TDC works as traditional ADC flash where the delay lines creates a set of time references and the flip-flops are used as time comparators.

Several modified linear Vernier architectures proposed in literature try to increase resolution and/or reduce power consumption by interpolation techniques [4] or exploiting the periodicity of the input signals [5]. However in all cases, the number of stages grows exponentially with the number of bits and with it the jitter noise and the sensitivity to mismatches. The TDC presented in this paper wants to reduce drastically these problems acting on the generation of the time references through a 2-dimensions (2-D) Vernier approach. This reduces significantly the length of delay lines required for a given full-scale.

The paper is structured as follow: in section II the 2-D Vernier algorithm is presented. In section III the TDC circuit implementation is reported and finally, in section IV, the measurement results of the TDC prototype are shown and compared with the state of art.

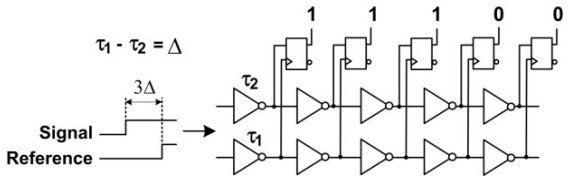

Fig. 1 Classic linear Vernier

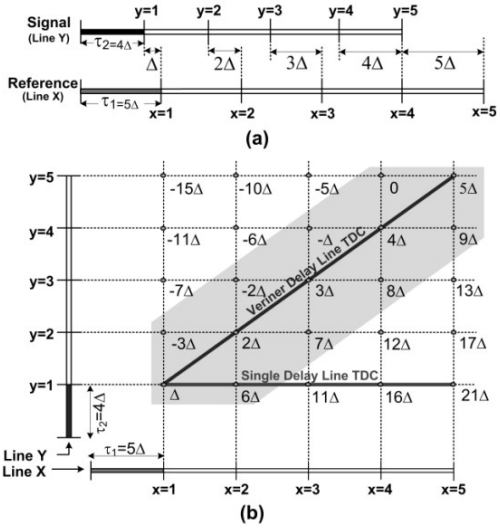

Fig. 2 Time quantization: (a) linear Vernier, (b) 2-D Vernier

II. From Linear to 2-D Vernier TDC

In the linear Vernier drawn in Fig. 1, the time quantization is realized by taking the time differences only between taps located in the same position of the two delay lines (Fig. 2.a). If all possible differences between the taps are used, the plane of time references (named *Vernier plane*) can be built, where the number of quantization levels is given by the product of the elements of two delay lines (Fig. 2.b). An immediate consequence of this 2-D solution is a potential improvement of the TDC range, since the uniform quantization provided by the linear Vernier (form Δ to 5Δ) is extended to the range from -3Δ to 9Δ (grey zone). In the following it will be shown that an even higher efficiency in the use of the time references

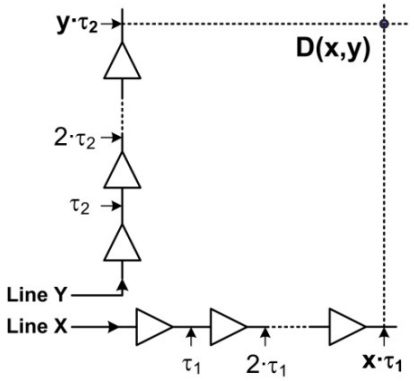

Fig. 3 Generic Vernier Plane

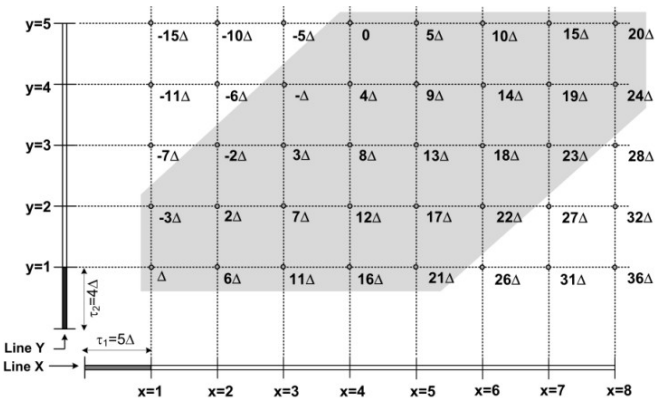

Fig. 4 Extension of Vernier plane

generated can be obtained exploring a wider region of the *Vernier plane*.

Notice that, the structure proposed can be considered as a generalization of the delay line [1] and of the linear Vernier TDC [2], which lie respectively on the borders and on the diagonal of the plane in Fig. 2.b.

A. From the Vernier plane to a 2-D TDC

To realize a time to digital converter, the set of time references generated in the *Vernier plane* (Fig. 3) must be arranged into a vector to obtain an ordered set with a constant quantization step Δ (i.e. the final TDC resolution). This operation is performed by a function $i=i(x,y) \in \mathbb{N}$ that associates the position i in the vector with the coordinates (x,y) of the *Vernier plane* so that

$$D(x,y) = x \cdot \tau_1 - y \cdot \tau_2 = i\Delta \qquad (1)$$

where $D(x,y)$ is the delay associated with the position (x,y). The function $i(x,y)$ depends on the choice of τ_1 and τ_2 and can be found dividing (1) by Δ :

$$i(x,y) = x\frac{\tau_1}{\Delta} - y\frac{\tau_2}{\Delta} \qquad (2)$$

Notice that the existence of $i(x,y)$ in $\mathbb{N}$ is guaranteed only by the assumption that both τ_1 and τ_2 are multiple of Δ. Indeed, starting from the Bezout's identity [9], it can be proved that the resolution Δ is always equal to the Greatest Common Divider (GCD)[1] between τ_1 and τ_2.

A particular family of 2-D *Vernier plane* is given by the set $\tau_1=k\Delta$, $\tau_2=(k-1)\Delta$ (e.g. 5Δ and 4Δ as shown in Fig. 2), where $GCD(\tau_1,\tau_2)=\tau_1-\tau_2=\Delta$ and the linear and the 2-D TDC are equivalent in terms of resolution. In all the other cases, it's easy to prove that the 2-dimension TDC has a time resolution always smaller then the linear Vernier. (e.g. $\tau_1=5\Delta$ and $\tau_2=3\Delta$ still have a GCD $=\Delta$ but their difference is 2Δ).

B. Uniform quantization with finite delay lines

Equation (2) assures a uniform mapping of the *Vernier plane* only if no boundary are set for the (x,y) domain. Unfortunately, when finite delay lines are used, the generated plane cannot assure a uniform quantization of the entire co-domain i (e.g. in the plane of Fig. 2, 10Δ, 14Δ and other values are missing).

The region of the plane (X,Y) that corresponds to a uniform quantization for the co-domain i can be found inverting (2). Unfortunately, this operation is not trivial since $i=i(x,y) \in \mathbb{N}$ is not biunique. In the following, only the class of *Vernier planes* with $\tau_1=k\Delta$, $\tau_2=(k-1)\Delta$ will be studied, so that (2) can be rewritten as

$$i = xk - (k-1)y \qquad (3)$$

Assuming $y \in [1,k]$, this equation can be inverted obtaining

$$\begin{cases} x(i) = i - \left\lceil \frac{i-1}{k} \right\rceil (k-1) \\ y(i) = i - \left\lceil \frac{i-1}{k} \right\rceil k \end{cases} \qquad (4)$$

where $\lceil a \rceil$ is the upper integer of a. As indicated in the example of Fig. 2 with k elements for both lines, a uniform quantization can be obtained only in the range between $-k+2$ and $2k-1$.

C. Extension of the Vernier plane

From (4) it is possible to verify that, while $y(i)$ is periodic and varies between 0 and k, $x(i)$ exceeds k, for $i > 2k-1$. This suggests that it is possible to extend the TDC range increasing only one of the two delay lines. An example of this is reported in Fig. 4 where the TDC range of Fig. 2 has been extended from 9Δ to 24Δ with the addition of only 3 delay stages. Actually, the use of a 2-dimensions approach significantly reduce the length of the delay lines compared to a linear Vernier. In fact, the number of stages required for N quantization levels is proportional to $\sqrt{N}$ instead of N.

Since the power consumption in a Vernier TDC is dominated by the delay stages, a 2-D approach results in a better power efficiency with the respect to a linear solution. Furthermore, the use of shorter delay lines reduces also the integral non linearity caused by mismatches between the delay stages. In particular, observing the *Vernier plane* in Fig. 4, it can be seen that the entire range is folded with a periodicity equal to 5 (i.e. k) which limits the integration of the distortion

[1] Notice that the GCD can be also defined in the time domain being it a commutative ring [9].

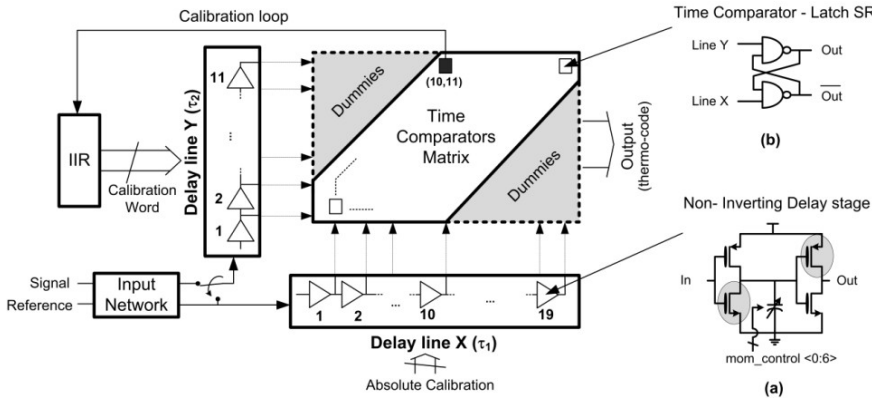

Fig. 5 2-D Vernier TDC circuit implementation (a. Delay stage, b. Time comparator)

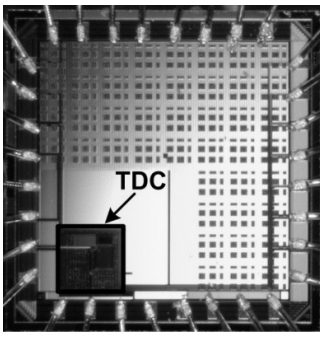

Fig. 6 TDC Microphotograph

for higher output codes. Notice that such kind of folding occurs only for the delay sets $\tau_1=k\Delta$, $\tau_2=(k-1)\Delta$, while other combination of delays generates *Vernier planes* with different quantization level distributions.

III. TDC CIRCUIT IMPLEMENTATION

To validate the theory just presented, a 7-bit TDC was designed and implemented. In particular a *Vernier plane* with 11 stages for line Y (i.e. k=11) and 19 stages for line X was built, resulting in 119 quantization levels, from -9Δ to +109Δ. The target resolution of Δ=5ps sets τ_1=55ps and τ_2 =50ps giving a TDC full scale of 590ps, from -45ps to 545ps.

The 2-D Vernier TDC circuit is shown in Fig. 5. The core is constituted by the two delay lines and the matrix of time comparators (one for each time reference). To provide a better symmetry, the delay lines were realized by non-inverting delay stages in order to perform the digital conversion only on rising edges. Furthermore, since not all the generated time references are used for the conversions (see Fig. 4), to provide the same capacitive load to all the stages of the delay lines, dummies time comparators were inserted at the corners of the matrix (grey zone). In the test chip, an additional input network was added to square the input signals coming from outside the chip.

A. The delay element and the time comparator

The non-inverting stage was realized through a cascade of two CMOS inverters (Fig. 5.a). Since the TDC works only on rising edge the critical transistors are the n-MOS of the first inverter and the p-MOS of the second one. In particular the second inverter has to be able to drive the matrix latches and the following delay stage.

To guarantee proper operation in presence of mismatches, process and temperature variation, the value of the delay of each stage can be calibrated by a 7-bit array of MOM (metal-oxide-metal) capacitors which gives a time granularity of 1ps. In order to mitigate the effects of mismatches on the linearity of the delay lines, the physical placement of the elementary MOM cell has been done according to the common centroid criterion.

The time comparator was realized using a SR latch (Fig. 5.b) which minimizes systematic *time skew* thanks to its perfect symmetry. Furthermore this structure is very compact and this feature is highly desirable since the matrix uses a huge number of comparator organized in a bi-dimensional architecture.

B. Calibration loop

While the value of the delay present in the X line (i.e. τ_1) is controlled in open loop, the correct ratio between the delays τ_1 and τ_2 is set using a delay locked loop (DLL) built-in in the matrix. Actually, during the calibration phase the reference signal is fed to both lines and the latch at the position (10,11) (the black one in Fig. 5) is used to estimate the delay difference between 10 stage of the X line and 11 stages of the Y line. The signal coming out from the latch is integrated by a IIR (infinite impulse response) and the filter output is used to control the values of the elements of the line Y. In steady state, the loop converge to the value of the digital control word that forces $10\tau_1=11\tau_2$.

IV. MEASUREMENTS RESULTS

The microphotograph of the TDC test chip, fabricated in 65nm Low Power standard CMOS technology by TSMC, is reported in Fig. 6. The active area of the TDC is 260um x 260um dominated for more than 2/3 by the digital part used for chip control and post processing.

All the measurement results are done for a 1.2V of voltage supply and a 100MHz clock. The TDC performs 50Msample/s measurements but the double clock allows to interleave the calibration with the measurements. Since the bandwidth of the calibration loop is very small, it is not necessary to calibrate the chip after each measurement but this solution was chosen for simplicity.

The TDC has been tested injecting at its inputs two signals provided by a Data Timing Generator (Tektronix DTG5274) able to generate square waves with edges slope of 5 GV/s and a variable phase difference. The entire TDC characteristic was explored generating a phase ramp between the two signals with a constant slope.

The TDC resolution was measured by tuning the capacitors banks present in the X delay line, while the Y line was set by the calibration loop, and it was found to vary from 4.8ps to 7.9ps. At the resolution of 4.8ps the power consumption for

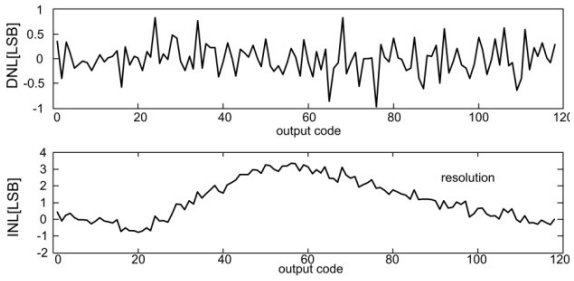

Fig. 7 DNL and INL measurements @ 4.8ps of resolution

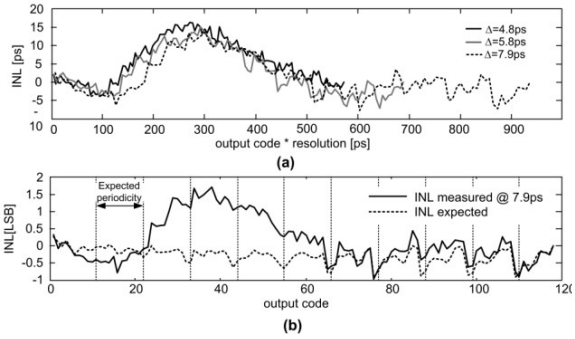

Fig. 8 INL measurements for different gain (a) and TDC intrinsic INL extrapolation (b)

the conversion phase was 1.7mW (1.1mW dissipated by the delay stages).

The integral and differential non linearities (INL and DNL) were evaluated for a resolution of 4.8ps by a data processing based on the histogram method (Fig 7). The DNL is always less the one LSB while the INL shows a bump with a maximum of 3.3 LSB. The big bump present in the INL measure is incompatible with the folding existing in the proposed architecture, that should produce a periodicity in the INL. This problem was investigated performing further measurements at different TDC resolutions (Fig. 8.a). These measurements show an invariance with respect to resolution of both the bump height and its position in time (300ps). From this we concluded that the bump is not caused by the quantization process but it is generated before entering in the TDC core. We believe that when the rising edges of the input signals are very closed to each other, and not yet well squared, a cross-talk through the power supply in the input network generates a pulling which distorts the phase ramp. Fig. 8.a shows also that this pulling effect become negligible for delays higher than 500ps. For this reason, to evaluated the intrinsic TDC INL, the measure was done at a resolution of 7.9ps that extends the TDC range to a zone where the phenomena is negligible. In this region the INL is below one LSB and the expected INL periodicity due to the folding (11 codes) appears.

A summary of the measured results, compared with those of other solutions, are reported in Table I. The architecture proposed shows the lowest power consumption (1.7mW). Referring to the FoM used in [8], the 2-D Vernier provides 0.28pJ/step, which is overcome only by the Gated-Ring Oscillator (GRO) TDC [8]. However the GRO approach has an inferior bound in the power consumption since the gated

TABLE I
MEASUREMENT RESULTS AND STATE OF ART

	This work	[1]	[2]	[5]	[6]	[8]
# of bits	7	6	7	6	9	11
Delay stages /step	0.26	1	2	1	0.1	n.a.
Resolution [ps]	4.8	17	30	12	1.25	1.2***
INL [LSB]	3.3 (<1*)	0.7	1	1.15	2	-
DNL[LSB]	<1	0.7	-	1	0.8	-
Bandwidth [MHz]	50	26	130	40	10	1
Area [mm^2]	0.02**	0.01	10	0.04	0.06	0.04
Supply Voltage [V]	1.2	1.3	5	1.2	1	1.5
Power dissipation [mW]	1.7	1.8	-	2.5	3	2.2-21
FoM [pJ/step]	0.28	1	-	0.96	0.58	0.23
Technology	65nm	90nm	0.7 µm	120nm	90nm	130nm

* Extrapolated TDC intrinsic INL
** TDC core
*** Equivalent overall 1MHz of bandwidth

ring oscillator requires a minimum number of cycles to perform the conversion. This limit (equal to 2.2mW in [8]) does not scale with the number of bits and it is greater than the total power drawn by TDC reported here. Among the solutions based on delay lines, the number of stages required by the 2-D Vernier is comparable only to the two steps architecture [6]. Notice also that, thanks to the shorter delay lines, the TDC core has one of the smallest area occupancy.

CONCLUSION

A novel 2-dimension TDC Vernier architecture was presented. In 2-D approach the number of stages required for N quantization levels grows with $\sqrt{N}$, resulting in a more compact and efficient solution in terms of area, power consumption and distortion.

ACKNOWLEDGMENTS

This research has been supported by the Italian National Program FIRB, contract n° RBIP063L4L. The authors want to thanks Marvell for technology access, Steve Shia (TSMC) for design kit support, Francesco de Paola for testing support and finally Francesco Rezzi and Fernando De Bernardinis for fruitful discussion.

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