2.6 3.3GHz DCO with a Frequency Resolution of 150Hz for All-Digital PLL

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In all-digital phase-locked loops (ADPLLs), the quantization noise introduced by the frequency discretization in the digitally controlled oscillator (DCO) can affect the performance in terms of out-of-band phase noise. In particular, the additional quantization noise has to be kept significantly lower than the intrinsic oscillator phase-noise, mandating a very fine frequency resolution (e.g. less than one kHz in GSM) [1]. Typically, in LC oscillators, the digital tuning is realized using two (or more) capacitor banks for coarse and fine tuning. The first bank is used to compensate process and temperature variation and to select the channel while the second is required for the DCO modulation inside the PLL. Since the coarse tuning range can be several hundred MHz (e.g. 800MHz in GSM [1]), a frequency resolution in the range of kHz can result in unitary elements for the capacitor banks of the order of atto-Farads. Although such values can be achieved by means of capacitive divider networks [2], the sensitivity to mismatches and parasitics of these solutions limit the robustness of the design. Staszewski et al. solved this problem by introducing a dithering of the 3 less significant bits of the DCO frequency control word [1]. This approach reduces considerably the equivalent DCO frequency resolution (from 12kHz to 30Hz) but, as occurs in any $\Delta\Sigma$ data converter, the quantization noise is moved to higher frequencies where generally the phase-noise specifications are more challenging. Due to this problem, the frequency of dithering must be significantly increased (225MHz) to satisfy the emission mask requirements far away from the carrier [1].

To realize very fine tuning, the existing solutions insert a circuit or a mechanism to shrink the smallest capacitive element available in the DCO tank. In this case, the idea is to move the fine-tuning bank from the tank to the sources of the switching pair, exploiting an intrinsic shrinking effect present in the structure (Fig. 2.6.1). As will be shown, this approach allows an easier design of both coarse and fine tuning banks, without any additional drawbacks on the phase-noise performance and without requiring dithering.

The capacitive degeneration introduced in Fig. 2.6.1 modifies the impedance seen at the drain of M1-M2 by adding a small reactive component in parallel to the classical negative resistance used to compensate the resonator losses. More precisely, the capacitance C at the sources of M1-M2 is reflected in parallel to the tank, reduced by a factor proportional to the square of the transistor transconductance. Since the circuit operates in a large-signal regime, the amount of shrinking has been evaluated using a small signal time variant analysis [3], where the MOS transconductance g_m was averaged over a time interval equal to one period of the oscillation frequency $2\pi/\omega_0$ (high order harmonics were neglected for simplicity). Under these assumptions, the real and imaginary components of the admittance Y in parallel to the tank were calculated and plotted in Fig. 2.6.1. For $g_m << 2\omega_0 C$ the admittance Y can be approximated as:

$$Y = -\frac{gm}{2} - j\omega_0 C \frac{g_m^2}{(2\omega_0 C)^2} \quad (1)$$

where the real part is the classical negative conductance that compensates tank losses, while the imaginary part is equal to the capacitor C shrunk by a factor $-g_m^2/(2\omega_0 C)^2$. As an example, assuming g_m=10mS, C=5pF and ω_0=3.6GHz, the capacitor shrinking factor is about 500. This means that adding a capacitor of 5fF at the sources of M1-M2 produces the same effect as adding a capacitor of 10aF in parallel to the oscillator tank. It can be shown that placing a large differential capacitor at the sources of M1-M2 does not significantly affect the intrinsic phase noise of the DCO.

The value of g_m required to sustain the oscillation can correspond to a shrinking factor that makes the value of C excessively large. This problem can be solved by adopting the solution in Fig. 2.6.2 where only a fraction of the total transconductance is degenerated. In this way a degree of freedom is added in the choice of the shrinking factor, which can be programmed by varying the current I_1. Furthermore, the possibility to adjust the fine-tuning range while preserving the same resolution offers multistandard capabilities (e.g. GSM and UMTS).

To validate the theory, a DCO based on the scheme in Fig. 2.6.2 was realized with an 8b coarse array and a 13b fine array. The 3 LSBs of the coarse tuning array were substituted by a varactor to be able to include the DCO in an analog PLL during some testing phases. However the capacitive load required by the fully-digital implementation was preserved. The fine-tuning bank was realized as depicted in Fig. 2.6.3. The 8 most significant bits (MSBs) were used to control a matrix of 16×16 varactors. All elements except one are connected either to the voltage supply (V_{dd}) or to ground, thus generating a thermometric filling of the matrix (gray and white units). The remaining varactor (black element in Fig. 2.6.3) is connected to the output of a 5b digital-to-analog converter (DAC) that provides an additional 32 voltage levels between V_{dd} and ground. Since only one varactor is biased at the point of this characteristic with a high voltage-to-frequency gain, the sensitivity of the oscillator to noise and spurious signals is minimized. Although the quantization of the varactor characteristic is not strictly required to reach the target fine frequency resolution, this approach was adopted to simplify the routing of the matrix.

The prototype was fabricated in a 65nm CMOS process using only standard devices provided by the technology. The unitary element of the matrix is an nMOS varactor with a capacitance that varies from a minimum of 4fF to a maximum of 12fF. In Fig. 2.6.4.a the measured fine tuning characteristic is reported, showing a very good agreement with the theory. Applying a shrinking factor up to 200, a fine-tuning range of 2.160MHz with an averaged resolution of 300Hz (minimum 150Hz) was achieved. Also multistandard capabilities were investigated by measuring the fine-tuning characteristics for different values of current I_1 (Fig. 2.6.4.b). The value of the fine-tuning range versus bias current of the shrinking block (I_1) is shown in Fig. 2.6.4.c. This can be programmed from 2MHz to 12MHz and the tuning characteristic is quite linear up to 8MHz.

The DCO phase noise measured by a spectrum analyzer is reported in Fig. 2.6.5. To minimize the phase noise the oscillator was biased to work in class-C (bias scheme not shown in Fig. 2.6.2 for simplicity) [3]. Due to the relatively low quality factor of the tank, estimated to be around 10, the phase noise at 1MHz away from the carrier is -127.5dBc/Hz at 3.3GHz. The structure draws 16mA from a voltage supply of 1.8V resulting in a figure of merit (FoM) of 183dBc/Hz. All other measurement results are reported in the table shown in Fig. 2.6.6. The DCO occupies an area of 0.32mm^2, dominated by the inductor and the two capacitor banks (Fig. 2.6.7).

Acknowledgments:
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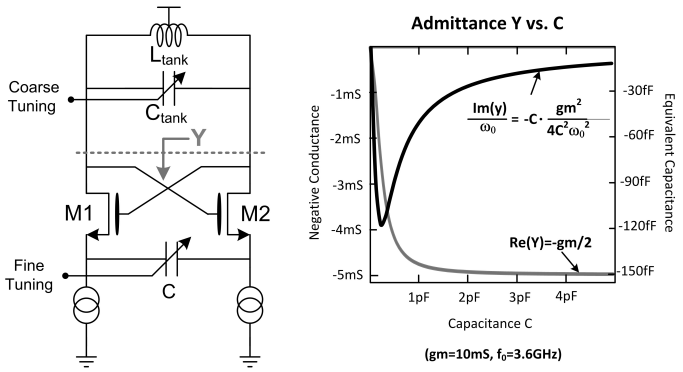

Figure 2.6.1: Capacitive degeneration tuning scheme.

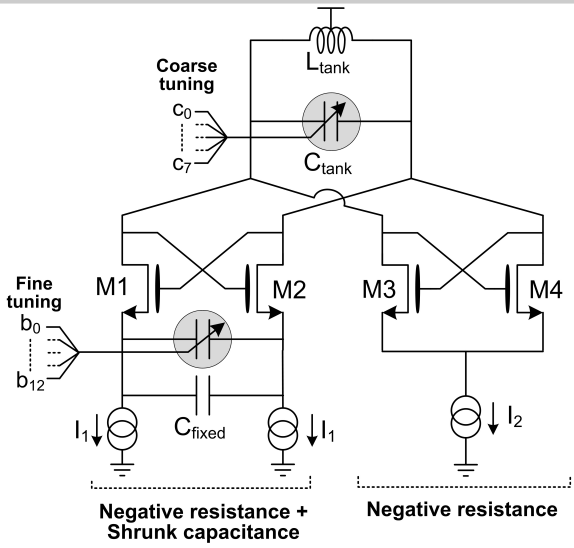

Figure 2.6.2: Complete DCO scheme.

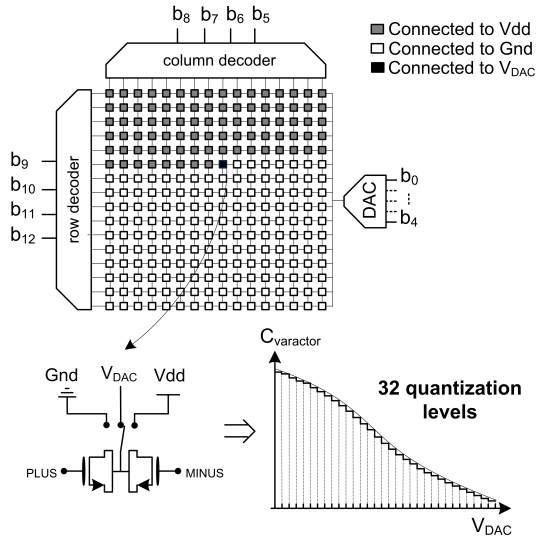

Figure 2.6.3: Fine tuning capacitor bank.

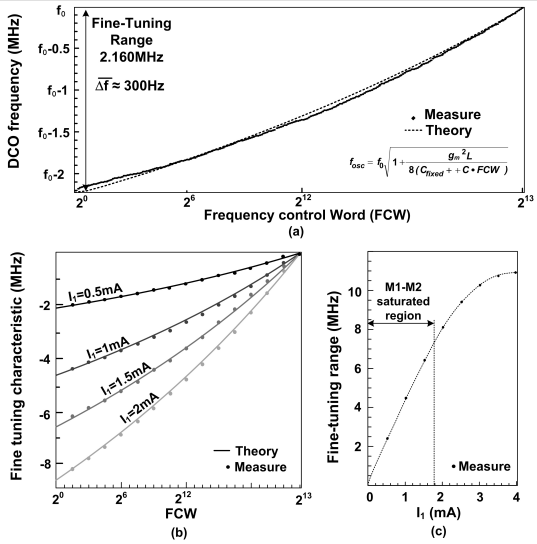

Figure 2.6.4: Fine tuning characteristics (a. shrinking factor =150).

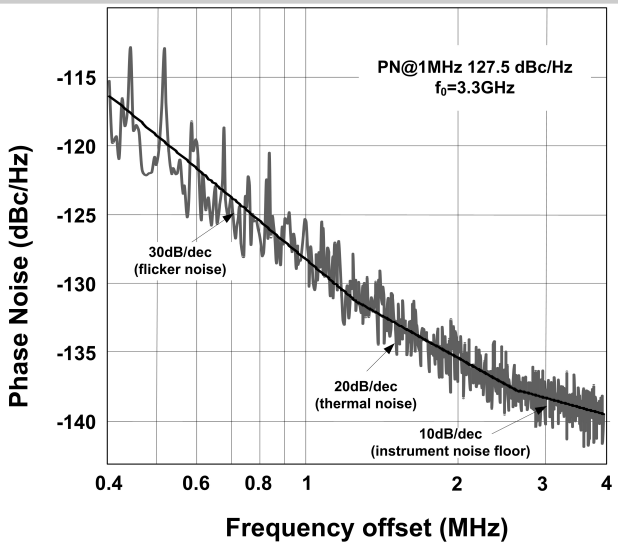

Figure 2.6.5: Phase noise measure.

Parameter	Result
DCO Frequency	2.62 – 3.3 GHz
Coarse Tuning Range	780 MHz (26%)
Coarse Frequency Resolution (excluding varactor)	25 MHz
Fine Tuning Range	2 to 12 MHz[(a)]
Fine Frequency Resolution	150 Hz to 1.5 kHz[(a)]
Power Supply	1.8 V
Current Consumption	16 mA
Phase Noise @ 1 MHz	-127.5 dBc/Hz
FoM	183 dBc/Hz
Technology	65 nm CMOS
DCO Area	0.32 mm^2

(a) Programmable by the bias current I_1

Figure 2.6.6: Measurement results.

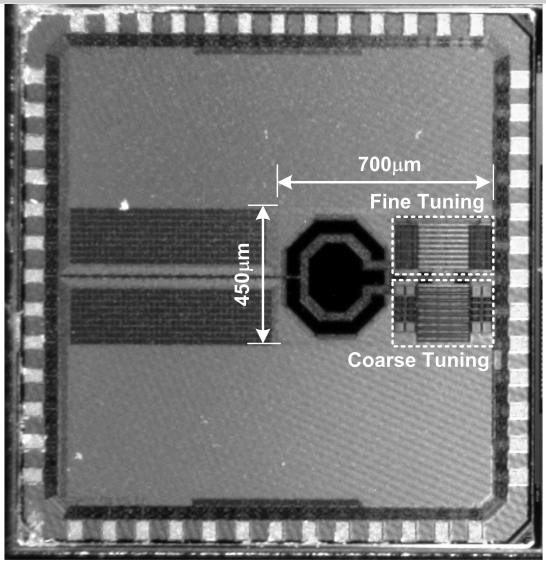

Figure 2.6.7: Die micrograph.

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