Two-Dimensions Vernier Time-to-Digital Converter

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***Abstract*—A two-dimensions Vernier algorithm applied to a time to digital converter (TDC) is presented. The solution proposed minimizes the length of the delay lines used to perform the digital conversion leading to a better efficiency compared to traditional linear approaches. A 7-bits TDC prototype, targeted for all digital PLL application, was realized in 65 nm CMOS technology with a time resolution of 4.8 ps and a power consumption of 1.65 mW for a conversion rate of 50 Msps. The longest delay line used in such a prototype is one third than what would have been required for a standard Vernier TDC.**

***Index Terms*—All digital PLL, TDC calibration, time to digital converter, Vernier.**

I. Introduction

In the evolution of phase-locked-loops (PLLs) towards a more flexible digital architecture, the time to digital converter represents one of the possible bottlenecks in the design of a spurs-free and low noise solution. Indeed, the quantization noise introduced by the converter limits the PLL integral in-band phase noise while the TDC distortions can generate unwanted tones near the output carrier [1], [2]. When the time resolution provided by a self-loaded inverter cannot satisfy the application requirements (e.g., for an in-band phase noise density below -100 dBc/Hz [1]) new solutions based on linear interpolation techniques have to be used [3]–[6].

One of the most popular approaches is based on the linear Vernier interpolation which can provide a time resolution Δ starting from two delay-lines formed by stages with respective delay of τ_1 and τ_2, both greater than Δ [3] (an example is reported in Fig. 1). Several modified linear Vernier architectures were proposed in literature in the attempt to increase resolution and/or reduce power consumption through additional levels of interpolation [5] or by exploiting the periodicity of the input signals [6]. Nevertheless, in all these solutions the number of stages grows exponentially with the number of bits making the TDC highly sensitive to delay jitter noise and mismatches especially when a high number of bits is required. The TDC presented in this paper aims at drastically reducing these problems exploring a novel two-dimensions (2-D) Vernier approach that allows a significant reduction in the length of the delay lines.

The paper is structured as follow: in Section II the 2-D Vernier TDC underlining concepts are introduced. In Section III, jitter noise and linearity are discussed and compared with linear solution. Finally, TDC prototype targeted of all digital PLL is presented in Section IV and measurement results are reported in Section V.

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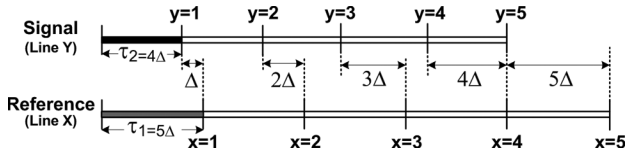

Fig. 1. Classic linear Vernier.

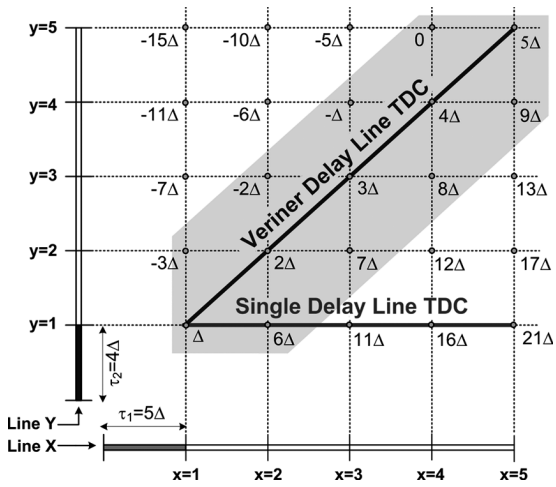

Fig. 2. Vernier plane $(\mathrm{k} = 5)$.

II. From Linear to 2-D Vernier TDC

In a linear Vernier, like the one drawn in Fig. 1, a differential delay Δ between two corresponding taps of the lines is accumulated after each stage so that a signal edge, which lags a reference edge by $n\Delta$ at the input of the Vernier, will be lined up with it after n stages. In this case delay quantization is realized by taking the time differences only between taps located in the same position of the two delay lines (e.g., the delay difference between the 2nd stage of line X and the 2nd stage of line Y) obtaining for example five quantization levels with two delay lines of five elements. If all possible differences between the taps are considered, the *Vernier plane* of Fig. 2 can be built, where 25 quantization levels instead of 5 are produced. However only a part of the generated quantization levels is uniformly spaced. Nonetheless an extension of the TDC range from $[\Delta,\ 5\Delta]$ to $[-3\Delta,\ 9\Delta]$ (grey zone) is obtained. This multiplies almost by three the number of uniformly spaced quantization levels of the linear Vernier.

The structure proposed can be considered as an extension of both the single line TDC [2] and the linear Vernier TDC [3], which lie respectively on the borders and on the diagonal of the

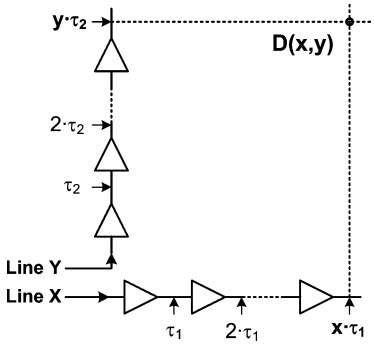

Fig. 3. Generic Vernier plane.

plane in Fig. 2. In the following, it will be shown that an even higher efficiency can be obtained exploring a wider region of the *Vernier plane*.

A. From the Vernier Plane to a TDC

To realize a time to digital converter, the differential delays generated in the plane XY must be arranged into a vector (with a generic index i) to obtain an ordered set of time references with a constant quantization step Δ (i.e., the final TDC resolution). Starting from the generic Vernier plane drawn in Fig. 3, this operation is performed by a function $i = i(x,y)\epsilon\mathbb{N}$ (called *routing function*) that associates the position i in the vector with the coordinates (x,y) so that

$$D(x,y) = x \cdot \tau_1 - y \cdot \tau_2 \triangleq i(x,y)\Delta \tag{1}$$

where $D(x,y)$ represents the differential delay generated at the position (x,y) (i.e., the time difference between x taps of length τ_1 and y taps of length τ_2). The *routing function* $i(x,y)$ depends on the choice of τ_1, τ_2 and can be found dividing (1) by Δ:

$$i = i(x,y) = x\frac{\tau_1}{\Delta} - y\frac{\tau_2}{\Delta}. \tag{2}$$

The existence of the *routing function* in $\mathbb{N}$ is guaranteed by the assumption that both τ_1 and τ_2 are multiple of the final resolution Δ. Indeed, starting from the Bezout's identity [7], it can be proved that the resolution Δ is always equal to the Greatest Common Divider (GCD)[1] between the unitary delays chosen (τ_1, τ_2). A particular family of 2-D Vernier is given by the set $\tau_1 = k\Delta$, $\tau_2 = (k-1)\Delta$ (e.g., 5Δ and 4Δ in Fig. 2), where the GCD $(\tau_1, \tau_2) = \tau_1 - \tau_2 = \Delta$ and the linear and the 2-D TDC are equivalent in terms of resolution. In other cases, starting from the same unitary delays τ_1 and τ_2, the two-dimension TDC and the linear Vernier do not have the same time resolution. (e.g., $\tau_1 = 5\Delta$, $\tau_2 = 3\Delta$ have still a GCD equal to Δ but their difference is 2Δ).

B. Uniform Quantization With Finite Delay Lines

Equation (2) implies that the *Vernier plane* can be mapped into a set of time references with a constant quantization step Δ only if no boundary are set for the (x,y) domain. Unfortunately, when delay lines with a finite number of elements are used, the generated plane cannot produce a uniform quantization of the entire co-domain i (e.g., in the plane of Fig. 2, 10Δ, 14Δ and other values are missing). The region of the plane (X,Y) that corresponds to a uniform quantization for the co-domain i can be found inverting (2). Since in the general case this operation is not trivial, being $i(x,y)\epsilon\mathbb{N}$ not biunique, the following analysis will be restricted to the class of *Vernier planes* with $\tau_1 = k\Delta$, $\tau_2 = (k-1)\Delta$. Under this assumption, (2) can be rewritten as

$$i = xk - (k-1)y. \tag{3}$$

Limiting $y\epsilon[0,k]$, this equation can be inverted obtaining

$$\begin{cases} x(i) = i - \left\lfloor \frac{i-1}{k} \right\rfloor (k-1) \\ y(i) = i - \left\lfloor \frac{i-1}{k} \right\rfloor k \end{cases} \tag{4}$$

where $\lfloor a \rfloor$ is the inferior integer of a. From (4) it is possible to verify that, while $y(i)$ is periodic and limited between 0 and k, $x(i)$ exceeds k, for $i > 2k-1$. This suggests that, contrary to a linear approach, it is possible to extend the TDC range increasing only one of the two delay lines. An example is shown in Fig. 4 where the range of uniform differential delays of the TDC reported in Fig. 2 has been extended from 9Δ to 24Δ with the addition of only 3 delay stages in line X.

For a given number of quantization levels N, the use of a 2-D approach reduces significantly the length of the delay lines used to generate the delay compared with a linear Vernier. In fact, in the limit, the number of stages required is proportional to $\sqrt{N}$ instead of N. In particular, for the example described in Fig. 4, it can be verified that the longest delay line $\mathrm{X}(8\ \mathrm{stages} \cdot 5\Delta = 40\Delta)$ does not exceed the double of the TDC full scale $(24\Delta - (-3\Delta) = 27\Delta)$. Notice that, in a linear Vernier TDC the longest delay cannot be less than twice the full scale if both τ_1 and τ_2 are greater than Δ.

As it will be shown in Section III, shorter lines produce a smaller analog jitter noise and reduce also the integral non-linearity of the TDC produced by the mismatches between the stages.

C. Circuit Implementation

A 2-D Vernier TDC implementation can be derived starting from the classical linear Vernier architecture where the time references are realized with two delay lines and the digital conversion is performed by flip-flops used as time comparators [3]. In Fig. 5 a circuit implementation of the 2-D Vernier corresponding to the plane of Fig. 4 is reported. The scheme refers to the integrated prototype discussed in detail in Section IV. In this case, the ratio between the tap delay of the two lines τ_1/τ_2 is equal to 11/10 and with 19 stages for line X and 11 stages for line Y, giving a total of 119 quantization levels.

For each point defined by the *routing function* a flip-flop is used as a time comparator. To provide the same load to all the taps of the delay lines, additional dummy comparators are placed at the corners of the matrix (grey zone). Finally, to obtain a thermometric code the flip-flops outputs are ordered into a register following the *routing function* $i(x,y)$ expressed by (3).

To define the proper routing function $i(x,y)$, the ratio τ_1/τ_2 needs to be precisely set to its nominal value of k/k-1. This ratio can be controlled using a delay-locked loop (DLL) which forces the total delay accumulated after $k-1$ stages of line X to be

[1]Notice that the GCD can be also defined in the time domain being it a commutative ring [11].

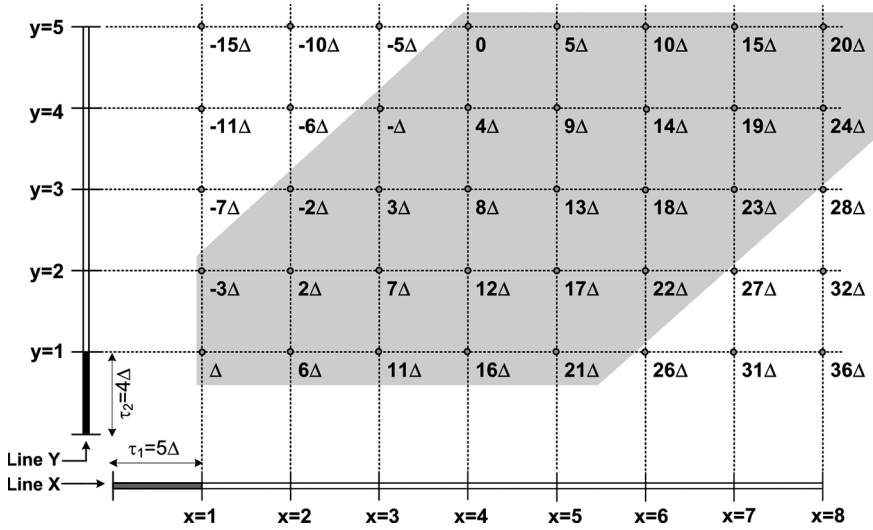

Fig. 4. Expansion of square Vernier TDC.

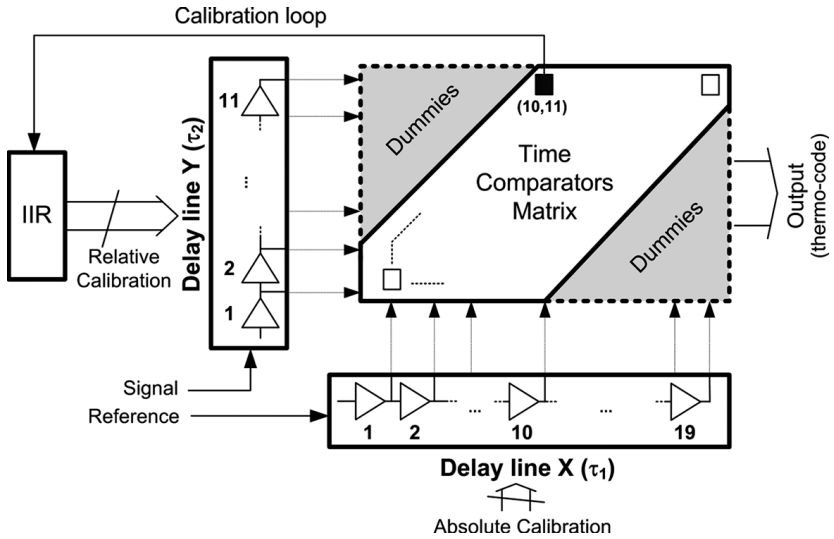

Fig. 5. 2-D Vernier TDC implementation.

equal to the one accumulated after k stages of line Y. To do this, during the calibration phase, both delay lines are fed with the same signal and the output of the latch at the position (10, 11) is used to estimate the delay difference between 10 delays of line X and 11 delays of line Y, forcing the τ_1/τ_2 ratio to 10/11. The latch output signal is integrated by an infinite impulse response (IIR) filter whose output (digital) is directly used to control the delay lengths of line Y (this is possible since the delay lines are digitally controlled). Since this calibration requires the same signal in both delay lines, this solution demands an input network able to interleave between acquisition and calibration phases.

III. Noise and Linearity Analysis in the Vernier Plane

The non-idealities of the two delay lines limit the effective number of bits achievable by the TDC. To quantify this effect the delay must be modeled in a way that accounts for noise and mismatches. The model used for the analysis of the 2-D Vernier TDC is reported in Fig. 6. The "analog jitter noise" introduced by each stage is represented inserting after each delay stage an additive, Gaussian and uncorrelated noise source with a standard deviation equal to σ_{jitter}. In addition, temperature and process variation are modeled with parameters α and β_j. α is associated with the absolute delay variation that affects all the

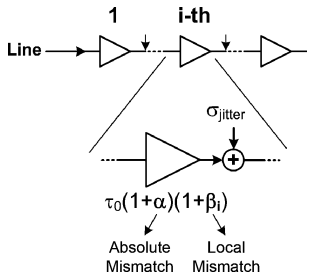

Fig. 6. Delay model for noise and linearity.

elements in the same way, while β_{j} corresponds to the local mismatch of each element that changes along the lines. The model shown in Fig. 6 can be described by the following equation:

$$\tau_{\mathrm{j}} = \tau_0 \cdot (1+\alpha)(1+\beta_{\mathrm{j}}) + \sigma_{\mathrm{jitter}} \tag{5}$$

where τ_0 is the nominal delay of the stage, σ_{jitter} is the standard deviation of the jitter noise associated to each stage, α models absolute process and temperature variations, and β_{j} represents the local mismatch of the element at position j in the delay line.

A. Jitter Noise Analysis

The jitter noise introduced by each stage limits the minimum delay that can be reliably measured by the TDC since adds an uncertainty to the measure. In particular, to guarantee less than one LSB integral error, the maximum jitter accumulated along the delay-lines has to be lower than the resolution Δ. The variance jitter noise $\sigma^2_{\mathrm{matrix}}(\mathrm{x},\mathrm{y})$ accumulated at a generic position (x, y) in the Vernier plane can be evaluated from (1) using the model described by (5) (with $\alpha = 0$ and $\beta_{\mathrm{j}} = 0$) obtaining

$$\sigma^2_{\mathrm{matrix}}(\mathrm{x},\mathrm{y}) = \sum_{\mathrm{i}=1}^{\mathrm{x}} \sigma^2_{\mathrm{x,i}} + \sum_{\mathrm{i}=1}^{\mathrm{y}} \sigma^2_{\mathrm{y,i}} = \mathrm{x}\cdot\sigma^2_{\mathrm{x}} + \mathrm{y}\cdot\sigma^2_{\mathrm{y}} \tag{6}$$

where σ^2_{X} and σ^2_{Y} are the variances of the jitter noise introduced by each stage of lines X and Y respectively. Assuming a total number of quantization levels equal to N, in the solution proposed the total numbers of elements for the two delay lines X, Y are respectively the superior integer of $2\sqrt{\mathrm{N}/2}$ and $\sqrt{\mathrm{N}/2}$ which lead to a maximum accumulated jitter of

$$\sigma^2_{\mathrm{matrix,max}} = 3\sqrt{\frac{\mathrm{N}}{2}}(\sigma^2_{\mathrm{X}} + \sigma^2_{\mathrm{Y}}) \tag{7}$$

Compared to the linear Vernier (where the number of element of both delay lines is equal to N), the proposed solution reduces the accumulated jitter noise by a factor proportional to $\sqrt{\mathrm{N}}$ assuming the same current is used in the delay elements in the two cases. Notice that this corresponds also to a significant power savings. Alternatively, for a given power consumption, shorter delay lines allow using much more current per stage that gives smaller jitter noise sources (i.e., σ^2_{X} and σ^2_{Y}) further reducing the accumulated noise.

B. Linearity

The linearity of linear and 2-D TDCs transfer function has been characterized in terms of integral-non-linearity (INL) and differential-non-linearity (DNL) including the effect of the calibration loop used to set the ratio τ_1/τ_2. This was realized performing Monte Carlo simulations of a behavioral model described by (1) and (5), assuming a variance σ^2_α for α, σ^2_β for β_{j}, while setting $\sigma^2_{\mathrm{jitter}} = 0$. The comparison was done for the same number of quantization levels of the prototype $(N = 119)$.

The INL variance σ^2_{INL} as a function of the TDC output code i is plotted Fig. 7(a) (normalized to the mismatch variance σ^2_β). Compared to the linear approach (dashed line), the 2-D solution (solid line) reduces by approximately a factor of three the maximum INL thanks to the use of shorter delay lines. In fact, while the linear TDC needs two 119 elements lines, the 2-D Vernier requires a line X with 19 elements and a line Y with 11 elements.

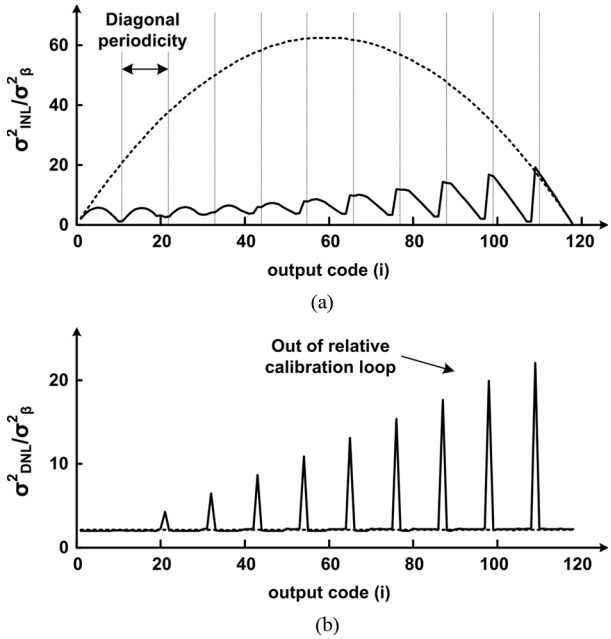

Fig. 7. σ^2_{INL} and σ^2_{DNL} versus TDC output code i (linear Vernier, dashed line; 2-D Vernier, continuous line), number of quantization levels $N = 119$.

The exploration of a plane, instead of a line, gives an equivalent folding of the time quantization realized along the two delay lines. This produces a periodicity in the INL that depends on the number k of consecutive quantization levels that lie on each diagonal (in this case equal to 11). The use of a calibration procedure to set the ratio τ_1/τ_2 to its nominal value reduces the impact of delay elements mismatches. However since the calibration includes only half of the delay line X (Fig. 5), the INL of the 2-D TDC grows for higher codes (Fig. 7(a)).

For the DNL Fig. 7(b), the folding realized in the 2-D structure produces a sharp peak when consecutive output codes lay on different diagonals. Also in this case the peaks are more evident for higher codes due to the absence of calibration in the last part of the Vernier plane. However, in the measurements section it will be shown that a monotonic characteristic of the TDC (necessary for the PLL stability) can be achieved.

IV. TDC Prototype

To validate the solution proposed, a TDC prototype was integrated in 65 nm CMOS technology, having as target a time resolution of 5 ps and a full scale of 595 ps (119 levels). The technology used gives a minimum delay per stage of 20 ps if worst case temperature and process variations are considered. As a consequence, a Vernier architecture (either linear or 2-D) became necessary to reach the target resolution. The design of the prototype (based on the 2-D architecture described in Section II-B) resulted in $k = 11$ $(\tau_1/\tau_2 = 11/10)$, which forces $\tau_1 = 11\Delta = 55$ ps and $\tau_2 = 10\Delta = 50$ ps (Fig. 5). The entire TDC full scale is covered using 19 element for line X, 11 elements for line Y resulting in a maximum delay line of 1.045 ns, that, as predicted in Section II is less than twice the TDC full scale.

The TDC design starts from the time comparators whose analog performances (jitter, offset, offset matching) are almost

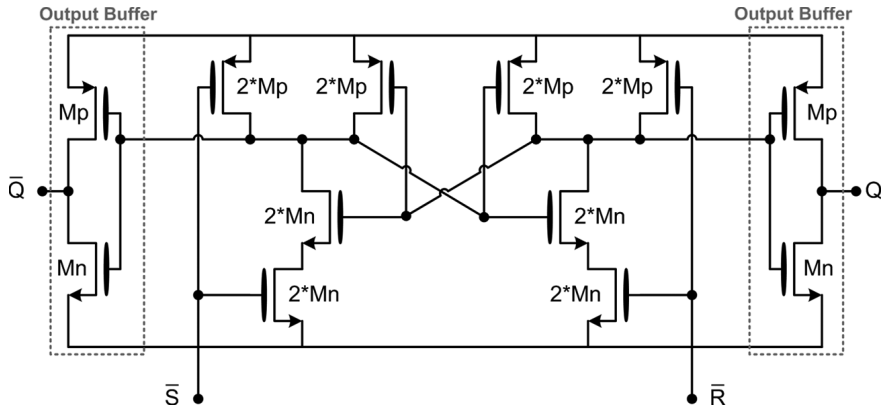

Fig. 8. Time comparator schematic.

independent of the other TDC building blocks. The input capacitance of the time comparators has to be minimized since in a 2-D Vernier an entire line of comparators is connected to a single stage of the delay lines. This sets the required driving capability of the delay element and at the same time affects the total power consumption of the two delay lines. Once time comparators are designed, the delay lines can be realized, with the target of minimizing the jitter noise and the distortion introduced. In the following, each TDC building block will be discussed, focusing on the main parameters that influence the final performance.

A. Time Comparator

The time (or phase) comparator can be thought as a single bit TDC which decides if the delay between the input signals is positive or negative (identifying which signal corresponds with the first positive edge). The time comparator is functionally equivalent to a voltage comparator in a flash A/D converter. As in a voltage comparator the input signal is a voltage difference in a time comparator the input signal is a delay between two rising edges (i.e., a time difference).

The most important parameter for the design of this block is the *offset* matching. While for a voltage comparator the *offset* is represented as a battery in series to one of the comparator inputs, in this case the *offset* corresponds to an additional delay between the input signals and it is known as *time skew*. The *offset matching* among the comparators affects the TDC linearity with a direct impact on the DNL (its influence on INL is less significant since the error introduced is not accumulated during the quantization process).

The time comparator was implemented with a Set-Reset (SR) latch (Fig. 8). The solution was preferred to the traditional flip-flop-D architecture [3] due to its perfect symmetry that allows to minimize systematic time skew and load in the same way both delay lines. Furthermore, the SR latch results in a very compact layout, highly desirable in a 2-D system where a large number of comparators are organized in a bidimensional structure. The size of the latch input devices was designed with the help of Monte Carlo simulations to minimize *offset mismatches*. A histogram of the simulated offset is reported in Fig. 9. The resulting time comparator exhibits a standard deviation of the input referred offset of less than 1 ps (enough for the target resolution of 5 ps).

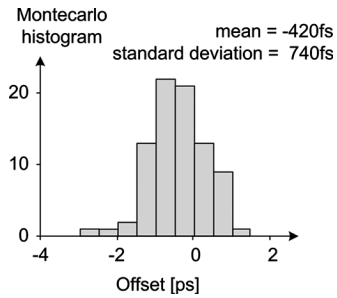

Fig. 9. Time comparator offset Monte Carlo histogram.

B. Delay Lines

Two different delay elements are needed to create the "time reference" for the 2-D Vernier TDC and their relative accuracy determines the linearity of the TDC. The structure of a delay element is shown in (Fig. 10). It is made up by the cascade of two inverters plus a digitally controlled capacitor bank used for the delay calibration. Two cascaded inverters in each delay tap are required when using an SR latch as a time comparator since such a latch operates only on the rising edges of the clock. Tuning of the delay acting on the capacitive load (at the output of the first inverter) produces a linear tuning characteristic (in term of digital word versus delay) benefitting both the overall linearity and the stability of the DLL used during calibration (Fig. 5). Finally, the presence of two delays stage per tap (required to have a non-inverting delay element) offers isolation between the capacitor bank and the latch, allowing to realize sharper edges in front of the latch.

To reach the target resolution of 5 ps, the delays in line X and Y have to be set respectively to 55 ps and 50 ps. To compensate for Process, Voltage and Temperature (PVT) variations a capacitor bank constituted by 80 elementary Metal-Oxide-Metal capacitors (MOM) is used. They can be either connected to ground through an n-MOS switch or left floating, producing in the worst-case PVT corner a delay tuning with steps of 1 ps. The capacitor array adopts a common centroid layout. To minimize the number of connection, the 80 programming switches are controlled with a "pseudo binary" code resulting in a twelve wires control bus. The simulations of the tuning characteristics for the most significant PVT variation corners are reported in Fig. 11. From the plot it is possible to verify that the required delays of 50 ps and 55 ps can be obtained in all the corners.

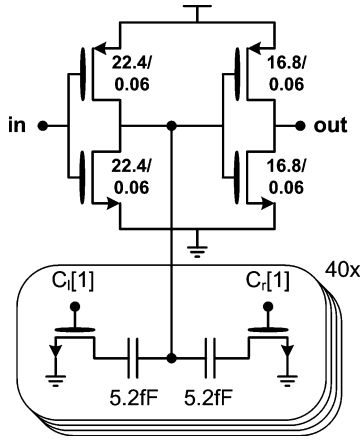

Fig. 10. Delay element schematic.

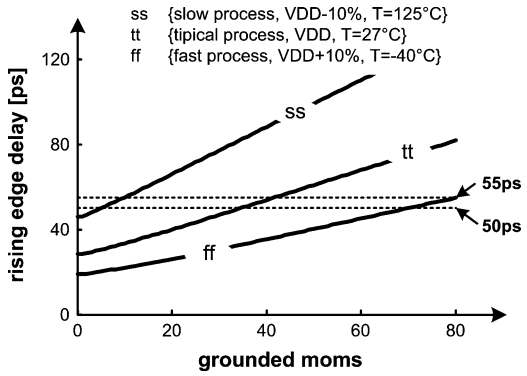

Fig. 11. Delay element tuning characteristic.

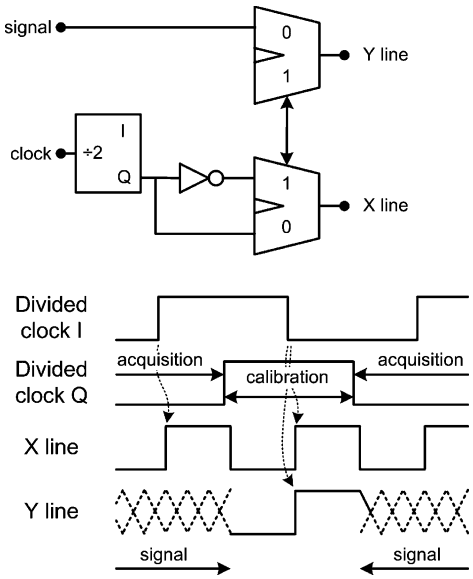

Fig. 12. Input network.

C. Input Network

The input network used to interleave the acquisition and calibration phases is reported in Fig. 12. The generation of the two operative phases is performed injecting a 100 MHz clock that is divided by two producing quadrature outputs. This solution guarantees a robust generation of the two operative phases over all PVT variations. During the acquisition phase, the 50 MHz reference clock and the input signal are injected respectively in the line X and Y, while during the calibration phase the two lines are feed with the same signal (i.e., the reference one).

The choice of a full-rate interleaving of acquisition and calibration phases allows a simple circuit implementation but doubles power consumption. However since the calibration has to correct only thermal drifts, the bandwidth associated with the calibration loop can be much lower than 50 MHz. Consequently the sample-rate can be significantly reduced (below one MHz) without affecting stability. The solution implemented was chosen only to simplify the input network for the testing phase.

In conclusion of this section we will make some general remarks and comparison. First, the achieved time resolution of 5 ps does not represent a fundamental limit of the solution proposed in this technology, but it derives only from the specs defined by the target application. Second, while with the solution proposed the longest delay line is 1.045 ns (i.e., 19×55 ps), to cover the same full scale with the same resolution a linear Vernier would have required two lines of 119 elements each with a minimum total delay length of 2.38 ns (i.e., 119×20 ps) for one line and of 2.975 ns (i.e., 119×25 ps) for the second line. This value is 5 times the TDC full scale and corresponds to 2.85 times the longest delay line used in the 2-D Vernier TDC.

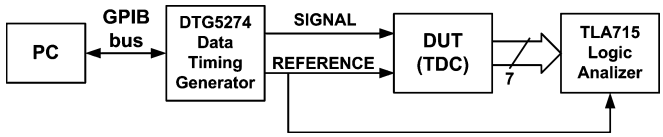

Fig. 13. Test bench.

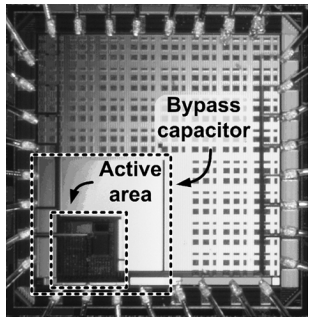

Fig. 14. Prototype microphotograph.

V. Measurements Results

The microphotograph of the TDC test chip, fabricated in 65 nm low power standard CMOS technology by TSMC, is shown in Fig. 14. The active area is 260 μm × 260 μm dominated for more than 2/3 by the digital part necessary for the chip control and the post processing. The digital logic performs three main tasks: output code processing, delay lines calibration and communication with the Test Bench (through an I^2C bus). The output code processing is based on a thermo-to-binary conversion for a 7-bits full-rate output. To verify the absence of bubbles within the thermometric code, a debug mode allows to serialize the thermometric word (119 bits), trough the 7-bits output bus.

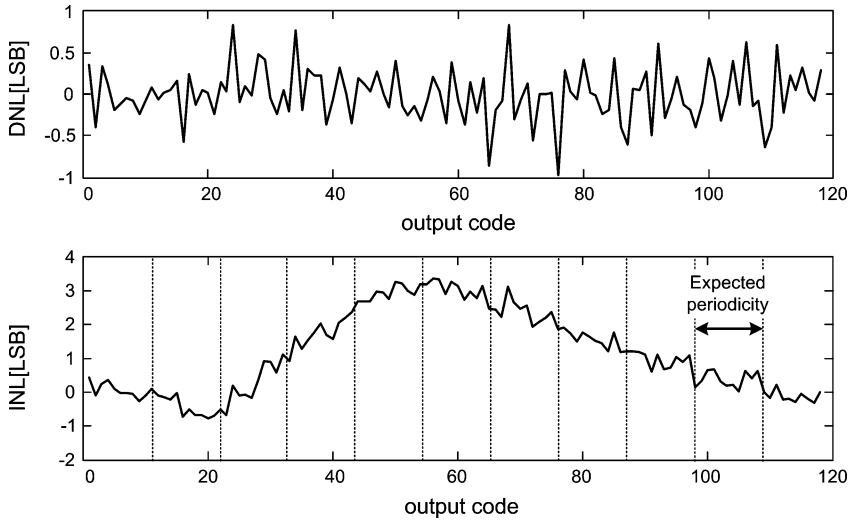

Fig. 15. DNL and INL measurements @ 4.8 ps of resolution.

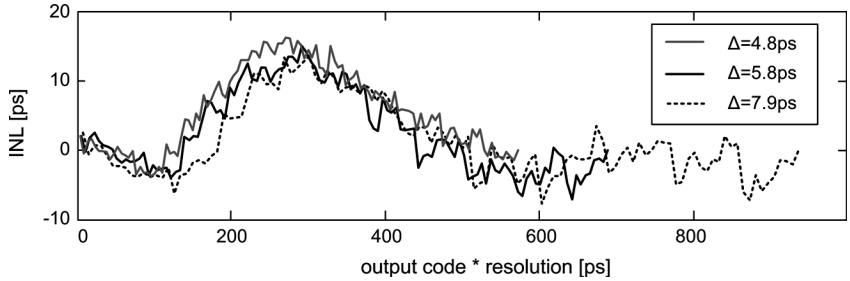

Fig. 16. INL measurements for different gain (a) and TDC intrinsic INL extrapolation (b).

The test bench used to characterize the prototype is depicted in Fig. 13. The entire TDC characteristic (around 600 ps) was explored incrementing the delay between reference and input signal by 1 ps per step using the Tecktronix DTG5274 data-timing generator. For each point of the characteristic, 9500 samples were taken and stored using a logic analyzer TLA715. All the measurement results correspond to a 1.2 V supply, a 50 Msps TDC output rate and a 100 MHz reference clock as required to interleave the calibration and the acquisition phases (see scheme in Fig. 12).

The measured INL and the DNL were obtained for a resolution of 4.8 ps using a data processing based on the histogram method. The results are reported in Fig. 15. The DNL is always less the one LSB while the INL shows a maximum of 3.3 LSBs. The big bump present in the INL measure is incompatible with the folding existing in the proposed architecture, which demands a periodicity in the INL (as explained in Section III). In order to identify the cause of this unexpected behavior the possible sources of distortion have been investigated. Three different distortion sources were analyzed: the comparators, the delay lines and the input network. Unmatched delay elements or unmatched comparators produce an effect on the absolute INL (and DNL) that depends on the time resolution or the offset of the converter. On the contrary, any distortion produced before the quantization process (i.e., within the input network), should have an effect on the absolute INL independent from the value of the TDC time resolution. For this reason, the TDC linearity has been measured varying the time resolution from 4.8 ps to 7.9 ps (acting on the capacitor bank present in the delay lines). The results are reported in Fig. 16. The invariance of the absolute INL bump with the time resolution suggested that the main source of the unexpected distortion occurs before the quantization process (i.e., on the board or most probably in the input network). One assumption is that when the rising edges of the input signals are very closed to each other, a cross-talk in the input network generates a pulling that distorts the delay ramp used to characterize the TDC.

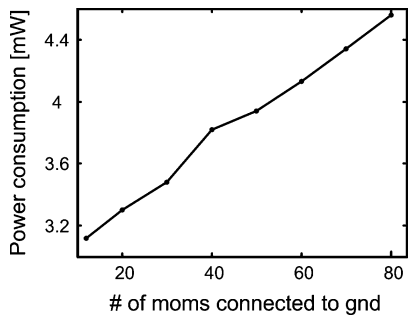

Fig. 17. Power consumption versus delay trimming.

The power consumption of the whole TDC has been evaluated for a 50 Msps sample rate including calibration phase contribution. Fig. 17 shows the power consumption for different number of capacitance connected to the delay elements of the X delay line (which corresponds to different time resolutions).

TABLE I
MEASUREMENT RESULTS AND STATE OF THE ART

	This work	[2]	[3]	[6]	[8]	[10]
# of bits	7	6	7	6	9	11
Delay stages /step	0.26	1	2	1	0.1	n.a.
Resolution [ps]	4.8	17	30	12	1.25	1.2***
INL [LSB]	3.3 (<1*)	0.7	1	1.15	2	-
DNL[LSB]	<1	0.7	-	1	0.8	-
Bandwidth [MHz]	50	26	130	40	10	1
Area [mm^2]	0.02**	0.01	10	0.04	0.06	0.04
Supply Voltage [V]	1.2	1.3	5	1.2	1	1.5
Power dissipation [mW]	1.7	1.8	-	2.5	3	2.2-21
FoM [pJ/step]	0.28	1	-	0.96	0.58	0.23
Technology	65nm	90nm	0.7 µm	130nm	90nm	130nm

* Extrapolated TDC intrinsic INL
** TDC core
*** Equivalent overall 1MHz of bandwidth

In Table I the measured results are compared with those of other solutions presented in literature. The number of delay stages required for a given number of quantization steps is significantly lower than all the others, and is comparable only to the solution reported in [8] which adopts a two-steps architecture. The proposed prototype shows the lowest power consumption with a FoM (defined as in [10]) of 0.28 $\mathrm{pJ}/(\mathrm{step} \times \mathrm{conversion})$. These comparisons should be taken with some care since different implementations use different technologies, whose impact is difficult to be evaluated.

VI. CONCLUSIONS

Novel two-dimensions TDC Vernier architecture was presented. In a 2-D approach the number of delay elements required for N quantization levels grows with $\sqrt{N}$ resulting in a set of design constraints that are favorable for large number of bits.

A 7-bits 5 ps resolution TDC prototype was design and tested validating the theory. The poor INL performances of the reported prototype have been demonstrated to be independent on the quantization process; therefore they represent a design fault of the prototype and not a theoretical drawback of the 2-D Vernier architecture.

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