Capacitive Degeneration in LC-Tank Oscillator for DCO Fine-Frequency Tuning

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***Abstract*—A digitally controlled oscillator (DCO) that achieves a minimum frequency quantization step of 150 Hz without any dithering is presented. The fine digital tuning is obtained through a capacitive degeneration of a portion of the transistor switching pair used in a classical LC-tank oscillator. The new tuning circuitry does not appreciably affect the intrinsic oscillator phase noise and allows to trim the frequency with a programmable resolution for calibration and multi-standard operation. A prototype integrated in 65 nm CMOS technology exhibits a phase noise of −127.5 dBc/Hz @ 1 MHz drawing 16 mA from a supply of 1.8 V, resulting in a FoM of 183 dBc/Hz. The active area is 700 μm$\times$ 450 μm.**

***Index Terms*—ADPLL, capacitance shrinking, DCO, digitally controlled oscillator, fine tuning, GSM, LC-tank oscillator.**

I. Introduction

THE migration of phase-locked loops (PLL) towards all-digital architectures with a comparable and even better performance will be made possible by further technology evolution that will allow to achieve an adequate quantization of time and frequency [1]. In particular, a fine resolution of the time-to-digital converter (TDC) is required to minimize the quantization noise introduced in the PLL band, while a tiny frequency discretization of the DCO allows to reduce the noise added far from the carrier. Although the technology evolves by itself in the direction of these goals, with shorter delay stages and smaller parasitic capacitances, the target resolutions for wireless applications are still quite challenging to make possible a simple transposition of analog solutions into digital ones [1]. For example, in the design of a DCO for GSM applications, the target frequency resolution of few kHz with respect to a tuning range of several hundred MHz around the carrier (e.g., 400 MHz in GSM [2]) results in unitary capacitive elements of the order of atto-Farad that cannot be easily integrated [3]. A possible solution is the use of capacitive divider networks to obtain a reduction of the minimum effective capacitance that can be switched in parallel to the tank [4]. This approach can improve the DCO frequency resolution but the sensitivity to mismatches and parasites limits the robustness of the final design. A more reliable technique proposed by Staszewski *et al.* [2] consists in the dithering of the less significant bits of the DCO frequency control word (like in a sigma-delta DAC). This solution reduces considerably the equivalent DCO frequency resolution (from 12 kHz to 30 Hz in [2]) but, as it occurs in any sigma-delta data converter, the quantization noise is moved to higher frequencies where the phase noise specs may be even more challenging. Due to this problem, the frequency of dithering must be very high (e.g., 225 MHz) to satisfy the emission mask requirements far away from the carrier [2].

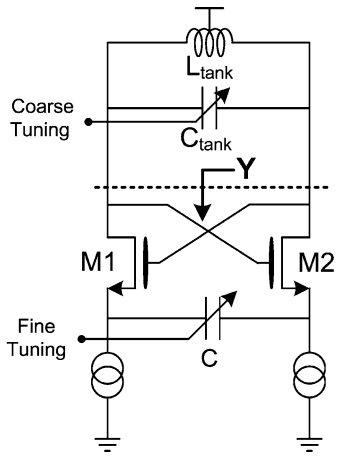

Fig. 1. Proposed fine-tuning DCO scheme.

All the solutions presented in literature try to improve the DCO resolution working at the level of the oscillator tank, either making a custom design of the capacitive element or exploiting some kind of shrinking effect of the elements of the *LC* resonator [2]–[7]. The idea of this work is to move part of the tuning bank from the tank to the sources of the switching pair of the *LC* oscillator exploiting an intrinsic shrinking effect present in the structure (Fig. 1). The portion of the capacitive array still in parallel to the tank (named *coarse tuning bank*) is used to compensate process and temperature variation, while the portion at the source of M1 and M2 (named *fine tuning bank*) is used for the DCO modulation inside the PLL. As it will be shown, this approach allows an easier design of both coarse and fine tuning banks, avoiding the use of dithering and without introducing any degradation in the DCO phase-noise.

The paper is organized as follows: in Section II the fine tuning scheme is introduced, focusing on the main mechanism that produces an equivalent scaled down replica of the fine tuning bank in parallel to the tank (Fig. 1). The impact on phase-noise performance is analyzed at the end of Section II and in more detail in the Appendixes. In Section III, the fine-tuning range and its calibration are discussed while in Section IV the design of a prototype in 65 nm CMOS technology tailored to GSM application

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is presented. A complete set of experimental measurements carried out on the prototype are reported in Section V, together with a comparison with the state of the art.

II. Basic Idea

In general, the role of the transistor switching pair in a classic *LC* tank oscillator is to sustain the oscillations restoring the energy losses that occur in the tank [8]. This operation is commonly represented as a negative resistance in shunt with the resonant load that, to a first approximation, does not affect the oscillator frequency ($\omega_{\rm LO}$). This frequency is adjusted acting on the total capacitance present in the tank ($\rm C_{tank}$) so that

$$\frac{\delta\omega_{\rm LO}}{\omega_{\rm LO}} \approx \frac{\delta \rm C_{tank}}{2\rm C_{tank}} \tag{1}$$

where $\delta\omega_{\rm LO}$ is the variation in the oscillation frequency caused by a change $\delta \rm C_{tank}$ in the total capacitance of the tank $\rm C_{tank}$. A frequency resolution $\delta\omega_{\rm LO}/\omega_{\rm LO}$ of less than a few ppm (e.g., 1 kHz over 3.6 GHz) would require almost the same tank capacitance resolution $\delta \rm C_{tank}/C_{tank}$. This corresponds to an exceedingly small unitary element in the capacitor tuning bank when the total capacitance in the tank is in the order of pico-Farad. In this section it will be shown that this problem can be overcome using the capacitive degeneration introduced in Fig. 1 that adds a reactive component to the classical negative resistance providing an additional tuning mechanism.

A. DCO Equivalent Circuit

Since the circuit operates in a large signal regime, the structure has been studied using a small signal time variant analysis [9], where the MOS transconductance $\rm g_m$ was averaged over a time interval equal to one period of the oscillation frequency $2\pi/\omega_{\rm LO}$ (high order harmonics were neglected for simplicity). Under these assumptions, the oscillator reported in Fig. 1 can be modeled by the scheme reported in Fig. 2. In fact, the signal current that flows into transistor M1-M2 is the same as that flows into capacitance C and is related to the voltage across the tank with an inversion of sign due the gate-drain cross-connections.

The effect of C on the DCO frequency tuning characteristic can be estimated evaluating the admittance Y (indicated in Fig. 2 as $\rm gm_{eq}+C_{eq}$) using a series to parallel conversion in the circuit of Fig. 2. The admittance Y can be expressed as follows:

$$\rm Y = -\frac{g_m}{2}\cdot\frac{4C^2\omega_{LO}{}^2}{gm^2+4C^2\omega_{LO}{}^2} - j\omega_{LO}C\cdot\frac{g_m{}^2}{g_m{}^2+4C^2\omega_{LO}^2} \tag{2}$$

where $\omega_{\rm LO}$ is the oscillation frequency of the DCO. For $\rm C \gg g_m/(2\omega_{LO})$ (2) can be rewritten as

$$\rm Y = -\frac{g_m}{2} - j\omega_{LO}C\cdot\left(\frac{g_m}{2\omega_{LO}C}\right)^2 = -\frac{g_m}{2} - j\omega_{LO}CQ_f^2 \tag{3}$$

where $\rm gm_{eq}$ becomes the classical negative conductance which compensates tank losses [8], while $\rm C_{eq}$ is equal to the capacitor C shrunk by a factor $-\rm g_m^2/(2\omega_{LO}C)^2$. As shown in (3) this factor is equal to $Q_{\rm f}^2$, where $Q_{\rm f}$ is the quality factor[1] of the impedance which models the degenerated switching pair given by

$$\rm Q_f = \frac{g_m}{2\omega_{LO}C}. \tag{4}$$

If the quality factor $\rm Q_f$ is reduced, the equivalent capacitance at the tank diminishes. It will be shown that, although $\rm Q_f$ has to be lower than one to provide a shrinking effect, this does not have any adverse effect on phase noise or amplitude of the LO since the impedance in parallel to the tank is negative and restores DCO losses.

Starting from (2), $\rm gm_{eq}$ and $\rm C_{eq}$ have been plotted in Fig. 3 versus C (assuming $\rm g_m = 10\ mS$ and $\omega_{\rm LO} = 3.6$ GHz). $\rm gm_{eq}$ shows a monotonic behavior that asymptotically tends to $-\rm g_m/2$ while $\rm C_{eq}$ is not monotonic and starts to decrease for $\rm C > g_m/(2\omega_{LO})$. Since the absolute value of the (negative) real part of Y has to be larger than $\rm 1/R_{loss}$ to sustain the oscillation, the useful portion of the plot of Fig. 3 corresponds to C greater than $\rm C_{osc}$ (i.e., the minimum value of C for which $\rm gm_{eq} > 2/R_{loss}$). From the plot of Fig. 3 it can be seen that, for the set of parameters used, a capacitor $\rm C = 3$ pF is reflected in parallel to the tank into an equivalent capacitance $\rm C_{eq} = 15$ fF with a shrinking factor of about 200. This means that switching on a capacitor of 5 fF at the sources of M1-M2 produces the same effect as switching on a capacitor of 25 aF in parallel to the oscillator tank.

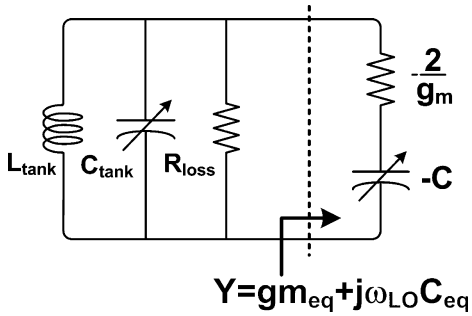

Fig. 2. DCO equivalent scheme.

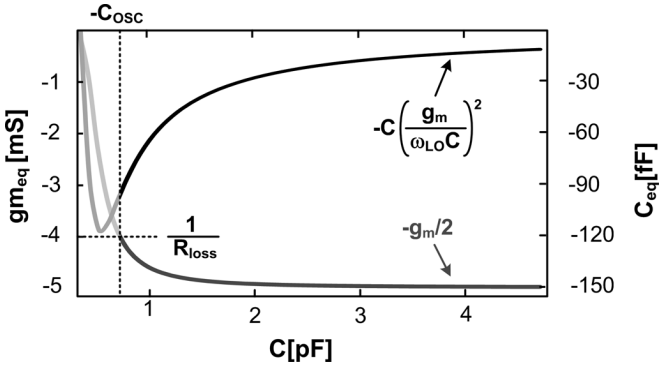

Fig. 3. Real and Imaginary par of admittance Y ($\rm g_m = 10\ mS$, $\rm R_{loss} = 250\ \Omega$, $\omega_0 = 3.6$ GHz).

[1]The quality factor is defined only as $\rm Im[Z]/Re[Z]$

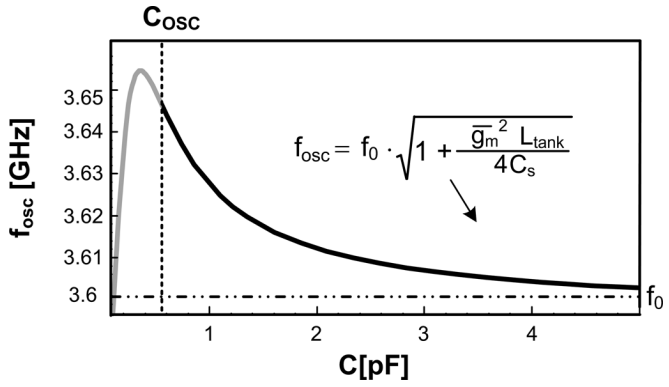

Fig. 4. DCO fine frequency tuning ($g_m = 10\ \mathrm{mS}$).

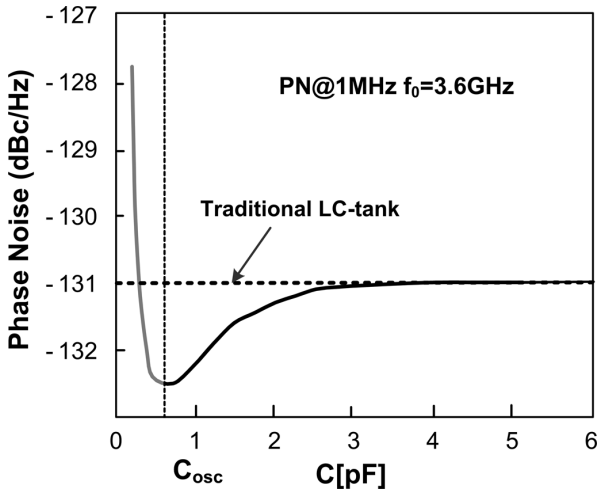

Fig. 5. Phase noise versus degenerating capacitance C.

B. DCO Fine-Frequency Tuning Characteristic

The tuning characteristic of the oscillator as a function of the capacitance C (i.e., $\omega_{\mathrm{LO}} = \omega_{\mathrm{LO}}(\mathrm{C})$) can be found evaluating the resonance frequency of the circuit of Fig. 2 and is given by the following expression:

$$\omega_{\mathrm{LO}} = \frac{\omega_0}{\sqrt{2}} \cdot \sqrt{1+\mathrm{Q_f^2}\left(\frac{\mathrm{C}}{\mathrm{C_{tank}}}-1\right)+\sqrt{4\mathrm{Q_f^2}+\left(1+\mathrm{Q_f^2}\left(\frac{\mathrm{C}}{\mathrm{C_{tank}}}-1\right)\right)^2}} \tag{5}$$

where $\omega_0 = 1/\sqrt{\mathrm{C_{tank}L_{tank}}}$ represents the resonant frequency of the classical *LC* oscillator and $\mathrm{Q_f}$ is given by (4) with $\omega_{\mathrm{LO}} = \omega_0$. ω_{LO} was computed as a function of C with (5) and is shown in Fig. 4. The curve has the same behavior as that of the capacitance $\mathrm{C_{eq}}$ showing a reduction of the slope for high values of C. In this zone the sensitivity of the output frequency to the capacitance C is small and consequently a very fine frequency tuning can be obtained. If $\mathrm{C} \gg \mathrm{gm}/2(\omega_0)$ the previous equation can be simplified as

$$\omega_{\mathrm{LO}} \approx \omega_0\sqrt{1+\mathrm{Q_f^2}\frac{\mathrm{C}}{\mathrm{C_{tank}}}}. \tag{6}$$

From (6) it follows also that

$$\frac{\delta\omega_{\mathrm{LO}}}{\omega_{\mathrm{LO}}} \approx -\frac{\delta\mathrm{C}\mathrm{Q_f^2}}{2\mathrm{C_{tank}}} = -\frac{\delta C_{\mathrm{eq}}}{2\mathrm{C_{tank}}}. \tag{7}$$

This expression has the same form as (1) which applies to the case in which the tuning is performed acting directly on the tank capacitance. The key difference is that in this case the frequency shift is magnified by a factor $\mathrm{Q_f^2}$ that is generally much smaller than one (e.g., 1/200). This means that the amount of capacitance necessary to obtain the same frequency shift is $1/\mathrm{Q_f^2}$ larger than $\delta\mathrm{C_{tank}}$.

C. Phase Noise

The analysis presented has demonstrated that the shrinking effect exploited to perform the fine tuning produces a negative capacitance in parallel to the tank with a quality factor $\mathrm{Q_f}$ much lower than one. The presence of a capacitance with a poor quality factor would suggest a degradation in the phase noise of the oscillator. However it can be proven that, if the capacitance C is sufficiently large, the oscillator operates as a traditional one without any penalty on the total output noise. This result has been verified simulating the phase noise at a fixed frequency offset for different values of C. From the plot of Fig. 5, it can be seen that when C is much greater than 2 pF (corresponding to the condition $\mathrm{C} \gg \mathrm{g_m}/(2\omega_{\mathrm{LO}})$), the phase noise obtained is almost equal to the one without capacitive degeneration. Actually, for lower values of C, the phase noise shows a slight improvement compared with the standard oscillator. However, no attempt was made to take advantage of this mechanism since it corresponds to a region that does not provide an adequate shrinking factor. In Appendix I, a quantitative analysis that makes use of the *impulse sensitivity functions* (ISF) [12] is also reported, providing a comparison with the results obtained by Andreani *et al.* for the classic *LC* tank topology [13].

The negligible effect of the shrinking capacitance technique on the total output noise could be erroneously justified by the fact that the added capacitance is small and thus, although it has a poor quality factor, does not significantly affect the tank losses. According to this reasoning, adding in parallel to the tank a capacitance C in series with a positive conductance $\mathrm{g_{m2}}/2$ (instead of negative one as in Fig. 2) could appear another good way to exploit the shrinking principle. However, as demonstrated in Appendix II, this last approach would produce a phase noise degradation of about 3 dB.

III. Fine Tuning Range and Calibration

Since it is very difficult to guarantee a continuity between the fine and coarse tuning characteristics, the fine tuning circuit must have a range able to maintain the PLL locked without using the coarse-tuning bank. In the case of a GSM transmitter, considering modulation and thermal drifts, the above condition is satisfied with a fine-tuning range of a few MHz, (800 kHz were assumed in [2]).

A. Fine Tuning Range

The range of frequency-tuning achievable when the tuning is performed directly at the tank is limited by the parasitic

capacitance and the quality factor used for the resonator [8]. On the other hand, in this case the tuning is limited by the range of the capacitance C_{eq} that can be synthesized in parallel to C_{tank}. From (2) it can be verified that the magnitude of the capacitance C_{eq} cannot exceed $C_{eq,max} = g_m/4\omega_{LO}$ (when $C = g_m/(2\omega_{LO})$). For this reason, independently to the size of the capacitance C used, the maximum tuning range $\Delta\omega_{fine,max}/\omega_{LO}$ is limited and given by

$$\frac{\Delta\omega_{fine,max}}{\omega_{LO}} = \frac{\Delta C_{eq,max}}{2C_{tank}} = \frac{g_m}{8\omega_{LO}C_{tank}}. \quad (8)$$

For a given tank and ω_{LO} the only possibility to enlarge the fine tuning range is to increase g_m and consequently the power consumption. However, according to (4), this strategy would reduce the shrinking factor. The only way to avoid that is to enlarge also C with a consequent increment of the design area.

Assuming $C_{tank} = 3.5$ pF and $g_m = 10$ mS, the maximum tuning range is slightly greater than 50 MHz, according to the plot in Fig. 4. However, the curve in Fig. 4 shows also that for values of C close to $g_m/(2\omega_{LO})$, the characteristic becomes quite non-linear. Therefore, to keep the DCO characteristic sufficiently linear, the usable tuning range cannot exceed more than about 20% of $\Delta\omega_{fine}$ (e.g., in this case 10 MHz).

B. Calibration Scheme

In the scheme of Fig. 1, the transconductance of M1 and M2 has to be large enough to sustain the oscillations but sufficiently small to give the required shrinking factor. This trade off does not allow an easy optimization of the structure since for a given g_m (as required to compensate the tank losses) and shrinking factor, C is univocally defined from (4), giving no degree of freedom. For example, when the resonator quality factor becomes low, g_m must become large leading to excessively large values for C.

These problems can be solved adopting the solution of Fig. 6 where a second cross-coupled transistors pair is added in parallel to M1-M2. The role of M3-M4 is to add an extra degree of freedom in the structure that allows to choose the most suitable values for the g_m of M1-M2 and C, without the constraint $g_{m_{eq}} > 2/R_{loss}$ present in the scheme of Fig. 1. In this implementation, while I_1 controls the transconductance for M1-M2 (defining Q_f and the DCO frequency resolution), I_2 controls the total negative resistance (defining the oscillation amplitude and the phase noise). In addition, the modified structure not only allows a better design optimization of the DCO, but at the same time offers an easy way to calibrate the fine tuning characteristic compensating process and temperature variations.

C. Class-C Operation

The transistors of the cross-coupled pairs can be biased to work always in the saturation region (Fig. 6), operating in Class-C as proposed by Mazzanti *et al.* [9]. Although this choice is not mandatory, it reduces the phase noise and at the same time increases the average transconductance of the differential pair, lowering the current I_1 necessary for a given shrinking factor. To operate in class-C, the bias voltages V_{b1} and V_{b2} (Fig. 6) have to be lowered with respect to the supply voltage. There is a lower bound for the value of V_{b1} and V_{b2}

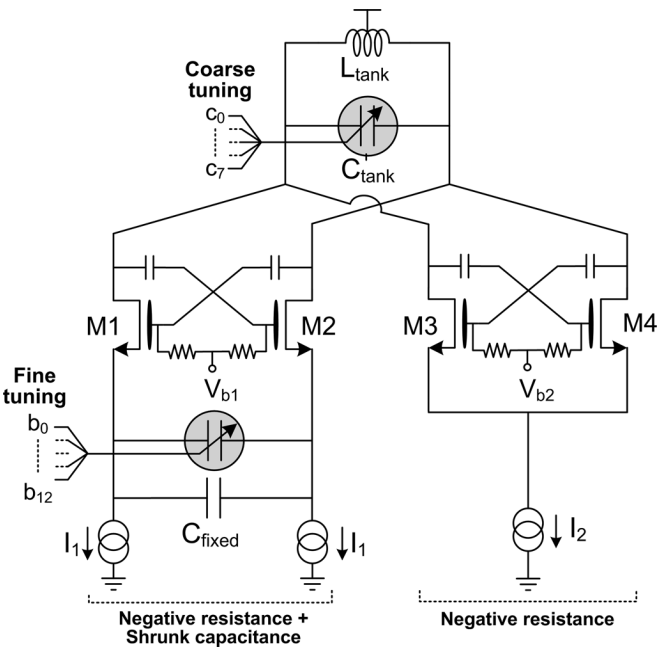

Fig. 6. Partial capacitive degeneration.

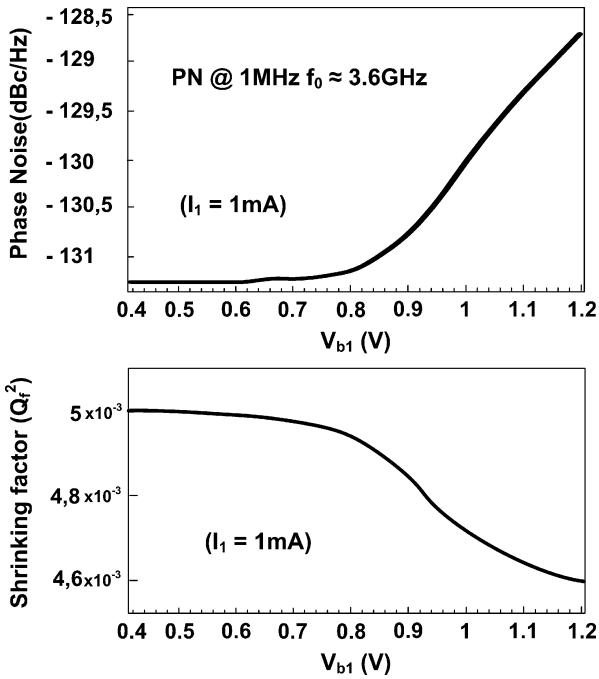

Fig. 7. Phase noise and tuning range versus V_{b1} (with M3–M4 in class-C).

related to the voltage drop reserved to the current generators I_1 and I_2. The plots in Fig. 7 confirm that for a given I_1 (1 mA), when V_{b1} is low (M1-M2 in saturation region), the phase noise reaches the minimum while Q_f^2 is maximized.

IV. DCO Prototype

To validate the presented theory, a DCO based on the scheme in Fig. 6 was realized with an 8 bits coarse array and a 13 bits fine array. The DCO was tailored to GSM application, with a center frequency of 3.6 GHz in order to provide quadrature signals at 1.8 GHz through a frequency divider.

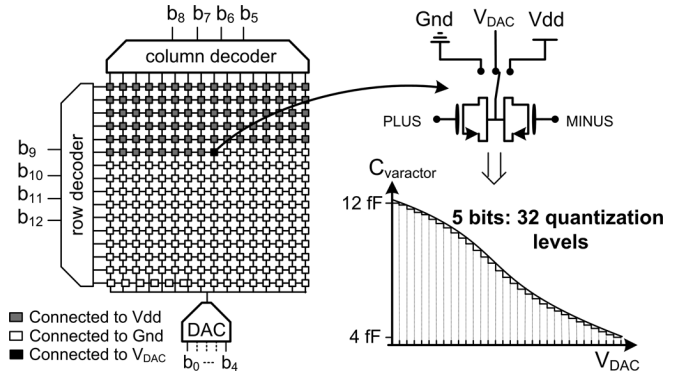

Fig. 8. Fine-tuning bank.

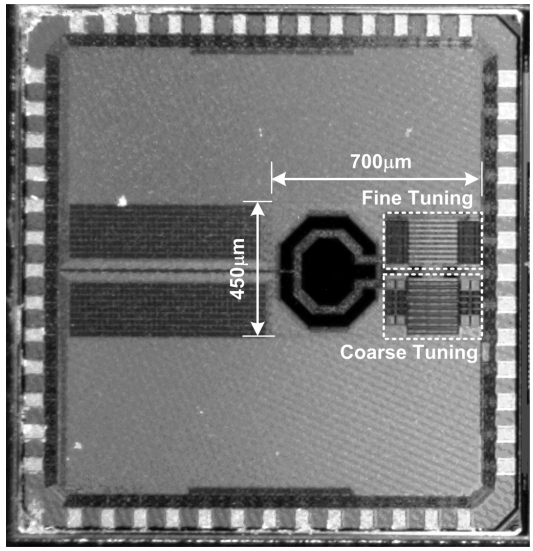

Fig. 9. Chip photograph.

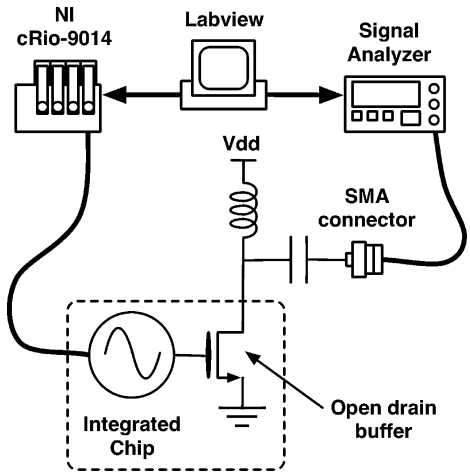

Fig. 10. Measurement setup.

The tank was realized using a differential inductor of 490 pH with a simulated quality factor of 18. For the coarse tuning bank a Metal-Oxide-Metal (MoM) capacitor matrix was implemented. The 3 LSBs of this bank were substituted by a varactor to be able to close the DCO in an analog PLL during some testing phases. This was necessary since the prototype was not inserted in any ADPLL. However the capacitive load required by the fully-digital implementation was preserved.

As described in Section III, the two cross-coupled pairs were both biased to operate in class-C. The voltage reference connected to the gates was filtered to avoid any additional noise injected by the bias.

The fine tuning bank was realized as reported in Fig. 8. The 8 most significant bits (MSB) were used to control a matrix of 16×16 varactors. All elements except one are connected either to the voltage supply ($\mathrm{V_{dd}}$) or to ground generating a thermometric filling of the matrix (gray and white units). The remaining varactor (black element in Fig. 8) is connected to the output of a 5-bits digital-to-analog converter (DAC) which provides 32 additional voltage levels between $\mathrm{V_{dd}}$ and ground. Since only one varactor is biased in the point of its characteristic with a high voltage-to-frequency gain, the sensitivity of the oscillator to noise and spurious signals coupled at the DAC output is minimized. Although the quantization of the varactor characteristic is not strictly required to reach the target fine frequency resolution this approach was adopted to simplify the routing of the matrix.

V. Measurement Results

The DCO prototype was fabricated in a 65 nm CMOS process using only the standard devices provided by the technology. The die was bonded on a dedicated RF board, with gold plated micro-strips on an FR4 substrate, where appropriately dimensioned 50 Ω strip lines carry the input signal from the SMA interconnectors to the die itself.

The prototype photograph is shown in Fig. 9, where it is also possible to identify the different building blocks. The DCO occupies an area of 0.32 $\mathrm{mm^2}$, dominated by the inductor and the two capacitors banks. The presence of a shrinking factor can be appreciated noting that the coarse and fine tuning banks have approximately the same size although they realize a different tuning range (780 MHz for the coarse bank and below 10 MHz for the fine bank). The unitary elements used for the fine tuning bank are nMOS varactors with a capacitance that varies from a minimum of 4 fF to a maximum of 12 fF. The DCO has a voltage supply of 1.8 V with a total current consumption of 16 mA, necessary to have a phase-noise of $-127.5\,\mathrm{dBc/Hz}$ @ 1 MHz offset (in line with the state of the art for GSM applications [2]). The 16 mA are divided between the two cross coupled pairs and the ratio between the two depends upon the desired shrinking factor.

The complete scheme of the measurement setup is reported in Fig. 10. The prototype includes a open-drain buffer that is directly connected to the 50 Ω input of a Rhode-Schwarz FSQ8 signal analyzer. The delivered power to the signal analyzer was around $-6\,\mathrm{dBm}$. The measurement setup is automatically controlled by Labview® driving the prototype through a real-time controller NI cRio-9014. In Fig. 11 the measured fine-tuning characteristic is reported, showing a very good agreement with the theory. The shrinking factor is around 200 with a fine-tuning range of 2.160 MHz and an averaged resolution of 300 Hz (minimum 150 Hz). In this case the current drawn by the fine-tuning branch ($\mathrm{I_1}$) is around 500 μA.

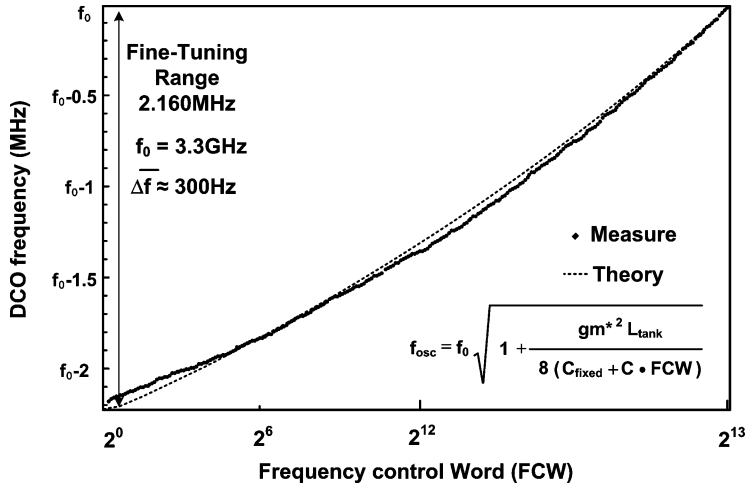

Fig. 11. Measured fine-tuning characteristic with $f_0 = 3.3$ GHz (shrinking factor of 200).

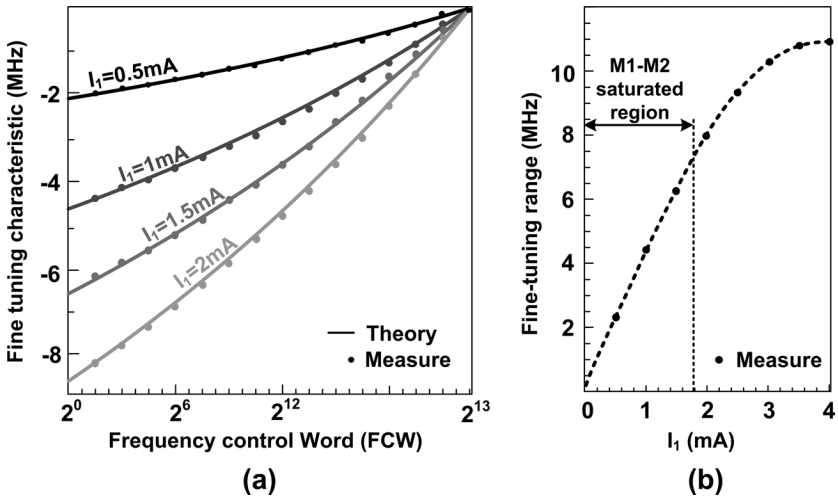

Fig. 12. Fine tuning characteristic versus I_1.

As stated in the previous section, acting on the current I_1 allows an agile calibration of the fine-tuning resolution. In addition to this, the possibility to change the DCO resolution keeping constant the number of bits allows to re-use the same oscillator for different standards that required the same number of bits but different tuning range and frequency resolution (e.g., GSM and UMTS). The DCO fine-tuning characteristics for different values of the bias current I_1 are reported in Fig. 12(a). Also in this case a very good agreement with the theory was obtained. The tuning range and the frequency resolution vary respectively from 2 MHz to 12 MHz and from a minimum of 150 Hz to a minimum of 800 Hz. The plot in Fig. 12(b) shows that the tuning range depends almost linearly on the bias current I_1 until 8 MHz. This is due to the fact that the transistor transconductance g_m in the saturated region is almost proportional to $\sqrt{I_1}$ and consequently the shrinking factor grows linearly with I_1 (being Q_f proportional to g_m^2). The tuning range versus frequency starts to becoming non linear for a current level that puts the auxiliary switching pair out of the saturation region during part of the oscillation period (no more class-C operation).

The DCO phase noise measured by a Rhode-Schwarz FSQ8 signal analyzer is reported in Fig. 13. Due to the relatively low quality factor of the tank, estimated to be around 10 due to parasitic resistance in the tank layout, the phase noise at 1 MHz away from the carrier is -127.5 dBc/Hz at 3.3 GHz. Notice that, due to the low output power delivered by the output buffer, the instrument noise floor affects the phase-noise measure far from the carrier. Considering the total power consumption around 28.8 mW, the DCO figure of merit (FoM) is equal to 183 dBc/Hz. All other measurements results compared with the state of the art are reported in Table I. The frequency resolution achieved is the smallest presented when no dithering is used. Furthermore the solution presented is the first one that allows re-configurability of the frequency resolution over a wide range. This property can be very attractive not only for an easy calibration of the DCO but also for the use in multistandard frequency synthesizer.

VI. Conclusions

To realize a fine tuning DCO, a capacitive degeneration has been introduced in the classic *LC* oscillator. This capacitance is

TABLE I
SUMMARY RESULTS AND COMPARISON WITH THE STATE OF THE ART

	This work	[1]	[2]	[3]	[4]	[5]
Center Frequency [GHz]	**3**	3.6	7.75	1.7	4	3.35
Tuning Range [MHz]	**780 (26%)**	900 (25%)	2800 (36%)	132 (8%)	1000 (25%)	600 (18%)
Fine Frequency Resolution [kHz]	**0.15-1.5**[(a)]	12[(b)]	0.8	150	200	5
Fine Freq. Range [MHz]	**2-12**[(a)] **(13 bits)**	0.8 (6 bits)	0.6 (9 bits)	132 (10 bits)	200 (10 bits)	10 (11 bits)
Voltage Supply [V]	**1.8**	1.4	1.2	0.5	2.5	1.2
Current Consumption [mA]	**16**	18	16	0.372	3.2	2
PN @1 MHz [dBc/Hz]	**-127.5**	-126	-118	-109	-114	-118
FoM [dBc/Hz]	**183**	183	183	181	177	185
Technology	**65 nm**	90 nm	65 nm	130 nm	130 nm	90 nm

(a) Tunable acting on I_1
(b) Without dithering

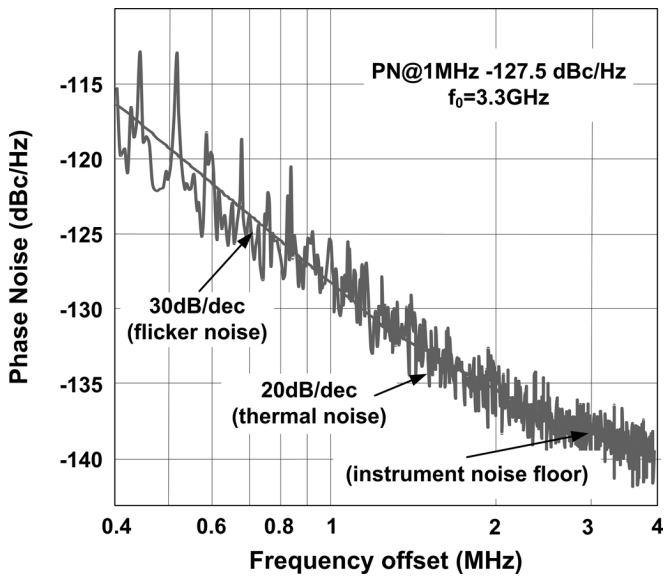

Fig. 13. Output phase-noise measure.

reflected in parallel to the tank shrunk by a factor proportional to the transconductance used in the cross-coupled pair. This allows to perform a fine frequency tuning with a resolution that is not limited by the unitary element present in the capacitor banks.

The theory presented has demonstrated the potentialities and the limits of the structure while the measurements on prototype for GSM application have proved its robustness.

APPENDIX I

As described by Hajimiri and Lee [12], the phase noise in the $1/f^2$ region caused by a white noise source, at the offset frequency $\Delta\omega$, depends on the ISF and it is given by

$$L\{\Delta\omega\} = 10\log\left(\frac{\Gamma_{\rm rms}^2}{q_{\rm max}^2}\frac{\frac{\overline{i_n^2}}{\Delta f}}{4\Delta\omega^2}\right) \tag{9}$$

where $q_{\rm max}$ is the maximum amount of dynamic charge loaded into the tank capacitance, $i_n^2/\Delta f$ is the white power spectral density of the noise current and $\Gamma_{\rm rms}^2$ is the square of the *impulse sensitivity function* (ISF) $\Gamma(\varphi)$.

Starting from the scheme in Fig. 14, the effect of the fine tuning capacitance C on the output phase noise is derived evaluating the ISF of the cross-coupled transistor (i.e., $\Gamma_{\rm M1}(\varphi)\Gamma_{\rm M2}(\varphi)$ with $\Gamma_{\rm M1}(\varphi) = -\Gamma_{\rm M2}(\varphi)$) and of the bias current generators (i.e., $\Gamma_{\rm Mtail1}(\varphi)$ and $\Gamma_{\rm Mtail2}(\varphi)$ with $\Gamma_{\rm Mtail1}(\varphi) = -\Gamma_{\rm Mtail2}(\varphi)$). The phase noise associated with the finite quality factor of the tank is not considered because it does not change with the capacitive degeneration of the switching pair.

Referring to transistor M1 in Fig. 14, to find $\Gamma_{\rm M1}(\varphi)$, the analysis distinguishes three different cases related to the operation mode of the differential pair, each of which is associated with a different ISF, i.e., both transistors work in saturation or one of them is turned off. However, the phase noise contribution of M1 differs from the classical oscillator scheme only when both transistors are carrying current, because in the other cases the *impulse sensitivity function* is zero in both oscillator architectures [13].

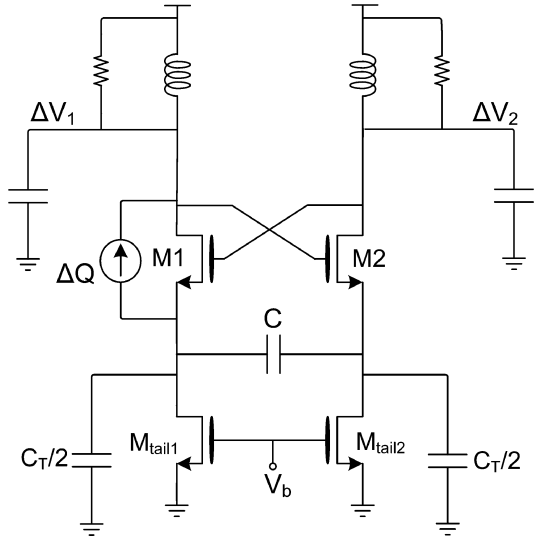

Fig. 14. ISF derivation in degenerate *LC* oscillator.

When the two transistors work in saturation region, the noise charge impulse ΔQ present between the drain and source of M1 produces a voltage difference between the DCO outputs that corresponds to the following Γ function

$$\Gamma_{\mathrm{M1}}(\phi) = \frac{\cos\phi}{2}\frac{2gm_2(\phi)}{\left(1+\frac{C_T}{C}\right)gm_1(\phi)+gm_2(\phi)} \tag{10}$$

where C_T is the parasitic capacitance at the source of M1–M2. This result is very similar to the one obtained by Andreani *et al.* for a the classical oscillator is given by

$$\Gamma_{\mathrm{M1}}(\phi) = \frac{\cos\phi}{2}\frac{2gm_2(\phi)}{gm_1(\phi)+gm_2(\phi)}. \tag{11}$$

Equation (10) differs from (11) for the presence in the denominator of the term $g_{m1}\cdot C_T/C$ which reduces the effect of the switching transistors on the phase noise. However, as explained in Section II, to sustain the oscillation and to achieve the desired resolution, C should be much greater than C_T making the difference between (10) and (11) negligible.

An analogous approach can be used to find the ISF of the bias current generators ($\Gamma_{\mathrm{Mtail1}}(\varphi) = -\Gamma_{\mathrm{Mtail2}}(\varphi)$). Once again it can be proved that the new ISFs differ from the classical one ($\Gamma_{\mathrm{tail}}(\varphi)$) only when both transistor are on, being

$$\Gamma_{\mathrm{Mtail1}}(\phi) = \frac{\cos\phi}{2}\frac{\mathrm{gm_1}(\phi)\left(1+\frac{C_T}{C}\right)-gm_2(\phi)}{gm_1(\phi)\left(1+\frac{C_T}{C}\right)-gm_2(\phi)} \tag{12}$$

and from [13]

$$\Gamma_{\mathrm{tail}}(\phi) = \frac{\cos\phi}{2}\frac{\mathrm{gm_1}(\phi)-gm_2(\phi)}{gm_1(\phi)+gm_2(\phi)}. \tag{13}$$

Equation (12) contains once again the factor $g_{m1}\cdot C_T/C$ that is not present in (13), in this case both at the numerator and at the denominator. As explained before, their contribution is irrelevant for the large C used.

When only one transistor of the cross-coupled pair is on, the large capacitance C ($C \gg g_{m1}/\omega_{LO}$) produces a short between M_{tail1} and M_{tail2} making the ISF equal to one like for the classical case [13].

Appendix II

The contribution to the DCO phase noise due to the use of a positive conductance $g_{m2}/2$ can be evaluated starting from the expression of the phase noise of a traditional *LC* oscillator [13]. In particular, this conductance is reflected in parallel to the tank obtaining

$$\mathrm{L}\{\Delta\omega\} = L_{classic}\{\Delta\omega\} + 10\log\left[1+\frac{\mathrm{R}g_{m2}}{2}\right] \tag{14}$$

where $L_{classic}\{\Delta\omega\}$ is the phase noise of the classic *LC* tank oscillator and R represents the tank losses. Contrary to the solution proposed (that does not have any effect on the phase-noise performance), in this case a degradation proportional to the conductance g_{m2} occurs. Since the value of g_{m2} sets a constraint on the maximum fine-tuning range available ((8)) it is better to rewrite (14) as follows

$$\mathrm{L}\{\Delta\omega\} = L_{classic}\{\Delta\omega\} + 10\log\left[1+4\mathrm{Q_T}\frac{\Delta\omega_{\mathrm{fine}}}{\omega_{\mathrm{LO}}}\right] \tag{15}$$

where g_{m2} is given by (8) and Q_T is the quality factor of the original resonator (i.e., $R\omega_{LO}C_{tank}$). From (15) it is clear that no penalty on the total outputs phase noise can be obtained only in the limit of a fine tuning range that approaches zero. In comparison with the solution proposed, assuming for the tank $Q_T = 18$, $\omega_{LO} = 3.6$ GHz and $\Delta\omega_{fine} = 50$ MHz (which correspond to a usable tuning range of 10 MHz) the degradation of the phase noise is around 3 dB. This penalty is even worse if the Q_T and/or the tuning range are increased.

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References

[1] R. B. Staszewski and P. T. Balsara, *All-Digital Frequency Synthesizer in Deep-Submicron CMOS*. New York: Wiley Interscience, 2006.
[2] Staszewski *et al.*, "A digitally controlled oscillator in a 90 nm digital CMOS process for mobile phones," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2203–2211, Nov. 2005.
[3] Hung *et al.*, "A digitally controlled oscillator system for SAW-less transmitters in cellular handsets," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pp. 1160–1170, May 2006.
[4] A. Chen *et al.*, "9 GHz dual-mode digitally controlled oscillator for GSM/UMTS transceivers in 65 nm CMOS," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC'07)*, 2007, pp. 432–435.
[5] J. H. Han and S. H. Cho, "Digitally controlled oscillator with high frequency resolution using novel varactor bank," *Electronics Lett.*, vol. 44, no. 25, pp. 1450–1452, 2007.
[6] J. Zhuang *et al.*, "A 3.3 GHz LC-based digitally controlled oscillator with 5 kHz frequency resolution," in *Proc. IEEE Asian Solid-State Circuits Conf. (ASSCC'07)*, 2007, pp. 428–431.
[7] Pletcher and Rabaey, "A 100 μW, 1.9 GHz oscillator with fully digital frequency tuning," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2005, pp. 387–390.
[8] T. H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge University Press, 1998.
[9] Mazzanti and Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[10] F. O'Mahony *et al.*, "A 27 Gb/s forwarded-clock I/O receiver using an injection-locked LC-DCO in 45 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 2008, pp. 452, 627.
[11] Pittorino *et al.*, "A UMTS-compliant fully digitally controlled oscillator with 100 MHz fine-tuning range in 0.13μm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig.*, 2006, pp. 770–779.
[12] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
[13] P. Andreani *et al.*, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

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