# A complete DVB-T/ATSC tuner analog base-band implemented with a single filtering ADC

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***Abstract*—A filtering ADC used to implement the complete base-band in a receiver chain is presented. Passive filtering and in-band noise shaping lead to a frequency dependent dynamic range that better fits with the system requirements of a wireless receiver. The 90nm CMOS prototype is embedded in a fully integrated tuner compliant with DVB-T and ATSC standards. For a 6MHz channel bandwidth, the filtering ADC exhibits a frequency dependent dynamic range varying from 75.6dB to 90dB while drawing 30mA from a 1.8V supply.**

## I. INTRODUCTION

The analog base-band in a receiver chain is generally a cascade of filtering and variable-gain stages that minimize the dynamic range required at the input of the analog-to-digital converter (ADC) (Fig. 1). Although the presence of several building blocks allows an easier optimization of the receiver, this strategy is paid in terms of flexibility and design complexity. The path towards a software-defined radio (SDR) goes through the reduction of the base-band analog section of a wireless receiver in favor to a more flexible digital one. This operation is realized moving the ADC as close as possible to the antenna (Fig. 1).

In wireless applications, the replacement of the entire analog base-band with a single ADC is limited by the capability of the converter to detect a small signal surrounded by strong interferers [1]. One of the possibilities to overcome this problem is to embed into the ADC the filtering action necessary to prevent the saturation of the quantizer [2]. However, this operation must be achieved without producing an increase of the in-band noise or the power consumption with respect to the filter-ADC cascade.

In this paper an ADC implementing the entire analog base-band of a DVB-T/ATSC tuner is presented. The proposed solution combines in the same feedback loop interferer filtering and signal digitization (Fig. 2). The high dynamic range required to place the ADC directly at the mixer output is obtained exploiting three intrinsic properties of the structure of Fig. 2. First, a grounded capacitance at the input of the ADC absorbs the largest part of the out-of-band interferers coming

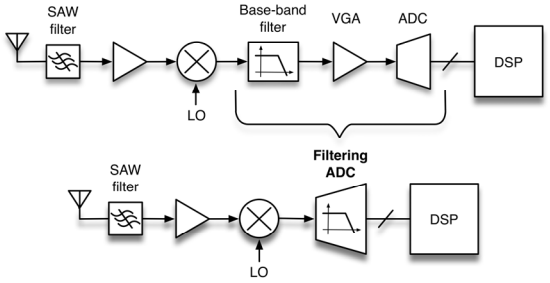


Figure 1. Towards a more flexible software defined radio

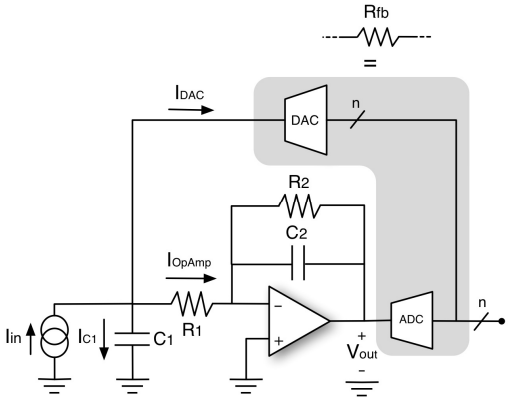


Figure 2. Proposed filtering ADC base-band

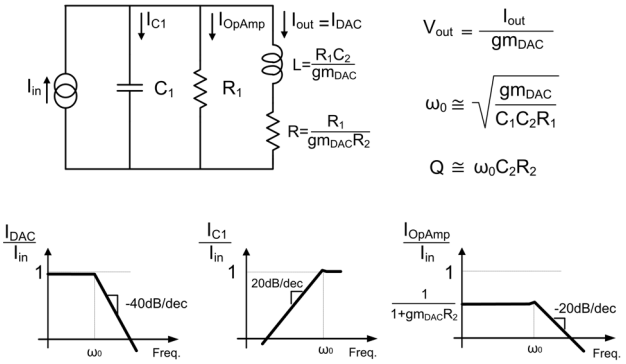


Figure 3. LRC model for signal transfer function analysis

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from the mixer. Second, both analog and quantization noise benefit from an in-band shaping that is not present when the filter is placed in front of the ADC. Third, the digital-to-analog converter (DAC) feedback path allows to synthesize a couple of complex conjugate poles leading to a steeper filtering profile than a simple two-real-poles cascade. In this sense, the proposed solution can be seen as a further step with respect to the base-band architectures recently proposed in [3] and [4] in the direction of improving the immunity to out-of-band blockers.

The paper is structured as follows. In section II, the filtering ADC transfer function is derived providing a comparison with the state of the art base-band architectures in terms of immunity to interferers. In section III both analog and quantization noise are computed highlighting the advantages of the proposed solution compared to a classic filter-ADC cascade. In section IV, the implementation of a DVB-T/ATSC tuner, the measurement results and a comparison with the state of the art of filtering ADC are finally discussed.

## II. FILTERING ADC

The proposed filtering ADC shown in Fig. 2 derives from a current driven biquad cell in which the main feedback resistance ($R_{fb}$) has been replaced by the cascade of an ADC and a DAC. Both input and output signals are currents with $I_{in}$ representing the down-converted signal coming from the mixer and $I_{out}$ the current absorbed by the DAC.

### *A. Signal transfer function*

To evaluate the filtering ADC transfer functions, the ADC-DAC cascade can be modeled with a transconductor whose transconductance ($gm_{DAC}$) is given by the ratio between the full-scale current of the DAC and the full-scale reference voltage of the ADC. Under this assumption, the filter embedded in the ADC is equivalent to an LRC shunt network (Fig. 3) whose output signal is the current flowing into the inductance. The equivalent inductance is equal to $R_1C_2/gm_{DAC}$ with a quality factor proportional to the damping resistor $R_2$.

The realized signal transfer function $I_{out}/I_{in}$ is a 2nd order low-pass biquad with in-band gain $G=gm_{DAC}R_2/(1+gm_{DAC}R_2)$ and $\omega_0$, Q given by:

$$\omega_0 = \sqrt{\frac{1+gm_{DAC}R_2}{C_1R_1C_2R_2}} \qquad (1)$$

$$Q = \omega_0 \frac{C_1R_1C_2R_2}{C_1R_1+C_2R_2} \qquad (2)$$

In Fig 3 the transfer functions from the input current to the current into the DAC, the current into the capacitor $C_1$ and the current into the operational amplifier (OA) are shown. While the DAC current experiences a second order

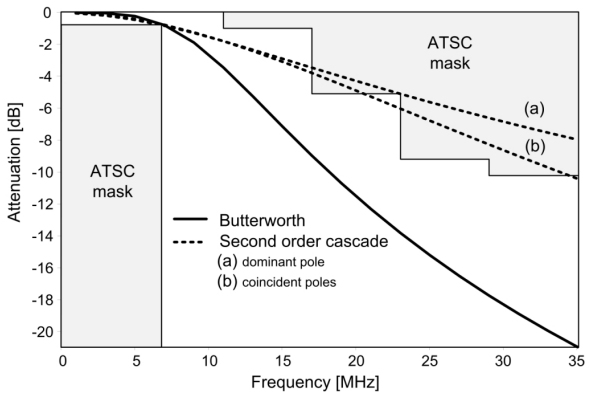


Figure 4. Comparison between a Butterworth and a second order cascaded solution

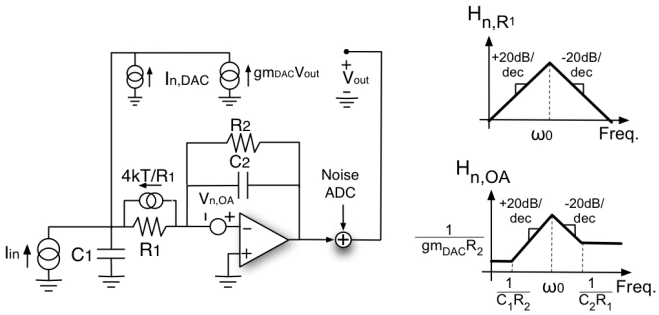


Figure 5. Noise sources and analog transfer functions

filtering, the current absorbed by the OA undergoes a first order filtering. The presence of the grounded capacitance $C_1$ ensures that the out-of-band interferers managed by the DAC and the OA are smaller than the ones present at the input of the base-band. From this point of view the proposed solution differs from existing filtering-ADC architectures where all the input current (coming from the mixer) must be absorbed by the active devices, making the first integrator the most power hungry element of the converter [2].

### *B. Proposed solution versus state of the art base-band*

In recent works, the handling of out-of-band interferers has been solved inserting an RC passive filter directly at the output of the RX mixer, followed by an additional active lossy integrator [3], [4]. Necessarily, this results into a two-real-poles cascade as opposed to the possibility of implementing conjugated complex poles that is available in the solution proposed here. Due to this, the advantage of the proposed architecture with respect to previous ones ([3], [4]) is a more selective filtering profile for the same in band flatness. The quantitative amount of such an advantage can be appreciated in Fig. 4 where different two-real-poles transfer functions (with different poles positions) and a second order Butterworth one are shown together with the filter mask required by an ATSC receiver. It turns out that the ATSC mask, that requires a 0.8dB maximum in band drooping and 9dB attenuation at 3.3 times the 7MHz signal bandwidth corner, can be satisfied only by a complex transfer function.

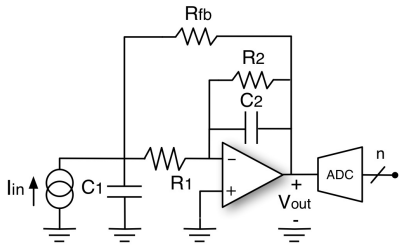


Figure 6. Filter ADC cascade

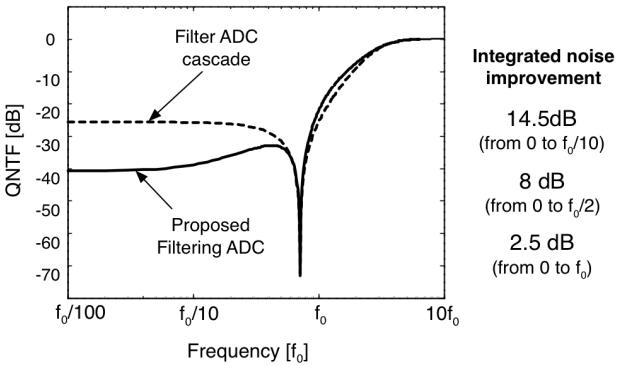


Figure 7. Quantization noise transfer function comparison (the ADC block is a 2nd order wideband ΣΔ with an in-band notch)

## III. NOISE IN THE FILTERING ADC

The filtering ADC topology presents further benefits with respect to noise, since the in-band loop gain of the main feedback compresses the noise of the filter and of the ADC.

The main noise sources of the filtering ADC, and its equivalent continuous time model, are reported in Fig. 5. The principal noise contributors are the resistor $R_1$, the OA, the feedback DAC and the ADC. With the exception of the DAC, that injects its noise directly at the input node, all the other noise sources have an in-band zero in their transfer functions (Fig. 5). For both digital (quantization) and analog ADC noise, this is the direct consequence of having inserted the ADC in the loop used to synthesize the complex poles. For the other noise sources, the high pass noise shaping is due to the intrinsic mechanism of current filters (proposed by Pirola et al. [5]) that occurs because the DAC senses the output signal as a current.

In terms of noise, it is difficult to make a comparison between the proposed solution and the two-real-poles cascade topology used in [3] and [4]. This because having different signal transfer functions the noise affects the final dynamic range in a different way. A fairer and more general comparison is carried on between the filtering ADC and the cascade of a filter and an ADC. The cascade is realized as depicted in Fig. 6, where the DAC has been substituted by a resistance placed in feedback around the OA. The two structures (Fig. 2 and Fig. 6) are compared assuming the same signal transfer function, the same impedance levels for the filter and the same OA.

For the filter noise sources (i.e. $R_1$, OA) the main difference between the two structures is the fact that the signal

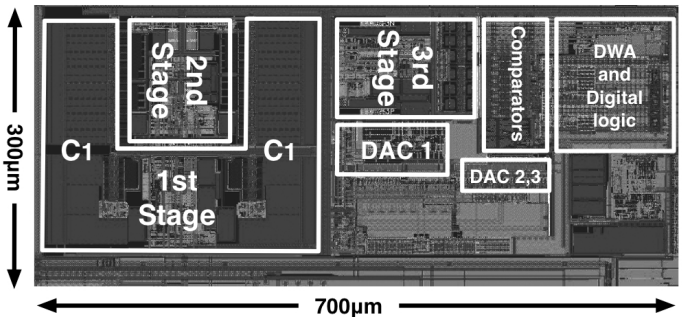


Figure 8. Filtering ADC picture

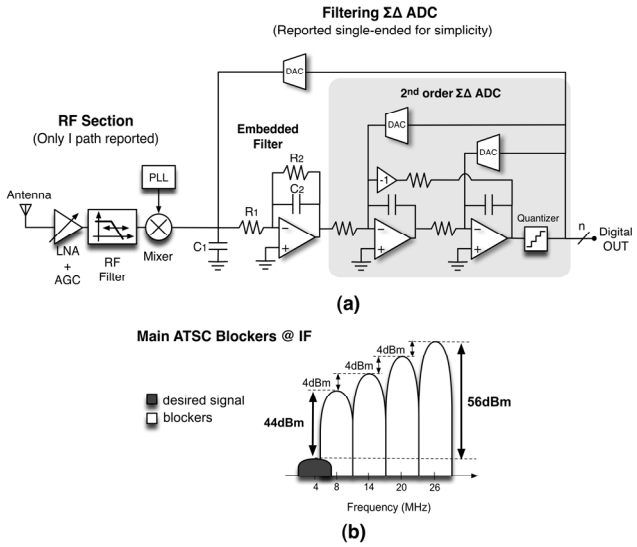


Figure 9. (a) Tuner with filtering ADC. (b) ATSC blockers profile in the 4MHz low-IF

path provided by $R_{fb}$ is bilateral while the DAC is unilateral. Due to this $R_{fb}$ gives an additional term in the noise transfer function compared with the DAC. This extra noise computed at the output of the OA is equal to the sum of the voltage noise of $R_1$ and of the OA.

The quantitative advantage in terms of quantization noise with respect to the traditional filter-ADC cascade can be appreciated from Fig. 7. The improvement depends on the noise integration bandwidth versus filtering ADC cut-off frequency $f_0$ (some examples are reported in the right side of Fig. 7). For a given channel bandwidth, a trade-off between noise and frequency selectivity occurs since a higher cut-off frequency reduces the in-band noise but at the same time diminishes the out-of-band blocker attenuation.

The actual topology of the filtering ADC is obtained substituting the ADC block (Fig. 2) with a second order wideband Sigma-Delta with an in-band notch. Notice that, although the topology appears very close to the ADC proposed by Straayer et al. [6], they implement a different signal transfer function. While our ADC is narrow-band, the previous one is wide-band. In fact the low frequency $R_1C_1$ pole is introduced only to attenuate the large current pulses coming from the DAC and its effect on the signal transfer function is cancelled introducing a zero in the OA feedback.

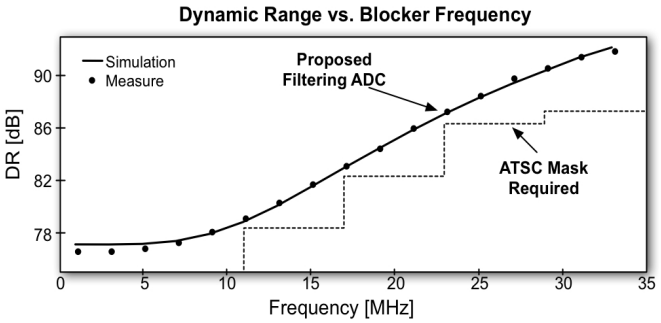


Figure 10. Dynamic range versus blocker frequency

## IV. MEASUREMENT RESULTS

The proposed filtering ADC was integrated in a reconfigurable quadrature DVB-T/ATSC tuner fabricated in a 90nm CMOS process (Fig. 8). A simplified schematic of the receiver chain is reported in Fig. 9.a (without quadrature path). To better understand the critical interferer scenario handled by the filtering ADC, the signals power profile appearing at the mixer output is also reported (Fig. 9.b). The ATSC standard presents adjacent channel interferers that can have an average power up to 56dB higher than the in band signal power (N+5 channel). Furthermore, the used low-IF architecture reduces the relative frequency offset of the undesired blockers from the channel bandwidth.

The filtering-ADC dynamic range versus frequency is reported in Fig. 10. The DR is defined as the ratio between the maximum signal that can be handled at each frequency and the integrated in-band noise (1MHz-7MHz). The maximum signal is defined as the one that corresponds to the onset of the modulator instability. Contrary to traditional ADC, the proposed one has a frequency dependent DR that matches the blocker mask. This results in an optimized base-band whose performance perfectly fits the system requirements.

The fabricated prototype noise advantage versus a filter-ADC cascade is 7.5dB for the integrated quantization noise and 2dB for the integrated analog noise. This 2dB reduction allows to use 35% less capacitance area keeping constant both noise and voltage swing at the mixer output (as required to preserve linearity for both the mixer and the feedback DAC).

All the other measurements are reported in Table I. Due to the filtering nature of the proposed ADC, the signal-to-noise plus distortion-ratio (SNDR) also varies with frequency as the DR and therefore should be defined as explained above. The SNDR results only 1dB below the DR. The FoM is 1.03pJ/conv-step for in-band signal and becomes 0.2pJ/conv-step at 30MHz. In Table II, a comparison with the state of art of filtering ADCs is reported. The proposed solution shows the best performance both in-band and out-of-band (the latter evaluated for a frequency four times the signal bandwidth BW). Notice that for the solution proposed in [7] the maximum signal handled by the ADC is not specified and this cannot be evaluated simply looking at the signal transfer function. In fact, a filtering signal transfer function prevents the saturation of the quantizer but in principle it does not guarantee the absence of clamping in the previous stages.

TABLE I. MEASUREMENT RESULTS

| Main Parameters | | DR and FoM* | |
|---|---|---|---|
| Supply | 1.2V-1.8V | In band DR/SNDR | 75.6dB/74.6dB |
| Power | 54mW | DR/SNDR@15MHz | 81dB/80dB |
| Clock | 405MHz | DR/SNDR@30MHz | 90dB/89dB |
| Bandwidth | 1-7MHz | In band FoM | 1.03pJ/c-s |
| Technology | 90nm CMOS | FoM@15MHz | 0.55pJ/c-s |
| ADC area | 0.21mm2 | FoM@30MHz | 0.2pJ/c-s |

* FoM=Power/($2^{ENOB+1}$BW)

TABLE II. COMPARISON WITH THE STATE OF THE ART OF FILTERING ADCS

| Parameter | BW [MHz] | Fclock [MHz] | Power [mW] | SNDR peak [dB] | DR [dB] | In-band FoM [pJ/step] | Out-of-Band FoM [pJ/step] | Area [mm$^2$] | Technology |
|---|---|---|---|---|---|---|---|---|---|
| This work | 6 | 405 | 54 | 74.6 | 75.6-90 | 1.03 | 0.2 | 0.21 | 0.09µm |
| [2] | 1 | 64 | 2 | 59 | 65-71 | 1.37 | 0.7 | 0.14 | 0.18µm |
| [7] | 6.5 | 96 | 122.4 | 70.9 | 75 | 3.28 | - | 2.15 | 0.18µm |

Out-of-Band FoM evaluated at 4 times BW


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