A 90nm CMOS Gated-Ring-Oscillator-Based Vernier Time-to-Digital Converter for DPLLs

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***Abstract*—Two gated ring oscillators (GRO) act as the delay lines in an improved Vernier time-to-digital converter (TDC). The already small quantization noise of the standard Vernier TDC is further first-order shaped by the GRO operation. The TDC has been implemented in a 90nm CMOS technology and achieves a resolution better than 5ps for a signal bandwidth of 800kHz. The current consumption is 3mA from 1.2V when operating at 25MHz.**

I. Introduction

Digital phase-locked loops (DPLL) are currently a hot research topic, as they allow for more flexibility and programmability compared to their analog counterparts. In a DPLL, the digitally-controlled oscillator (DCO) phase noise and the time-to-digital converter (TDC) quantization noise dominate the out-of-band and the in-band noise, respectively.

At the DPLL output, the spectral power density S_{TDC} contributed by the TDC quantization noise within the PLL bandwidth is [1]

$$S_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{delay}}{T_{DCO}}\right)^2 \frac{1}{f_{REF}}\Delta f \,, \qquad (1)$$

where Δt_{delay} denotes the quantization time error of the TDC, T_{DCO} is the period of the DCO oscillation, and f_{REF} is frequency of the reference clock in the DPLL. Obviously, a smaller Δt_{delay} results in a lower in-band PLL noise. In a straightforward TDC, where the time resolution is determined by the delay of an inverter loaded by another (identical) inverter, the TDC quantization noise is limited by the CMOS process used. Therefore, more advanced approaches, such as the Vernier structure [2], pulse shrinking [3], and sub-exponent TDC [4] have been proposed to achieve a time resolutions that is well below the delay of the inverter itself.

A Vernier TDC uses two (instead of one) delay lines with respective inverter delay of τ_1 and τ_2. The effective time resolution Δt_{delay} is given by the delay difference $\tau_1-\tau_2$ (assuming $\tau_1>\tau_2$), which of course can be designed much smaller than τ_1. In this way, the TDC noise contribution is greatly reduced, according to (1). However, since the time resolution is now determined by a very small delay difference, a very large number of inverter stages may be required to cover a large-enough detection range. To solve this issue, a Vernier TDC based on ring oscillators rather than delay lines has been proposed [5]. Since a ring oscillator is a delay line terminated on itself, the signal can travel more than once along the delay line (i.e. the oscillator), in principle extending the detection range without limits.

Noise shaping is yet another method for reducing the in-band TDC noise contribution [6]. This type of TDC has still a coarse resolution of an inverter delay, but the corresponding relatively large quantization noise is shaped in frequency as in a first-order Delta-Sigma modulator, i.e., it is largely pushed towards higher frequencies, where it can be suppressed by the low-pass filter of the DPLL.

Considering that the coarse resolution in a GRO-based TDC is still limited by an inverter delay, a new TDC combining the Vernier approach with the GRO TDC is proposed in this work. The two delay lines in the Vernier architecture are replaced by two GROs, to achieve both a very low time quantization beyond the inverter delay, and a first-order frequency shaping of the quantization noise.

This paper is organized as follows: Section II describes the proposed GRO-based Vernier TDC, Section III details the circuit implementation, and Section IV reports the measurement results on the fabricated prototype. Conclusions are drawn in Section V.

II. Gated-Ring-Oscillator Vernier TDC

Fig. 1 shows the structure of the proposed TDC. It includes the GRO core, the phase-frequency detector (PFD), and a multi-phase counter.

The PFD senses the delay between the two inputs *REF* and *CKV* (in the context of a DPLL, these are the usual names for the reference clock and the feedback clock, respectively) and generates two enable pulses *EN_REF* and *EN_CKV* controlling the Vernier GRO core. The quantized delay generated by the GRO core is read out by the multi-phase counter.

In the TDC, *EN_REF* is always leading *EN_CKV* if the delay between *REF* and *CKV* (or vice versa) is not zero (this will be explained in detail in Section III). The GRO core (Fig. 1) consists of two 9-stage ring oscillators and a sampling block. The slow GRO (SGRO) is started by *EN_REF*, so that the fast GRO (FGRO, started by *EN_CKV*) can catch up with it in Vernier-like fashion, since the delay between the leading phase in SGRO and the leading phase in FGRO decreases by Δt_{delay} across each new delay-stage pair. When FGRO has caught up with SGRO, the state of both GROs is frozen by falling *EN_REF*/*EN_CKV*, and the number of delay cells that have experienced one (or more) rising transitions yields the quantized delay output. The capacitance at each node in SGRO/FGRO holds now the voltage value at the freezing instant (Fig. 1, bottom left), and during the next measurement cycle, each GRO starts from this state, rather than discarding it as would be the case in a standard Vernier TDC. In this way, the quantization error is accumulated across all measurements, resulting in the expected first-order shaping [6] shown in Fig. 1 (bottom right), obtained through high-level simulations in a

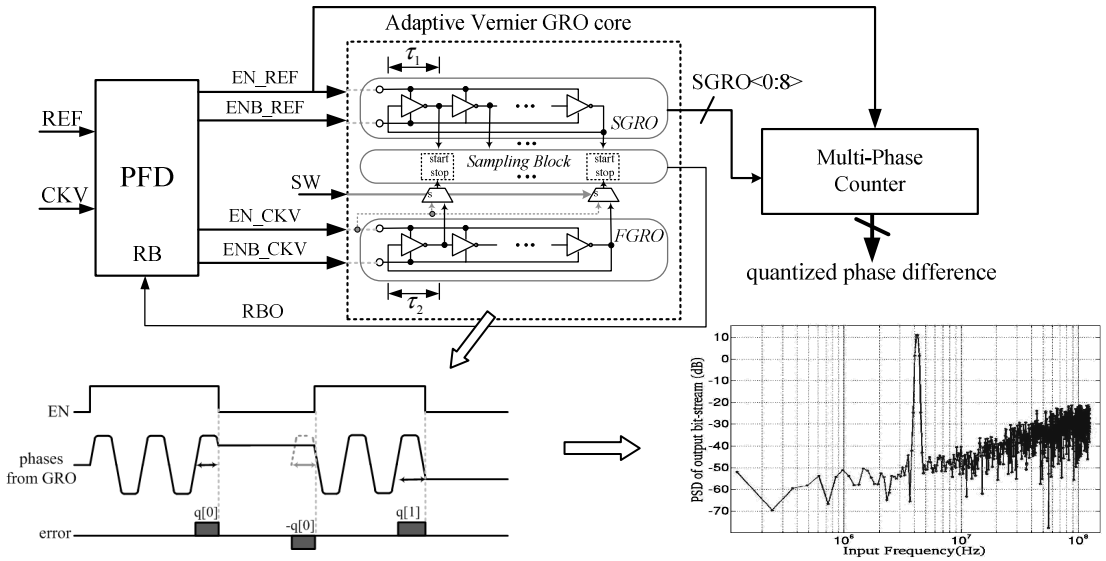


Figure.1 Block diagram of the proposed Vernier GRO TDC

Simulink platform.

Of course, an important challenge in the Vernier GRO TDC is that each measurement starts from a different SGRO/FGRO delay-cell pair, rather than always from the first pair as in a normal Vernier TDC. On the other hand, the (ideally random) rotation of the starting delay-pair cell has the additional advantage of avoiding harmonic tones due to the mismatch between the delay cells in the GROs.

The number of delay cells used by the GROs during the measurement is counted by a multi-phase counter clocked by all staggered phases from the SGRO. An enable pulse allows an accumulator to be triggered by the rising edge of the SGRO phases; at the falling edge of the enable, the counter saves the result and resets the accumulator for the next measurement.

It should be noticed that only the rising edge of the GRO phases is used in the sampling block, in order to avoid the mismatch between rise time and fall time of the inverter. It means that the Vernier time resolution is equal to twice the difference between SGRO inverter delay and FGRO inverter delay.

In the sampling block, which has the task of determining when FGRO has caught up with SGRO, each *start/stop* input pair is fed to an SR latch driving a D flip-flop, rather than directly to the D flip-flop, in order to be able to detect a delay with a narrower metastability region. However, the level sensitivity of the SR latch results in a narrow detection range, as illustrated in Fig. 2. A correct sampling is shown in Fig. 2(a), where a rising edge of *stop* catches up with a rising edge of *start*. Simulations show that even a very small lead (<1ps) for *stop* is enough to generate a valid trigger (*out*) for the D flip-flop. In fact, it is when the delay between *start* and *stop* becomes large that the SR latch may generate a faulty signal for the D flip-flop. Fig. 2(b) shows a *start-stop* delay that allows *out* to rise close to the trigger level of the D flip-flop, yet without passing it; however, if the *start-stop* delay increases further, the D flip-flop will be incorrectly triggered (Fig. 3(c)). This case may arise at the beginning of the measurement window, when the delay between *start* and *stop* is equal to delay between *REF* and *CKV*.

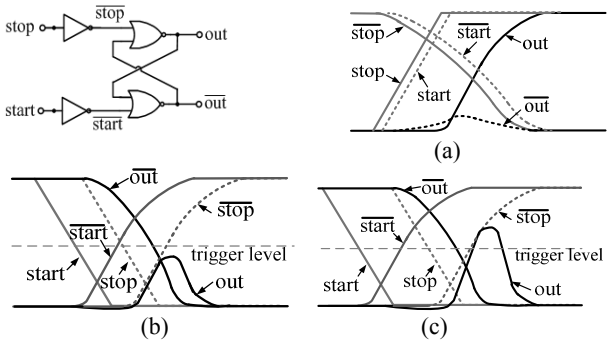


Figure. 2 SR latch: (a) Correct sampling when *stop* catches up with *start;* (b) Acceptable *start-stop* delay for correct falling-edge sampling; (c) Excessive *start-stop* delay results in faulty falling-edge sampling.

The maximum acceptable value of the *start-stop* delay, i.e. the detection range of the Vernier GRO TDC, is approx. 120ps, limited by the SR latch. Obviously, we could remove the SR latches to widen the detection range, sacrificing some of the metastability performance. A better alternative, however, is to introduce another working mode for the TDC, to both keep an excellent metastability performance, and achieve a full-period detection range as well. In this mode, all *stop* phases are replaced by *EN_CKV* (see Fig. 3), which is never high at startup, so that the situation of Fig. 2(b)-(c) never arises. In fact, in this mode the TDC works as a plain GRO TDC (i.e., using FGRO but not SGRO), with a resolution of an inverter delay, which is of course much coarser than the Vernier resolution. The consequent resolution loss can be easily compensated by increasing the gain in the DPLL loop.

III. CIRCUIT DETAILS

A. Gated-Ring-Oscillator core

To get a high Vernier time resolution, two identical ring oscillators with different frequency controls are used in the GRO core, as shown in Fig.3. In each delay cell, 15 thermometer-coded inputs (derived from a 4-bit off-chip control bus) control fifteen small unit-weight NMOS capacitors. For SGRO, all control signals are low, which results in the maximum capacitance load. The Vernier resolution is therefore determined by the control signal to

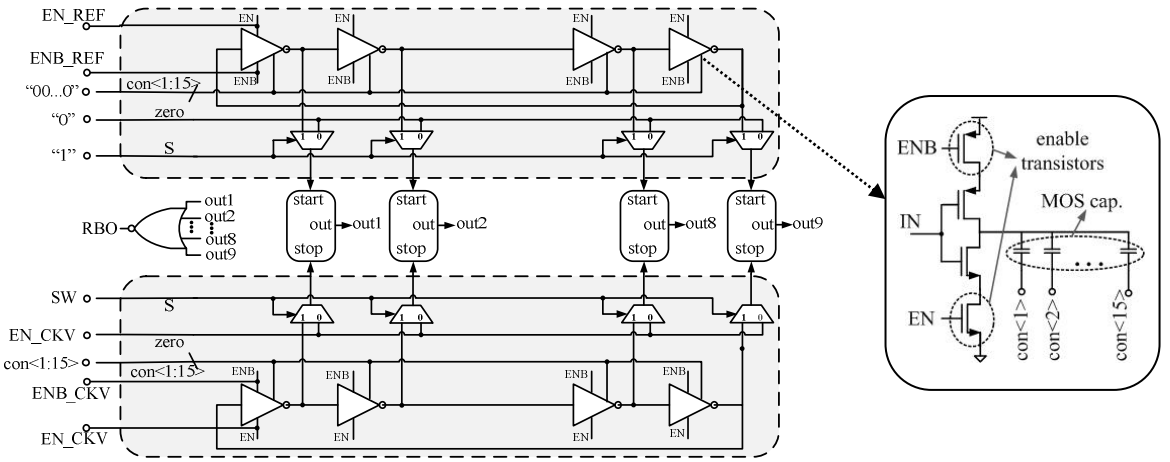


Figure.3 Vernier GRO TDC and its delay cell

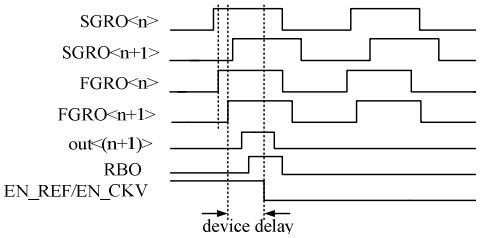


Figure.4 Gate delay in sampling and reset

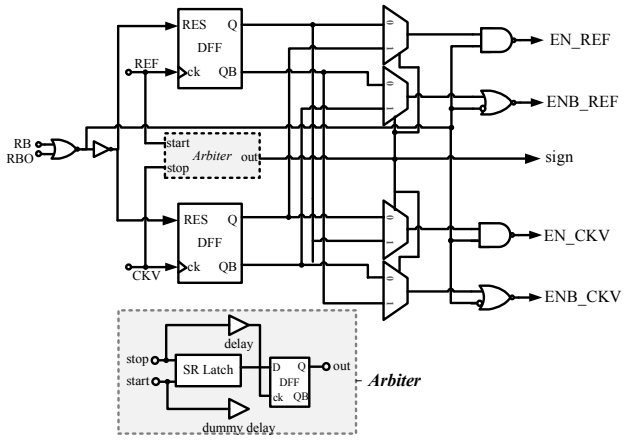


Figure.5 Phase frequency detector (PFD)

FGRO, where 1 LSB changes the delay by approx. 1.2ps in nominal conditions. Since there are two options for the *stop* signals, as mentioned in the previous Section, 9 multiplexers are used in FGRO, while corresponding dummy multiplexers with always-high selection inputs are introduced in the SGRO for symmetry.

An additional difficulty in the Vernier GRO TDC, compared to the plain GRO TDC, is that we must guarantee that the SGRO phases are leading the FGRO phases at the beginning of each measurement window. This is a challenge in presence of device delays. For example, if phase *FGRO<n+1>* (see Fig. 4) catches up with *SGRO<n+1>*, the sample result *out<n+1>* is supposed to become active immediately. In fact, some propagation time is unavoidable, as illustrated in Fig.4. The delay may accumulate to up to 200ps before *EN_REF* and *EN_CKV* respond to the reset signal *RBO* generated by the sampling block (Fig. 3). During this time, the two GROs are still active; however, no further rising edges

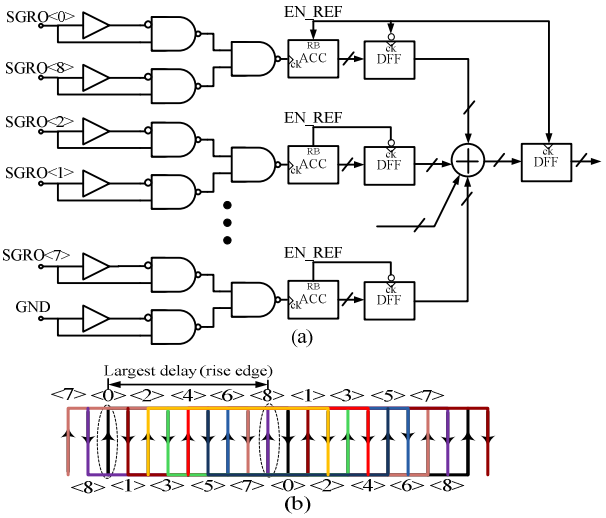


Figure.6 Multi-phase counter: (a) Schematic; (b) The largest possible delay for rise edges in the 9-stage ring

should be generated by the GRO core, otherwise an incorrect sampling operation may occur in the following measurement, where the FGRO (rather than the SGRO) may start with a leading phase. A straightforward solution is to increase the absolute delays in the cells of the GROs, so that the delay between adjacent rising edges in each GRO is larger than the time lag in the feedback path. However, a large (absolute) cell delay results in a large delay mismatch, compared to the Vernier resolution, which increases both noise and non-linearity. In this work, 400ps has been adopted for adjacent rising edges (i.e., two inverter delays). Even under this large absolute delay, good noise shaping is obtained, as shown in Section IV.

B. Phase & frequency detector

We have seen that *EN_REF* is required to always lead *EN_CKV*. However, for a normal PFD in which the output pulses corresponds to the two input clocks, this condition cannot be guaranteed, since the feedback clock frequency (and phase) are adjusted dynamically in the DPLL. Therefore, an SR latch is used as an arbiter, as shown in Fig. 5. It senses the leading edge between *REF* and *CKV*, and generates a sign signal controlling four multiplexers. When *REF* is leading, *EN_REF* corresponds to *REF*, while when *CKV* is leading, *EN_REF* corresponds to *CKV*.

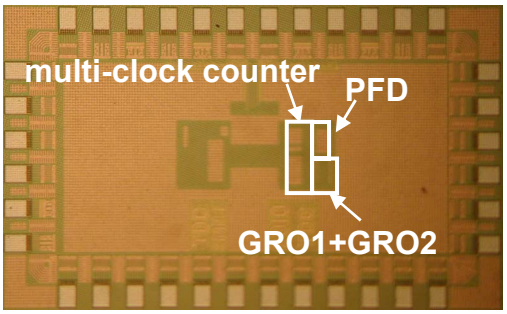
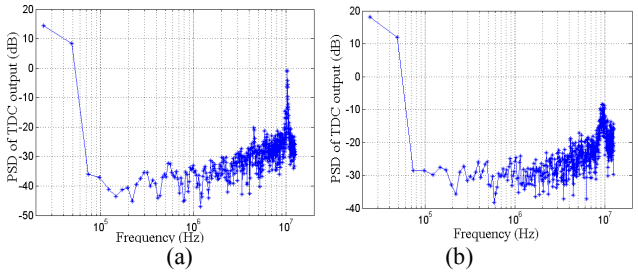


Figure.7 Die photograph



(a) (b)

Figure.8 Measured TDC output PSD with dc delay input: (a) Vernier resolution of 5.8ps; (b) Vernier resolution of 4.9ps

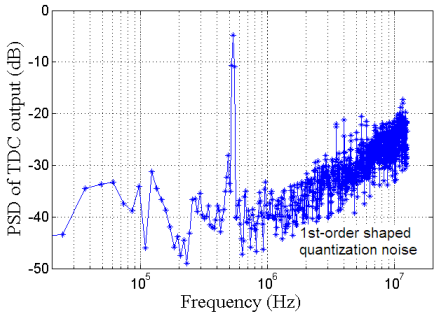


Figure.9 Measured TDC output PSD with sinusoidal delay input

C. Multi-phase counter

The digitized phase error is read out by counting the SGRO phases that have become active during the measurement interval. An obvious approach is to assign an individual accumulator for each phase (it will be remembered that each phase can become active more than once during each measurement), which however needs many adders and flip-flops. If all phases could be combined into a single signal containing all edges, only one accumulator would suffice; however, this signal would inevitable be very high frequency, bearing on the accumulator speed. Our trade-off solution is to group the phases in pairs, where the two phases in each pair are separated by the largest possible delay (Fig. 6), which eases the requirement on the accumulator speed.

IV. Measurement Results

The GRO Vernier TDC has been implemented in a 90nm standard CMOS process. Fig. 7 shows the die photo of the TDC, where the active area is 0.18mm·0.15mm.

The most straightforward way of testing the TDC is by measuring the delay between the two input signals *REF* and *CKV* having the same frequency but different phases. Since the delay between the two signals is constant, this measurement yields a dc value in the spectrum of the TDC output. Fig. 8 shows the PSD of the Hann-windowed TDC output for a dc delay of approx. 20ps and two different values of the Vernier resolution, when the input signals have a frequency of 25MHz. The two plots clearly show the effectiveness of the proposed TDC, were most of the quantization noise is pushed toward high frequencies (since the frequency of the input signals is the sampling frequency as well, the resulting Nyquist frequency in Figs. 8-9 is 12.5MHz), although with a slope slightly lower than the 20dB/decade expected from theory. Assuming that the TDC is used in a DPLL having a bandwidth of 800 kHz (i.e., operating the TDC with an oversampling ratio OSR of ~16), the in-band SNR for the PSD in Fig. 8(a) is approx. 40dB, corresponding to an in-band *rms* noise of approx. 200fs. To achieve the same SNR with the same OSR but assuming a white noise PSD, (1) yields the required Δt_{delay} of 3.2ps, which is clearly below (although not by a large amount) the Vernier delay of 5.8ps employed in the measurement. It should be noticed that the in-band noise in the PSDs of Fig. 8 is not shaped but rather white, indicating that its origin is most likely thermal (although well above the expected thermal noise of the transistors in the GROs).

Fig. 9 illustrates the measured PSD of the TDC output when the delay between *REF* and *CKV* varies sinusoidally in time with a frequency of approx. 500kHz, which is possible by using a Tektronix DTG5274 Data Timing Generator. Unfortunately, a relatively large 2.5MHz spur and its harmonics are present on the generated sinusoidal delay, making a quantitative analysis of the PSD in Fig. 9 unreliable. Nevertheless, by removing the high-frequency spurs from the PSD, it can be appreciated that the sinusoidal input results in a quantization noise shaping following the expected first-order 20dB/decade slope.

Working at a 25MHz sampling frequency, the current consumption of the Vernier GRO TDC is 3mA from 1.2V.

V. Conclusions

We have presented a Vernier TDC that makes use of two gated-ring oscillators (GRO) instead of two delay lines. The TDC, fabricated in a standard 90nm CMOS process and consuming 3mA from 1.2V, displays a first-order shaping of the quantization noise, improving the already good Vernier time resolution. The TDC is an attractive choice for use in a digital PLL.

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