A Dither-less All Digital PLL for Cellular Transmitters

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***Abstract* – Frequency synthesizer for cellular transmitters demands low phase-noise both in-band and out-of-band. The first is necessary to implement wideband modulations (e.g. WCDMA), while the second to satisfy the challenging emission mask of GSM. Moreover a low level of fractional spurs must be ensured. The paper describes the first dither-less ADPLL capable to satisfy all these requirements.**

These results are achieved exploiting a highly linear 2-dimension Vernier TDC and a very fine frequency resolution DCO. Both building blocks heavily rely on digital calibration techniques to precisely and efficiently implement two-point modulation and spur cancellation in the presence of many implementation impairments.

I. Introduction

Nowadays, in the design of a mobile transmitter, the frequency synthesis seems to be more and more a digital stuff. Differently than for the rest of the radio, in the case of phase-locked-loops (PLL) the digital revolution has been enabled by the possibility to efficiently quantize time and frequency variables.

The resolution in time and frequency demanded for a full digital approach is not less challenging than its analog counterpart. For example, in the case of the GSM the required phase noise (PN) of -165dBc/Hz @ 20MHz demands also a DCO frequency resolution below 1 kHz when a carrier of 900MHz is used [1]. At the same time, if an in-band phase noise below -105dBc/Hz is sought, a TDC time resolution close to 5ps is required for a 2GHz output carrier and a 26MHz reference clock. Both these targets are reached with the fractional-N ADPLL solution presented in this paper where a dither-less DCO able to meet GSM specs and a 2-dimensional highly linear Vernier TDC are used. In addition to this, digitally assisted locking and calibrations allow a fast phase/frequency locking and the implementation of two-point modulation.

The modulation of the signal acting directly at the level of the frequency synthesizer is becoming common for standard using phase or frequency modulations (e.g. GSM) [1]. However, thanks to the advantages given by a digital approach in terms of calibration and re-configurability, the attempt is to displace the traditional direct-up architecture through the use of polar or out-phasing techniques even when non-constant envelope standard are used (e.g. WCDMA) [2].

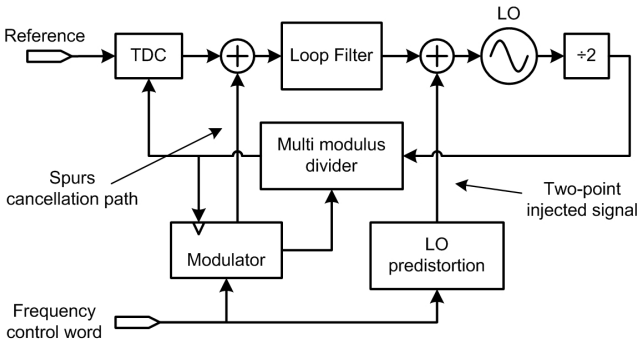

Fig. 1 Fractional-N, two-points modulation ADPLL architecture

In this paper we present an ADPLL for GSM transmitter featuring wideband direct phase modulation.

The paper is structured as follow. An overview of the proposed ADPLL architecture is given in Section II. The 2-dimension Vernier TDC and dither-less DCO are described in Section III and IV respectively. In section V, frequency-phase locking acquisition is reported, while calibration algorithms are discussed in Section VI. The paper ends with the measurements results of the ADPLL prototype reported in Section VII.

II. ADPLL Architecture Overview

Digital PLLs are usually obtained from analog ones splitting the loop into two domains, an analog one, which contains the oscillator, and a digital one, which typically includes the loop filter. The position and the characteristics of the A/D and D/A interfaces characterize the architecture of the digital PLL giving rise to several published topologies.

In this paper we present a digital PLL where the D/A interface is placed at the DCO and the A/D interface is placed at the PFD level, using a high resolution TDC to perform phase comparison [3]. The DCO has enough resolution not to require ΣΔ dithering. The analog path from the RF output to the divided edge is exactly the same as in a classic PLL. The architecture is shown in Fig. 1 and implements a type II fractional-N loop. There is a straightforward analogy with the analog PLL, the main differences being that in the digital domain an accurate ΣΔ noise cancellation can be achieved and that the loop filter can be easily reconfigured. The latter possibility [1] allows not only reconfiguration to different

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standards but also the use of gear shifting to achieve very fast locking times.

An alternative approach to implement a digital PLL consists in placing the A/D interface directly at RF, using a counter at the output of the DCO (or after a few divider stages to decrease the counting frequency). This solution eliminates the need for a multi-modulus divider chain replacing it with an RF-counter [1][4]. The operation of a multi-modulus divider however does not differ in any fundamental way from that of an edge counter, even though some differences on power consumption and synchronous behavior might apply. The comparison between the two digital PLL topologies is further carried out in [3], where the conclusion is reached that for the same TDC and DCO dynamic ranges, the two architectures are completely equivalent when a 1st order ΣΔ modulator is used in the fractional-N divider. In this work, we use a first-order ΣΔ modulator to control the fractional-N loop since it requires the smallest dynamics for the TDC. As for the D/A position, some solutions implement an analog VCO controlled through a DAC [5], thus shifting the interface at the filter output. Even though conceptually straightforward, this solution maintains the same issues of coupling and sensitivity of an analog PLL and requires a very careful DAC design in terms of noise and supply rejection.

The ADPLL presented in this paper is targeted for a GMSK transmitter using direct phase modulation. As previously mentioned, 2G transmission poses extreme challenges on the DCO phase noise profile. The insertion of a direct modulation path led to a two-point modulation scheme that ideally provides flat phase modulation response no matter which loop bandwidth (BW) is selected. Therefore, the PLL BW can be kept small to achieve low noise and spur into the adjacent channel. In principle this feature can also be leveraged to implement a polar transmitter for non-constant envelope standards (e.g. EDGE or WBCDMA).

As a final remark, it is easily understandable that the overall operation of the ADPLL must rely on multiple calibration loops. The most important one is TDC gain calibration to achieve accurate ΣΔ noise cancellation. Any gain mismatch here translates not only into phase noise degradation but also into possibly large fractional spurs, as it will be explained in Section V. Another important calibration is DCO linearization, as the dither-less DCO used in this PLL [21] exhibits a systematic non-linear characteristic that would make accurate modulation unachievable.

III. Vernier Time to Digital Converter

The A/D and D/A blocks in an ADPLL set most of its characteristics when compared to an analog PLL. The time-to-digital converter represents one of the key building blocks since its resolution limits in-band noise, while its linearity sets a lower bound for the power level of fractional spurs [4].

A. State of the Art

In terms of resolution, independently of the ADPLL architecture (with or w/o divider), the TDC must provide a time quantization that is a small a fraction of the DCO period to guarantee an acceptable in-band noise. To overcome the limit set by the minimum delay available in the technology, several architecture were proposed in literature. Linear Vernier TDCs quantize time differences exploiting the cumulative delay difference of two lines based on elements

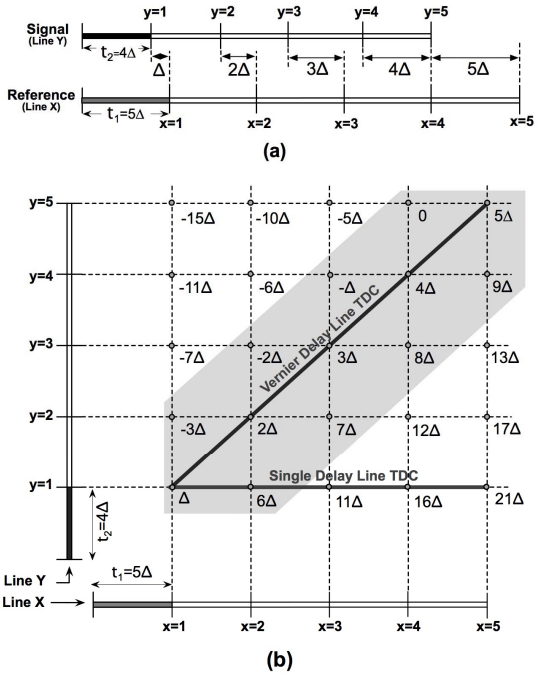

Fig. 2 (a) linear and (b) 2-dimension Vernier TDCs

whose delay is greater than the target resolution [7]-[8]. This technique can overcome technology limitations as it separates minimum stage delay from resolution. However, its full scale is limited by the number of delay elements that grows exponentially with the number of bits. Multi-path approaches [9]-[10] perform interpolation between several parallel delay lines and, as for the linear Vernier, have a full scale that is severely limited by the number of delay stages required. A larger number of bits can be obtained adopting more complex architectures directly derived from voltage-to-digital converters as the GRO based TDCs [12]-[13], that provides a shaped quantization noise like in sigma-delta ADCs, and the two-steps TDC proposed in [11] based on a time amplifier. The main drawback of these approaches is that their power efficiency decreases reducing the number of quantization levels synthesized. From this point of view when 6 bits or less are demanded, other topologies like flash TDCs becomes competitive.

B. From linear to 2-D Vernier

Linear Vernier TDCs are probably the simplest topology to implement high-resolution converters. However, the large number of delay stages required for moderate conversion ranges increases the integral non-linearity (INL) of the time-to digital conversion. In fact, in the classic linear Vernier (Fig. 4) the time quantization is realized by taking time differences only between taps located in the same position of the two delay lines (Fig. 2.a). Since a delay Δ is accumulated after each stage, a signal edge that lags a reference edge by $n\Delta$ at the input of the lines will lead it after n stages. Inserting one flip-flop for each delay line stage it is then possible to produce a digital thermometric code that represents the digitalization of the time difference [7]. This provides uniform quantization with N codes (N is the length of each delay line), each representing a time step Δ (the TDC resolution).

When all possible differences between the taps are considered, it is possible to define a plane (named *Vernier*

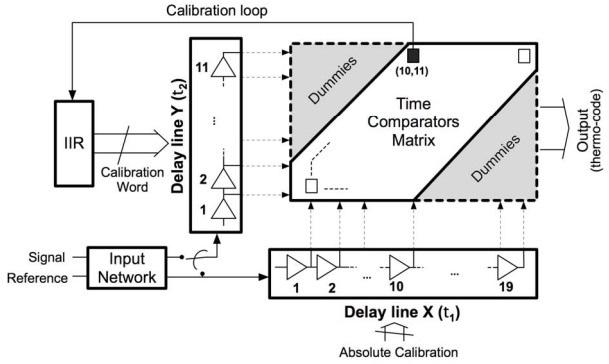

Fig. 3 TDC scheme

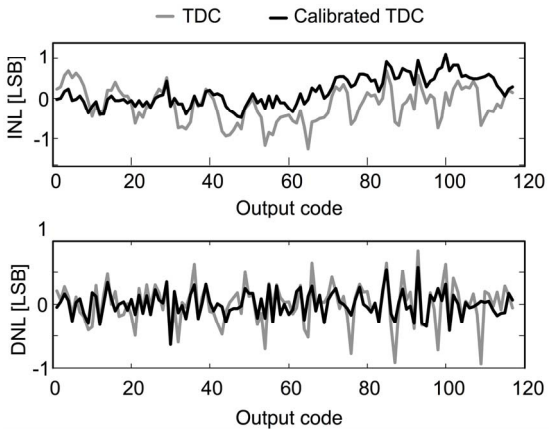

Fig. 4 TDC INL and DNL measurements

plane) as the one reported in Fig. 2.b [15]. In this way, having two lines with N elements each, N^2 quantization levels are defined. This approach can significantly decrease the number of stages of the delay lines needed to achieve a given number of quantization steps with the same resolution Δ. The reduction of the number of stages not only reduces the complexity and the power consumption of the structure, but also significantly reduces the distortion of the TDC compared to linear Vernier topology [15]. Finally, it is easily recognizable that the structure proposed can be considered as an extension of the both single delay line and linear Vernier TDCs which lie respectively on the borders and on the diagonal of the Vernier plane (Fig. 2.b).

C. Implementation

The realized 2-D Vernier TDC schematic diagram is shown in Fig. 3. The two delay lines define the *Vernier plane* that is completely covered by a matrix of SR latches used as a time comparators. Each latch produces a 1 or a 0 depending if the rising edge of the reference leads or lags the rising edge of the signal. However, while a linear Vernier produces intrinsically a thermometric code, in this case the outputs must be ordered following the position of consecutive quantization levels [16].

To allow proper operation over process and temperature change, a background DLL was used to enforce an equal length for the delay lines. This is achieved using tunable delay elements. In particular, the proper ratio between the delays τ_1 and τ_2 (in this case 11/10) is defined by a local calibration loop closed on line Y (Fig. 3). In the calibration phase, the reference feeds both the lines and the loop forces the delay accumulated after $10\tau_1$ on the line X and after $11\tau_2$ on the line Y to be equal. The tuning elements present in the line X are controlled at the PLL system level defining the TDC gain. Further details on TDC calibration will be discussed in Section VII.

Overall, the TDC is a 7-bit structure with 119 quantization levels. For line X and line Y, 19 and 11 stages are respectively used. The target resolution of Δ=5ps is obtained choosing τ_1=55ps and τ_2 =50ps, achieving a full scale of 590ps, from -45ps to 545ps. Notice that a linear Vernier approach for the same full-scale and resolution would have required two delay lines of 119 elements each (i.e. 238 stages instead of 30). This allowed containing the un-calibrated INL to below 1 LSB, as shown in Fig. 4.

IV. Digitally Controlled Oscillator

Due to the challenging out-of-band emission mask, an LC tank oscillator is a mandatory choice in terms of phase noise performances [14]. When a DCO is realized instead of a VCO an extra quantization noise is introduced. This noise has to be kept more than 10dB lower than the analog noise not to degrade the phase noise of the oscillator [14]. To achieve this for a GSM transmitter, a simple tuning of the capacitance of the LC tank would require unitary element in the order of a few atto-Farad [17], quite difficult to achieve with standard CMOS process.

A. DCO State of the art

A possible solution proposed in literature is the use of a capacitive divider network to shrink the capacitance effectively switched in parallel to the tank [18]. This approach potentially improves the DCO frequency resolution but is severely limited by parasitic capacitance. A more reliable technique proposed by Staszewski et al. consists of dithering the less significant bits of the DCO frequency control word in the same manner as in a sigma delta DAC [19]. This solution reduces considerably the equivalent DCO frequency resolution (e.g. down to 30Hz) but, since it is based on a sigma-delta modulator, the quantization noise is moved to higher frequencies where phase noise specs may be even more challenging. Due to this problem, the dithering frequency must be very high (a fraction of the LO) to satisfy the emission mask requirements far away from the carrier, thus increasing the power consumption. Furthermore, this technique requires a retiming of the digital control word in order to minimize the charged injected in the tank during the dithering. This charge in fact appears as an additional contribution to DCO phase noise [20].

B. Capacitive degenerated LC-tank DCO

In this work, we exploit the DCO topology proposed in [21], reported in Fig. 5. The fine-tuning bank is moved from the tank to the sources of the switching pair of the LC oscillator exploiting an intrinsic shrinking effect present in the capacitive degeneration of transistors M1-M2. The capacitive degeneration of the switching pair adds a reactive component to the classical negative resistance providing an additional tuning mechanism (Fig. 5). If the value of the capacitance C is much greater than the ratio between the MOS transconductance g_m and the oscillation frequency ω_{LO},

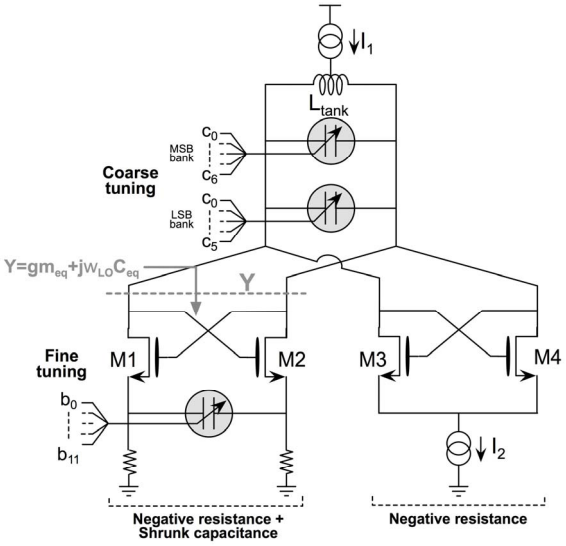

Fig. 5 ADPLL digitally controlled oscillator scheme

the real and imaginary components of the admittance Y appearing in parallel to the tank can be expressed as follows:

$$Y = -\frac{g_m}{2} - j\omega_{LO}C\left(\frac{g_m}{2\,\omega_{LO}C}\right)^2 = -\frac{g_m}{2} - j\omega_{LO}C\,Q_f^2 \qquad (1)$$

where $Q_f = g_m/(2\omega_0 C)$ is the quality factor of the impedance which models the degenerated switching pair. The equation shows that the real part of Y is still the classic negative conductance used to compensate the tank losses. On the other hand the tunable capacitance is reflected in parallel to the tank shrunk by the square of its quality factor. As an example, setting g_m = 10mS, C=4pF and f_{LO} = 3.2GHz, the shrinking factor $1/Q_f^2$ is about 350. This means that switching on a capacitance of 5fF at the sources of M1-M2 produces the same effect as switching on a capacitance of 14 aF directly in parallel to the tank, thus achieving high resolution without recurring to dithering.

The tuning characteristic of the oscillator as a function of the capacitance C (i.e. $\omega_{LO}=\omega_{LO}(C)$) can be found evaluating the resonance frequency of the circuit of Fig. 5 obtaining [21]:

$$\frac{\Delta f_{LO}}{f_{LO}} \approx -Q_f^2 \frac{\Delta C}{C_{tank}} \qquad (2)$$

To have an additional degree of freedom in the choice of the switching pair transconductance and the shrinking factor, a partial degeneration of the switching pair is used [21].

C. Implementation

The dither-less tuning scheme was applied to an existing VCO architecture obtaining the DCO scheme reported in Fig. 5. This topology differs from the original one proposed in [21], since in this case the oscillator was biased through a current generator connected between the voltage supply and the center the tap of tank inductor. Placing the current source between the power supply and the DCO improves the Power Supply Rejection (PSR) of the noise associated with the voltage regulator (1.5V) that supplies the oscillator. The current generator I_1 biases the whole DCO, with a current consumption of 18 mA with half coarse tune-capacitances at the center of the coarse tuning range. The second generator I_2 biases M3-M4, setting the current I_1-I_2 that flows in the degenerated switching pair. This solution allows to control the transconductance of the degenerated switching pair (defining Q_f and the DCO frequency resolution) and to minimize the parasitic capacitive load at the sources of M1-M2 that reduces the fine-tuning range.

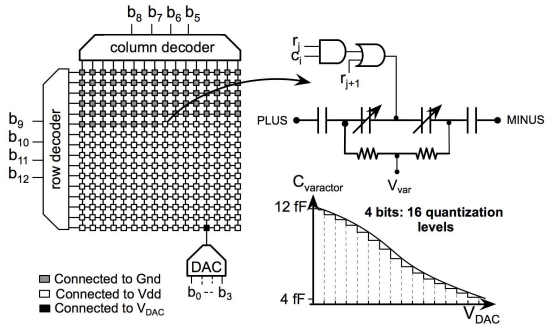

Fig. 6 Fine-frequency switching of unit capacitors

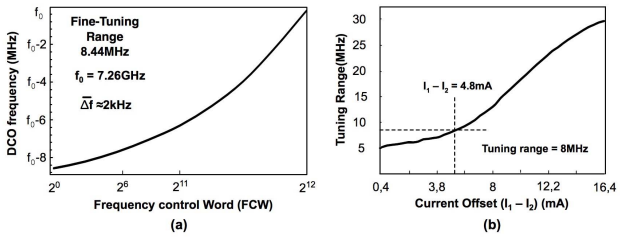

Fig. 7 (a) DCO characteristic, (b) Fine tuning-range vs. I_1-I_2

The DCO center frequency is 7.2GHz and can be varied between 5.8GHz and 8.1GHz with a tuning range of 2.3GHz (33%). The tank is realized using a differential inductor of 250pH with a simulated quality factor of 20 in the middle of the frequency characteristic. The coarse-tuning of the frequency, used to compensate the process and temperature variation and to select the channel is achieved acting on two different capacitive banks (MSB and LSB banks).

The fine-tuning bank placed between the sources of the switching pair M1 and M2 is realized as reported in Fig. 6. The 8 most significant bits (MSB) are used to control a matrix of 16x16 varactors. All elements except one are connected either to the voltage supply (V_{DD}) or to ground generating a thermometric filling of the matrix (gray and white units). The remaining varactor (black element in Fig. 6) is connected to the output of a 4-bits digital-to-analog converter (DAC) that provides 16 additional voltage levels between V_{DD} and ground. Thus a total of 12 DCO control bits are available. Since only one varactor is biased in the high-gain region of its characteristic, the sensitivity of the oscillator to noise and spurious signals coupled at the DAC output is negligible.

D. Resolution and re-configurability

The current in the degenerated switching pair (i.e. I_1-I_2) was set to have an average resolution of 2kHz with a tuning range of 8MHz (Fig. 7). This value made negligible the effect of the frequency discretization since the quantization noise laid more than 10dB below the intrinsic phase noise of the DCO.

Acting on the current I_2 allows to calibrate the DCO tuning range that can be changed between 5MHz and 30MHz as

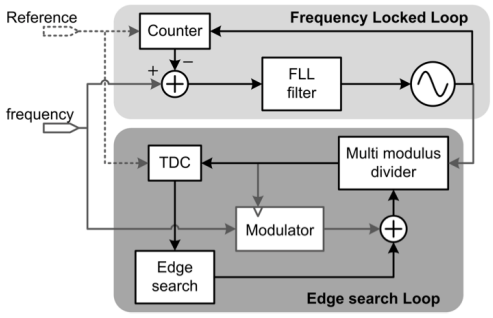

Fig. 8 FLL and Edge Search loop

reported in Fig. 7.b. The capability to change the shrinking factor allows to reuse the same oscillator for different standards that may require the same number of bits but different tuning range and frequency resolution (e.g. GSM and UMTS).

V. Frequency and Phase Locking Acquisition

In PFD based PLLs, whose linear tuning range is less than the required one usually achieve locking in 2 steps, first a coarse frequency tuning is performed re-centering the LC tank and then the real phase locking acquisition is achieved acting on the linear control node. The TDC adopted in this work does not provide the equivalent of a PFD for locking purposes. Moreover, its linear range is limited to 600ps, thus very small compared with the reference period (38ns). Therefore, a bridge is needed between coarse frequency calibration (AFCAL-Amplitude and Frequency CALibration) and PLL operation. Two calibration steps are thus added (Fig. 8), an FLL phase to compensate for the PD-only behavior of the TDC and an Edge-Search phase to compensate for the very small linear range of the TDC. Finally, linear locking is accelerated through gear shifting.

A. Frequency locked loop

The frequency locked loop is realized through the use of an RF counter that counts the number of LO periods that occurs in one reference period. The counter output is compared to the FCW and the resulting frequency error is fed to the loop filter, which consists of a simple integrator to make the FLL unconditionally stable. The ADPLL stays in FLL mode until the frequency errors falls within the linear range of acquisition.

B. Edge search loop

The narrow TDC linear range requires that the divided LO edge and the reference edge are closer than one DCO period from each other to operate linearly. If not, the TDC saturates and the loop dynamics become highly non linear and much slower. This problem can be solved keeping the system in FLL mode and controlling the multi-modulus divider to make it swallow LO edges until the TDC enters the linear region. If the divided edge is lagging (leading), and the TDC saturated high (low), the divider ratio is incremented (decremented) by 1 until the TDC enters its linear region. The multi-modulus divider does not affect the output frequency as the DCO is closed in FLL through the RF counter.

A linear search algorithm was implemented in the prototype; this solution is capable of bringing the TDC within its linear region within at most N-1 reference cycles,

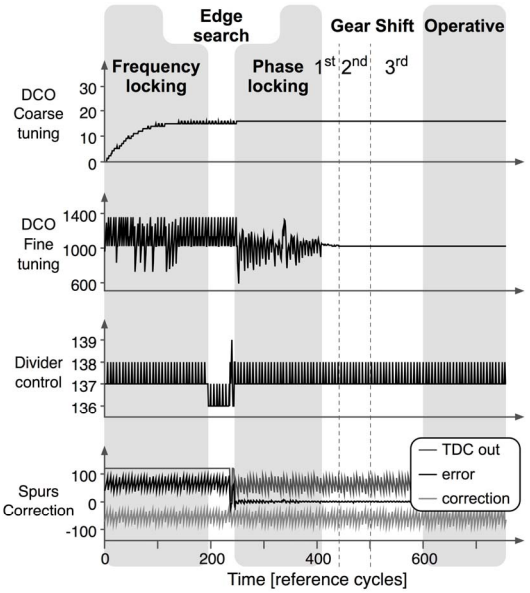

Fig. 9 Frequency -phase locking acquisition

TABLE I
ADPLL LOCKING TIME

	Time duration			average fraction of locking time	maximum end time
	Minimum	**Average**	Maximum		
AFCAL	42.5 µs	**42.6 µs**	42.7 µs	57.7%	42.7 µs
FLL	2.6 µs	**2.9 µs**	3.8 µs	4.0%	46.5 µs
Edge Search	0.2 µs	**2.4 µs**	4.7 µs	3.3%	50.5 µs
PLL WB	1.3 µs	**5.4 µs**	9.3 µs	7.4%	59.1 µs
Gear Shift	3.5 µs	**3.5 µs**	3.5 µs	4.7%	62.6 µs
DCO calibration	17 µs	**17 µs**	17 µs	23.0%	79.6 µs

depending on the initial phase offset (as shown experimentally in Table I). This can be easily improved with more sophisticated search algorithms, but in this prototype simplicity was given priority, as the overall improvement on locking was not critical.

C. Phase locking and Gear Shift

After the Edge Search phase is completed, the FLL is disabled and the PLL is activated with maximum bandwidth. A maximum of 4 gear shift steps can be programmed to achieve the final bandwidth. The first gear shift is triggered as the DCO input variation becomes smaller than a programmable threshold, thus indicating steady state operation. However, the following gear shifts are time triggered to avoid the long observation time required to detect the steady state condition. Gear shift intervals are then chosen according to their respective time constants. The overall locking process is reported in Fig. 9 and the relative locking time in Table I. Since the locking procedure is adaptive, it depends on the initial locking conditions, with a variation of 10% over the mean locking time. The greatest part of the locking time is required by the AFCAL, which is the most conservative part of the locking process and whose time duration is almost constant. On the contrary, the FLL, the Edge Search and the PLL WB sections show the highest variability due to the high sensitivity to the initial conditions.

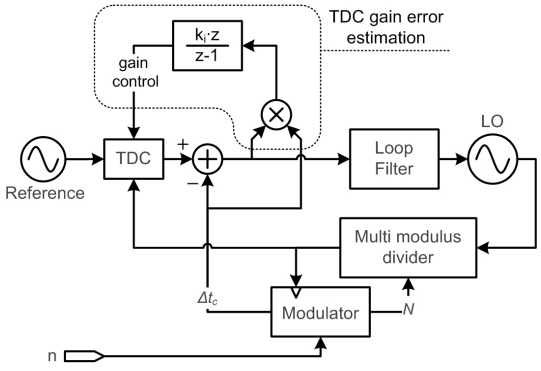

Fig. 10 TDC gain calibration loop

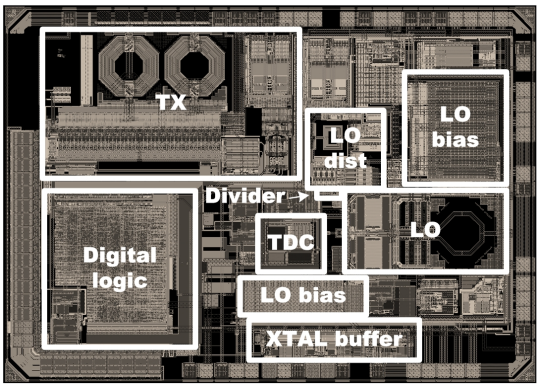

Fig. 11 ADPLL prototype

VI. Calibrations

Advanced digital features in an ADPLL rely on a seamless interface between analog and digital components. Because of analog non-idealities and process spread, it is thus fundamental to perform calibration steps to take the mismatch between analog and digital behavior below a performance threshold that is acceptable for the required ADPLL specs.

A. TDC gain calibration

The proposed ADPLL architecture is based on the cancellation of ΣΔ noise whose accuracy is completely dominated by the gain of the time-to-digital conversion [3]. Therefore we rely on an accurate background calibration scheme to track gain variations. This scheme is widely used in ADC calibrations and has been extended to TDCs as well [22]. Background operation is achieved correlating the signal after cancellation with the incoming signal, as in Fig. 10. When convergence is reached, the signals become uncorrelated. If a gain mismatch is present, the sign of the correlation can be used to feed a filter and drive gain correction. The bandwidth of the filter determines the accuracy of the correction and can be changed during operation. On the other end, the accuracy of calibration is limited by the granularity of the correction that is implementable around the TDC. As described earlier, the TDC gain is controllable in the analog domain with 10ps resolution. This is not enough and the TDC output is further corrected in the digital domain to achieve a finer resolution. The calibration machine implements the necessary logic to merge coarse analog with fine digital calibration. It is important to note that the TDC gain calibration loop has to be disabled when the fractional spur falls in band as it alters the correlation mechanism and decreases the calibration accuracy.

B. TDC linearity calibration

In a PLL implementing first-order ΣΔ residue cancellation, the TDC linearity has a deep impact on the fractional spurs that are generated in the PLL. Therefore, TDC linearity has to be trimmed to achieve INL well below 1 LSB. Because of this, we achieve linearity calibration with a foreground process that is aimed at identifying individual threshold non-discrepancies and correcting them. Threshold identification is achieved through a histogram method as from converter literature. Once the actual thresholds have been estimated, the mismatch on the X and Y delay lines are estimated as well. This is optimally achieved averaging through least squares fitting of measured thresholds with inverted delays. In more implementable terms, the delay increments on the X and Y axes are used to estimate inverter delays and compute analog correction adjustments. This process is reiterated until convergence is achieved. Then, a digital fine correction step is performed where each individual TDC output code is digitally shifted to minimize INL. This results in uneven quantization steps, but correct INL. Because of a digital limitation in the current silicon, the amount of fine correction is limited to 0.5 LSBs which nonetheless provide 5 to 10 dB improvement in the lab on the spurs level, as shown in Fig.13. Simulation results with 6 bit digital correction indicate a margin of improvement of at least 10 dB, which would take spurs below -60dBc.

C. DCO calibration

Accurate two-point modulation relies on reliable DCO gain. In the presented PLL, as shown in Section IV, the DCO fine-tuning characteristic is non-linear. During two-point modulation, the instantaneous frequency deviation is presented as a control word to the DCO assuming a linear relationship. Therefore, it is of uttermost importance calibrating not only gain, but also non-linearity so as to provide a "nominal" DCO to the modulation engine. We also remark that during modulation the DCO input signal cannot be regarded as a "small" signal since large portion of the DCO input range might be explored.

In all digital PLL, the DCO gain is generally calibrated with a digital normalization based on a background algorithm function of the phase error present in the loop [1]. The same approach could be extended to provide the predistortion of the entire DCO characteristic. However this operation is not trivial and inside the PLL loop would result to costly in term of computation. The solution proposed in this paper provides the signal predistortion only on the path that drives directly the DCO, reducing the computational complexity. This is the only component of the two-points modulation that, acting outside the loop band, is not linearized by the loop.

A polynomial equation was used for the LO predistortion. The higher is the order of the polynomial equation, the more accurate is the approximation of the nonlinear function. However, the accuracy trades off with the implementation complexity that grows with the polynomial order. A second order approximation was chosen for the LO predistortion. Polynomial coefficients are efficiently computed measuring the DCO control word variations when a given frequency is shift imposed through the sigma-delta modulator. As shown in Table I, the DCO calibration step adds 17 μs to the

TABLE II
SUMMARY RESULTS AND STATE OF THE ART

	This work	Borremans [ISSCC'10]	Hsu [ISSCC'08]	Tasca [ISSCC'11]	Zanuso [ISSCC'10]	Temporiti [JSSC '10]	Lee [JSSC'09]	Pavlovic [ISSCC'11]
Reference (MHz)	**26**	N/A	50	40	40	25	50	48
Output Carrier Frequency (GHz)	**1,8**	7,0	3,7	3,2	3,6	3,5	1,7	5,3
Tuning Range	**33%**	83%	N/A	32%	N/A	29%	N/A	34%
In-band Noise (dBc/Hz)	**-108**	-90	-108	-101	-104	-101	-114	-97
DCO phase noise (dBc/Hz)	**-160@20MHz**	-144@20MHz	-150@20MHz	-121@3MHz	-118.8@10MHz	-123@3MHz	N/A	-114@1MHz
Max PLL Bandwidth (MHz)	**3**	2	0,5	0,3	3,2	3,4	0,8	N/A
In-band spurs (dBc)	**-50**	N/A	-42	-42	-57	-58	-48	-45
RMS Jitter (fs)*	**138**	255	120	426	894	N/A	490	303
Power Dissipation (mW)	**41,6**	30	39	4,5	80	9	121	20
FoM (dB)	**-241**	-237	-242,4	-241	-222	N/A	-226,2	-237,5
Area (mm^2)	**0,7**	0,3	0,9	0,2	0,4	0,4	2,3	1,3
Process (nm)	**55**	40	130	65	65	65	90	65

* Estimated assuming optimal bandwidth for FoM [24]

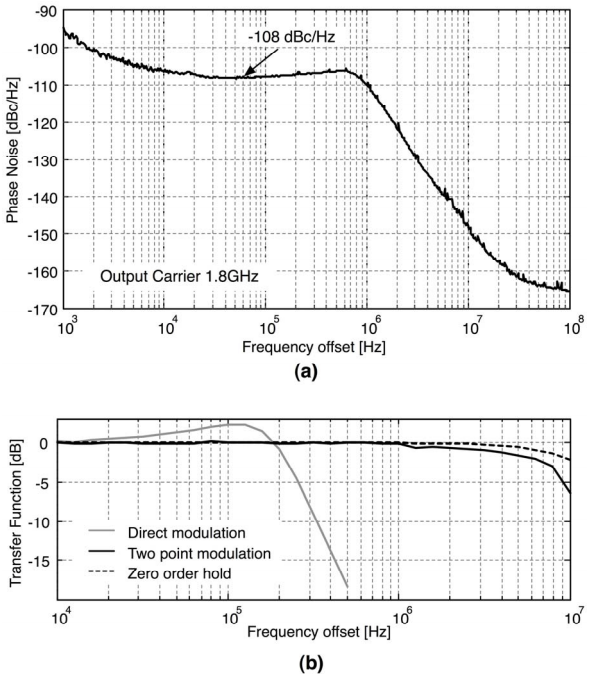

Fig. 12 (a) Phase noise and (b) PLL transfer function

calibration time, resulting in an ADPLL with an off to start time of TX of 79 µs.

VII. ADPLL PROTOTYPE

The ADPLL prototype, fabricated in 55nm low power CMOS TSMC process was inserted in a complete transmitter for GSM application (Fig. 11). The entire transmitter occupies an area of 3.5mm^2 while the total active area reserved to the ADPLL is 0.7mm^2. The output carrier frequency corresponds to 1.8GHz/900MHz after a division by 4/8 of the DCO oscillation frequency. The use of a 7.2GHz DCO core was motivated at the system level to minimize the pulling with other oscillators when integrated in a full transceiver, at the cost of increased power consumption for a given phase noise performance.

The total power consumption of the frequency synthesizer is 41.6mW, where 32.5mW are consumed the DCO, 5.4mW by the dividers, 0.75mW by the TDC and 3mW by the digital processor.

A. Phase Noise and ADPLL transfer function

Fig. 12.a shows the phase noise spectrum of the ADPLL with a carrier at 1.8 GHz and a loop bandwidth of 800 kHz. The measurement was taken with an Agilent E5052B-M1 phase noise meter. In-band phase noise is dominated by the TDC and the reference oscillator (which itself dominates for frequencies lower than 10 kHz) while the DCO has a negligible impact. The measured -108dBc/Hz in-band phase noise is only 2dB away from the theoretical quantization noise floor for the given TDC resolution of 5ps and a reference of 26MHz [6].

In Fig. 12.b the ADPLL transfer functions with and without the two-point modulation are reported. When the two-point is activated, the modulation bandwidth is limited by the zero order hold transfer function due to the reference clock of 26MHz. This curve represents the ultimate limit to the two-point modulation bandwidth. The two-point modulation transfer function is remarkably flat also in the surroundings of the ADPLL bandwidth, where an inaccurate signal injection at the input of the DCO could produce a discontinuity in the signal transfer function.

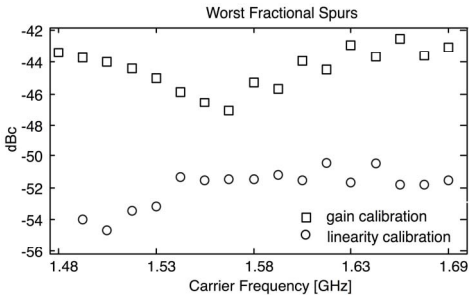

Fig. 13 Fractional spurs

B. Spurs

Fractional spurs are an issue for all frequency synthesizers. The choice of a first order Sigma Delta modulator (without any dithering) that was taken to minimize the required TDC full-scale has the fractional spurs augment as its major drawback. A spurs cancellation approach was used that rely on the TDC gain calibration. Since the fractional spurs are injected in the system at the TDC input they are processed by the low pass system transfer function. The fractional spurs were measured in band for different values of the carrier frequency. The measurement results are depicted in Fig.13 The TDC gain calibration algorithm resulted in a -42dBc worst case spurs level while a worst case spur level of -50dBc was obtained after linearity calibration.

C. State of the art comparison

The main characteristics of the proposed ADPLL are summarized in Table II. The out-of-band phase noise must be normalized to the output carrier frequency while the in-band noise also to the reference frequency [25].

Different implementation are compared using the following figure of merit (FoM) [24]:

$$FOM = 10Log\left(\frac{\sigma_T^2}{1s}\cdot\frac{P_{PLL}}{1mW}\right) \qquad (3)$$

where σ_T is the RMS jitter and P_{PLL} the total power consumption of the PLL. Expression (3) assumes to use for the PLL the optimum bandwidth for Jitter minimization [24] i.e. the one that gives the same jitter contribution for the DCO and the rest of the PLL. For this reason, the different PLL architectures were compared evaluating the jitter for the optimal bandwidth. Furthermore the optimal bandwidth was extrapolated assuming only white noise for the oscillator. Equation (3) also assumes that the oscillator consumes the same power as the rest of the PLL. Under both of these conditions (i.e. optimum bandwidth and optimum power consumption partition between the PLL building blocks) the FoM reaches its absolute minimum value [24]. For the PLL reported here the DCO consumes about 80% of the total power consumption to satisfy the stringent GSM out-of-band emission mask. This situation slightly penalizes the proposed solution with the respect to the rest of Table II.

CONCLUSIONS

In this paper a high performance ADPLL for cellular transmitters has been presented. It combines noise performances of the best analog PLLs with the flexibility of digital circuits, allowing wideband two-point modulation and fast locking. Measurements and FoM classification confirm the soundness of the proposed solution.

ACKNOWLEDGMENTS

This research has been supported by the Italian National Program FIRB, contract n° RBAP06L4S5. The authors want to thank to Marvell for technology access, Luca Romanò, Antonio Milani, Enrico Sacchi, Alessandro Venca and Francesco Rezzi for fruitful discussions.

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