A 2G/3G Cellular Analog Baseband Based on a Filtering ADC

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***Abstract*—A current-driven low-pass filter embedded in a sigma-delta analog-to-digital converter is presented. The implementation of a class-B feedback digital-to-analog converter, together with in-band noise reduction and passive filtering, gives the possibility to handle challenging wireless communication scenarios with low power consumption. The architecture is a suitable candidate to implement the entire baseband analog section of a Global System for Mobile Communications–Universal Mobile Telecommunications System (GSM–UMTS) reconfigurable receiver.**

***Index Terms*—Baseband (BB), dynamic range (DR), low-pass filters, out-of-band blockers, receivers, software-defined radio (SDR).**

I. Introduction

THE software-defined radio (SDR) ultimate goal is to substitute all the analog blocks with a more flexible and lower cost digital processor [1]. For a wireless receiver, this corresponds to placing the analog-to-digital converter (ADC) at the antenna. Such a solution is, however, either not feasible or extremely power hungry. A first step toward the implementation of an SDR moves the ADC just after the down-conversion mixer (Fig. 1). Still, removing all the blocks located between the mixer and the ADC remains very challenging since the filtering action of the analog baseband (BB) prevents the saturation of the ADC in the presence of large interferers. Moreover, the need to detect a very small signal when the receiver is operating at the sensitivity level sets challenging BB noise requirements.

In this brief, a low-pass continuous-time (CT) $\Sigma\Delta$ ADC that combines interferer filtering, variable-gain amplifier (VGA), and signal digitization is presented (Fig. 1). Such a filtering ADC is intended to replace the entire analog BB of a 2G–3G receiver. The ADC is based on the Rauch biquad filter in which the feedback resistance is substituted by the cascade of a quantizer and a digital-to-analog converter (DAC) (Fig. 2). The DAC closes the loop around the forward integrator injecting a current at the input of the filter, which is assumed to be operated in the current domain. The input current represents the down-converted received (RX) signal, while R_S models the finite output resistance of the mixer [2].

The topology is an evolution of the one used in the Digital Video Broadcasting—Terrestrial–Advanced Television Systems Committee (DVBT–ATSC) receiver presented by the same authors [3] and extends its range of application to the more challenging Global System for Mobile Communications–Universal Mobile Telecommunications System (GSM–UMTS) environment. In the latter case, in fact, a dynamic range (DR) much larger than that for the case of a digital terrestrial television (DTT) tuner is required.

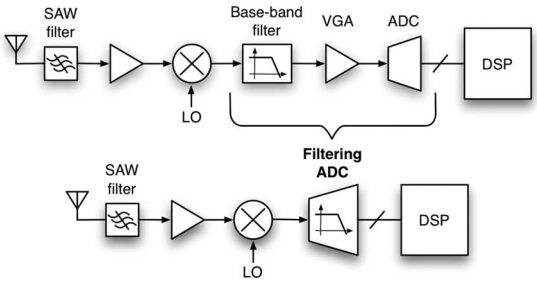

Fig. 1. First step toward a more flexible receiver.

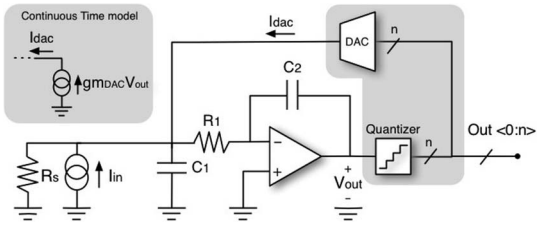

Fig. 2. Proposed low-pass-filtering ADC (single ended for simplicity).

The GSM–UMTS BB specifications can be satisfied combining the benefits of the filtering ADC with three key novel elements. They are briefly introduced here but will be explained in greater detail in the following part of this brief, pointing out the main differences with the previous implementation [3]. First, when a passive mixer is used [4], [5], the use of a pure integrator in the forward path (Fig. 2) (as opposed to a damped one) reduces BB sensitivity to the mixer output impedance. Second, in order to increase the receiver DR, a class-B DAC architecture is proposed. Third, an automatic gain control (AGC) is embedded in the filtering ADC to increase the robustness of the receiver in the presence of blockers.

This brief is organized as follows. In Section II, the filtering ADC transfer function analysis is reported, with particular focus on the input impedance result. In Section III, the noise analysis is developed, and in Section IV, the class-B DAC concept is explained. The AGC implementation is shown in Section V. Finally, in Section VI, the simulated results for GSM and UMTS application are reported.

II. Filtering ADC Response

In any wireless receiver, the power of the blockers increases with their distance in frequency from the desired channel [6]. This characteristic makes the BB filter crucial in determining the DR of the ADC.

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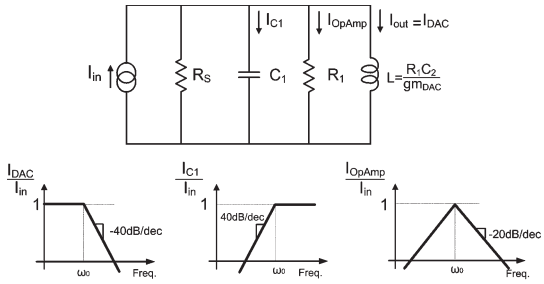

Fig. 3. Current biquad Rauch filter as an LRC shunt network.

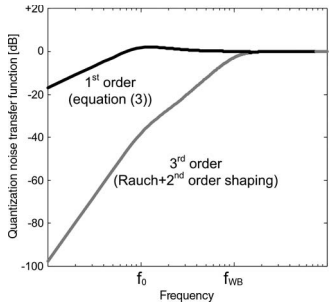

Fig. 4. QNTF. (Black) Rauch ADC and (gray) Rauch + second-order shaping.

A. CT Model and Impact of the Embedded Filter on the DR

The signal transfer function (STF) $V_{\rm out}/I_{\rm in}$ of the circuit shown in Fig. 2 has been studied in the CT domain, modeling the cascade of the quantizer and the DAC with a transconductance equal to $gm_{\rm DAC}$. The value of this transconductance is the ratio between the maximum current that the DAC has to handle and the maximum allowed voltage swing at the input of the quantizer. Although this is only an approximated model, it has been verified that, in the band of interest, the more correct discrete-time model [7], [8] provides the same results.

As expected, the structure realizes a second-order low-pass filter whose transfer function is

$$H(s) = \frac{G}{1 + s/(\omega_0 Q) + s^2/\omega_0^2} \tag{1}$$

where $H(s) = V_{\rm out}/I_{\rm in}$, G is the transimpedance gain and is equal to $1/gm_{\rm DAC}$, and ω_0 and Q are given as follows:

$$\omega_0 = \sqrt{\frac{gm_{\rm DAC}}{R_1 C_1 C_2}} \quad Q = \sqrt{gm_{\rm DAC} R_1}\sqrt{\frac{C_1}{C_2}}\frac{R_S}{(R_S + R_1)}. \tag{2}$$

The second-order filtering described by (1) is embedded in the ADC. The BB DR improvement, compared with that obtained using a classical wideband ADC, is proportional to the attenuation provided by such a filter and thus is frequency dependent. It can be seen that the use of a pure integrator in the forward path makes both the transimpedance gain G and ω_0 independent from the driving impedance R_S. This property becomes extremely important when the filter bandwidth is very close to the RX channel edge and is not valid for the filtering ADC used in the DTT tuner [3].

B. RLC Model and Input Impedance

State-of-the-art receivers [4], [5] use passive mixers to reduce power consumption and improve linearity. The main drawback of this strategy is that the passive mixer does not isolate BB and RF, displaying a driving impedance R_S that depends on RF parasites and whose finite value must be taken into account. To set the filter cutoff frequency very close to the channel edge requires BB architectures with low dependence of the STF on R_S.

The filter embedded in the ADC corresponds to an LRC shunt network in which the output signal is the current flowing into the inductance (Fig. 3). The equivalent inductance is equal to $R_1 C_2/gm_{\rm DAC}$ and is realized by the feedback DAC. The use of a pure integrator gives an infinite quality factor for the inductance as opposed to the solution presented in [3] where a damped integrator was used.

In Fig. 3, the currents absorbed by C_1, by the DAC, and by the operational amplifier (OA) are plotted versus frequency for a unitary input current. As expected, the current of the DAC has a second-order low-pass shape. On the other hand, the OA draws all the signal current at the resonance frequency, while beyond that, it sees a first-order low-pass filtering. While the role of C_1 is not modified compared with that in [3], since it still absorbs the majority of the out-of-band input current, thereby limiting the swing at the mixer output even for large out-of-band blockers, the in-band behavior of the filtering ADC is heavily modified.

Based on the RLC model, the input impedance can be easily calculated. At low frequency (in band), the input impedance is dominated by the inductance, thus providing a small load for the mixer. At ω_0, it is equal to R_1 while C_1 sets its out-of-band value. On the other hand, in the DTT tuner, a finite dc input impedance was synthesized.

Compared with the DVBT–ATSC tuner [3], the sensitivity to R_S is reduced. For the ADC used in the tuner, R_S affects all the parameters of the biquad filter, i.e., G, Q, and ω_0. For the solution presented here, instead, R_S affects only the Q of the poles (from (2), R_1 parallel R_S decides the Q), i.e., it changes the STF only close to ω_0. This characteristic is particularly important for a complex (I and Q) receiver based on passive mixers where asymmetry around the carrier frequency is observed since RF and BB are not isolated from each other.

III. Filtering ADC Noise

While the amount of filtering sets the maximum out-of-band signal that can be handled by the ADC, the minimum detectable signal is defined by the noise floor, i.e., the sum of quantization and analog noise. In this respect, the larger G of this topology compared to that in [3] improves the noise figure (NF).

A. Quantization Noise

The quantization noise transfer function (QNTF) for the structure in Fig. 2 has been evaluated with a linear model [9], leading to the following result:

$$QNTF(s) = \frac{sC_2(1 + sC_1R_1)}{s^2C_1C_2R_1 + sC_2 + gm_{\rm DAC}}. \tag{3}$$

As shown in the plot in Fig. 4, which refers to (3), the presence of the zero at dc leads to a first-order noise shaping that peaks at ω_0 where QNTF is equal to $(1 + Q^2)^{0.5}$. A first-order noise shaping is not enough to reach the DR required in a wireless receiver. To increase the order of the quantization noise shaping, without compromising the frequency selectivity provided by the filter, the quantizer is replaced by a wideband multifeedback second-order $\Sigma\Delta$ modulator. The resulting topology is the third-order $\Sigma\Delta$ filtering ADC shown in Fig. 5. The plot of the new QNTF is also shown in Fig. 4. As expected, in band, the QNTF has a 60-dB/dec slope for the new structure as opposed to a 20-dB/dec one for the old one. Notice that the

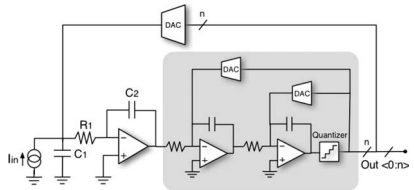

Fig. 5. Third-order noise shaping architecture.

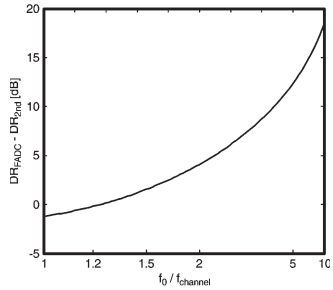

Fig. 6. Integrated quantization noise of the filtering ADC compared to a second-order wideband sigma-delta ADC (in terms of DR difference).

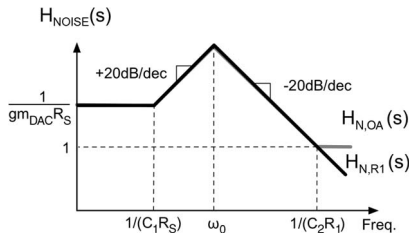

Fig. 7. ADC noise transfer functions.

stability issues for the filtering $\Sigma\Delta$ ADC are essentially the same as that for the second-order modulator (the gray position in Fig. 5) since its bandwidth is much wider than that of the filtering stage.

The filtering $\Delta\Sigma$ ADC has an advantage in terms of quantization noise compared to the cascade of an equivalent filter plus an ADC. The loop gain used to synthesize the complex poles, in fact, contributes also to noise shaping. The amount of additional noise shaping has been quantified computing the integrated quantization noise in the signal bandwidth, versus filtering cutoff frequency, for a given clock frequency. The results of such a calculation are shown in Fig. 6. As expected, the further away the filter bandwidth is placed from the channel bandwidth, the more significant the extra noise shaping is. The slight degradation in the integrated noise when the filter bandwidth is made to coincide with the channel bandwidth is due to the chosen filter Q.

B. Analog Noise

The main analog noise contributors of the structure (Fig. 2) are the resistor R_1, the OA, and the feedback DAC. The latter will be analyzed in the next section.

For the resistor R_1 and the OA, the transfer functions from their voltage noise sources to the quantizer input have been evaluated using the CT model in the previous section

$$H_{\mathrm{noise},R_1}(s)=H(s)\cdot\left(\frac{1}{R_S}+sC_1\right) \tag{4}$$

$$H_{\mathrm{noise,OA}}(s)=H(s)\cdot\left(\frac{1}{R_S}+sC_1+sC_2\left(1+\frac{R_1}{R_S}\right)+s^2C_1C_2R_1\right). \tag{5}$$

These two output noise spectra (plotted in Fig. 7) show a high-pass shape due to the presence of an in-band zero in both transfer functions. The high-pass shaping of the analog noise is an intrinsic mechanism of current-driven filters [10]. This effect is less evident when the driving impedance R_S is decreased. Under the assumption of $R_S \gg 1/(C_1\omega_0)$ and $C_1 \gg C_2$, the integrated in-band noise at the input of the quantizer is given by

$$\overline{V_{\mathrm{ON}}^2}=4kT\frac{1}{gm_{\mathrm{DAC}}^2}\left[gm_{\mathrm{ED}}f_B+\frac{2\pi}{3}C_1\left(\frac{Q}{f_0}+2\pi C_1R_{\mathrm{EQ}}\right)f_B^3\right] \tag{6}$$

where k is the Boltzmann constant, T is the absolute temperature, R_{EQ} is the input equivalent noise resistance of the OA, gm_{ED} is the equivalent noise transconductance of the DAC, f_0 is the filter cutoff frequency, and f_B is the channel bandwidth.

The proposed undamped solution has a smaller analog noise compared to the damped one [3] because R_1 is smaller with damping than without. There is a tradeoff between the value of the input impedance and the frequency selectivity on the one side and the integrated noise on the other side that is the same as that in [3].

IV. Class-B DAC

Because of their high-pass-shaped noise transfer functions, R_1 and OA can be made to contribute a similar amount of or even less noise than the DAC. It becomes therefore mandatory to minimize the DAC noise. In a traditional approach (class A), the DAC noise is proportional to its full-scale current, which is determined by the level of blockers to be handled. This is true even when no blockers are present (e.g., sensitivity test). The proposed class-B DAC is able to break the dependence of the injected noise on the full-scale current in the latter case.

In the classical Rauch biquad filter, the feedback resistor R injects at the input of the filter a current noise spectral density, independent of the input signal amplitude, given by

$$i_{\mathrm{noise},R}^2 = 4kT/R. \tag{7}$$

When the resistor is replaced with a DAC, the feedback path injects rectangular pulses of current that are controlled by the output of the quantizer. For a current-steering architecture, the noise of each cell of the DAC is given by

$$i_{\mathrm{noise,cell}}^2 = 4kT/R\left(2\gamma\frac{V_{\mathrm{LSB}}}{V_{\mathrm{OV}}}\right) \tag{8}$$

where V_{OV} is the overdrive voltage of the MOS transistor implementing the cell current generator and V_{LSB} is the voltage at the input of the quantizer that corresponds to one LSB. Furthermore, in (8), the relationship $gm_{\mathrm{DAC}} = 1/R$ has been used since the same transfer function is assumed for the two cases. For a 4-bit DAC and typical values of V_{OV}, $i_{\mathrm{noise},R}^2/i_{\mathrm{noise,cell}}^2$ varies from 4 to 10 dB. This means that, at a given time, the noise injected by the DAC can be larger or smaller than that of the corresponding R depending on the number of DAC cells contributing noise. The key points are if the DAC noise depends or not on the output code and if it is possible to minimize it in the absence of large interferers, i.e., when the required sensitivity is maximum. In the following, two different DAC topologies are compared [Figs. 8(a) and 9(a)] both based on a six-level thermometric architecture (just for simplicity). In both cases, there are seven possible output levels ranging from $+I$ to $-I$ with a minimum step of $I/3$.

The first DAC is operated in class A [11] and is shown in Fig. 8(a) for the fully differential case. Each output signal is the difference between a fixed current supplied from the positive rail (equal to full scale) and that of six current sources (injected

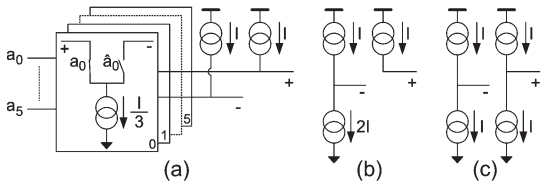

Fig. 8. (a) Classical class-A DAC architecture. (b) Input code $a_0, \ldots, a_5 = 111111$; $I_{\rm OUT} = +I$. (c) Input code $a_0, \ldots, a_5 = 000111$; $I_{\rm OUT} = 0$.

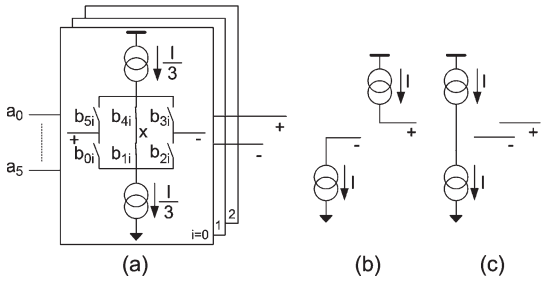

Fig. 9. (a) Class-B DAC architecture. (b) Input code $a_0, \ldots, a_5 = 111111$; $I_{\rm OUT} = +I$. (c) Input code $a_0, \ldots, a_5 = 000111$; $I_{\rm OUT} = 0$.

into the negative rail) that can be switched to either one of the output nodes. The elementary DAC cell is a differential pair connected to the positive or to the negative output driven by one bit of the code.

Fig. 8(b) shows how the positive full-scale output current $(+I, -I)$ is obtained for the DAC code $a_0, \ldots, a_5 = 111111$, while Fig. 8(c) shows how the zero output current is obtained for the code $a_0, \ldots, a_5 = 000111$. The latter case can be representative of the sensitivity condition. At sensitivity, in fact, a very small signal is present at the input of the quantizer (with its added noise), and statistically, for a high percentage of time, only the middle code drives the DAC input. In the class-A implementation, however, independent of the DAC code, the noise of all the current generators is injected at the input node.

The second topology [Fig. 9(a)] is a push–pull structure [12] that injects or absorbs current without any fixed bias connected directly to the output. The proposed class-B concept uses three-way [13] current-switching cells at the cost of a higher number of switches and more complexity in the driving logic. The controls $b_0 - b_5$ of each elementary cell are obtained from $a_0 - a_5$ through a simple digital logic. The elementary cell uses four switches to send the current taken from the positive rail either to the positive or to the negative output and vice versa for the current taken from the negative rail. In addition, two extra switches (connected to a fixed node X) are added, making it possible to switch off the cell while maintaining the current generators always in the ON state. Not only the cells pull and push the current but also they can be put in a rest condition. For the $I/3$ signal level, only one cell is driven in ON state. The $2I/3$ signal level is realized with two cells in the ON state, while the full-scale current requires all the three cells in ON state. The positive full-scale $(+I, -I)$ and the zero current levels are shown in Fig. 9(b) and (c), respectively. In the latter case, all cells are switched off from the output nodes, therefore contributing zero noise.

With large interferers, all the DAC cells are in the ON state and contribute to the overall noise. In this situation, however, also, the noise requirements are less critical. When the input signal decreases, less feedback current is required, and less cells are turned on. In the limit of a very small input signal (sensitivity test), almost zero noise is injected by the DAC. The current noise spectral density injected at the input of the $\Sigma\Delta$ ADC for a class-B DAC at each clock cycle depends on the value of the feedback signal according to the following expression:

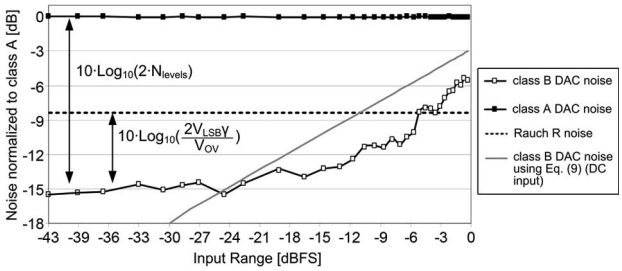

Fig. 10. Simulated (MATLAB) and calculated DAC noise into a CT sigma-delta converter and R noise into a Rauch biquad filter.

$$i^2_{\rm noise,BDAC} = 4kTgm_{\rm DAC}\left(2\gamma\frac{V_{\rm QUANT}}{V_{\rm OV}}\right) \qquad (9)$$

where $V_{\rm QUANT}$ is the voltage at the input of the quantizer. Notice that, for a dc signal, (9) gives also the rms $\Sigma\Delta$ input noise. On the other hand, the noise at the $\Sigma\Delta$ output for a sinusoidal input has been obtained via simulation for both a class-B and a class-A DAC (13 levels) and is plotted in Fig. 10 versus input amplitude. The noise obtained using (9) (dc signal) is also shown in the figure for comparison. As expected, the class-B DAC has always a noise advantage compared to a class-A one, but the difference varies from about 14.5 to about 6 dB going from small- to full-scale inputs. The flat portion of the noise curve for small input in the class-B case is due to the fact that, for simplicity, it has been assumed that the LSB cell is never switched off. For inputs larger than a few LSBs, (9) overestimates the actual noise of the class-B DAC by an amount that represents the peak-to-average ratio (PAR) of the used signal. It follows that, for signals with a very high PAR, like those used in high-spectral-efficiency modulators, the advantage is even bigger. Fig. 10 also shows the noise of the feedback resistor for the equivalent Rauch filter assuming a 6.5-dB ratio for $i^2_{\rm noise,}R/i^2_{\rm noise,cell}$. The filtering ADC is better than the Rauch filter in terms of noise for small signal where noise reduction is critical. Furthermore, for a higher PAR signal, the advantage would remain up to a larger amplitude.

V. VGA Implementation

2G–3G standards are so critical that class-B DAC DR boosting, R_1 noise reduction, and embedded filtering are still not enough to satisfy all specifications. Taking into consideration the required receiver robustness to fading and the signal PAR, more decibels of DR are required. The BB can be relaxed implementing a VGA in the receiver chain. The filtering ADC is able to embed some VGA action too.

The variable gain is realized by modifying the feedback capacitance C_2 and the full-scale current level $(gm_{\rm DAC})$ and switching the resistance R_X from virtual ground to ground, as shown in Fig. 11. Gain reduction necessarily worsens the noise performance. However, the signal itself is significantly greater than the one to be detected at sensitivity when large blockers are present, ensuring a sufficient SNR at the output.

VI. Simulation Results

GSM and UMTS standards are suitable to show the potentiality of the proposed structure. The simulated direct conversion (I and Q) receiver chain consists of the cascade of a low-noise transconductance (LNT), two 25%-duty-cycle passive mixers,

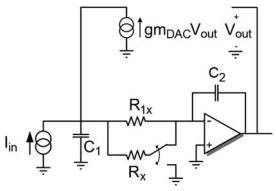

Fig. 11. Variable-gain Rauch ADC architecture.

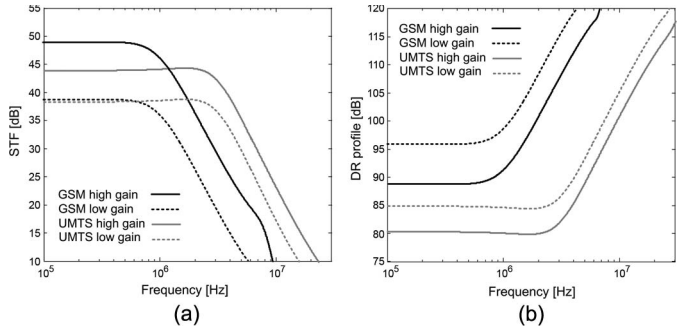

Fig. 12. STF and DR profiles: (Black) GSM and (gray) UMTS.

and two BB Rauch ADCs. The simulated LNT has a transconductance gain of 50 mS and a 400-fF–1-kΩ single-ended output impedance. NMOS mixers are driven with 900-mV square-wave swings. The LNT-plus-mixer NF is assumed to be 1.5 dB which is a reasonable value achievable at low power consumption with state-of-the-art technology. PSS, PAC, and PNOISE Spectre and MATLAB simulations have been performed.

A. GSM

The sensitivity target for GSM is -110 dBm (SNR of 5 dB), and 4 dB of board attenuation (surface acoustic wave (SAW) plus antenna switch) is assumed. To satisfy the corresponding 2-dB NF requirements, the ADC noise floor has to be -128.5 dBm. GSM standard presents interferers with a power of $+76$ dBc at a distance of 3 MHz from the desired signal (-99 dBm). Moreover, the reference interferer test considers a single tone with a power of $+41$ dBc at a distance of 400 kHz from a signal of -82 dBm. To meet these specifications, 101.5- and 83.5-dB DRs are respectively required at the ADC in the absence of any analog filtering or VGA. Choosing $f_0 = 1.4$ MHz for the filtering ADC, the 3-MHz interferer is reduced by filtering, and the needed (in-band-referred) worst case DR becomes 88.3 dB. Providing some practical numbers for the 3-MHz test, e.g., -23 dBm at the antenna, due to SAW, LNT gain and mixer attenuation consist of 320-μA input current coming from the mixer. The DAC current is 70 μA, while the OA current is 190 μA.

Noise simulation shows that 2-dB NF and 89-dB in-band DR can be obtained with a DAC full-scale current of 80 μA and using a 210-pF total capacitance. The BB noise is contributed as follows: R_1 (65%), OA (25%), DACs (6%), and others (4%). The estimated converter power consumption is 5 mA. STF and DR (defined as the ratio between the power of the maximum signal that can be handled by the ADC and the integrated in-band noise) versus frequency are shown in Fig. 12(a) and (b), respectively, for GSM and UMTS and for low- and high-gain modes. The in-band gain (in high-gain mode) is 48.5 dB. This is obtained from the 50-mS transconductance of the LNA, the -7-dB mixer conversion gain, and the 12-kΩ equivalent transimpedance of the BB. In low-gain mode, the gain is reduced by 10 dB, acting on BB only, and the NF of the complete receiver becomes 4 dB.

B. UMTS

The UMTS sensitivity is -107 dBm (SNR of -6 dB and duplexer loss of 4.3 dB). The ADC noise floor has to be -113.7 dBm to satisfy the corresponding 2.2-dB NF. The UMTS adjacent channel can reach a power of $+41$ dBc at a distance of 5 MHz from the desired signal, whose power is equal to -66 dBm. An ADC DR of 84.4 dB is required. Choosing $f_0 = 3.2$ MHz for the ADC, the needed in-band-referred worst case DR is 76.4 dB. Providing some practical numbers for the 5-MHz test, obtaining 250-μA input current coming from the mixer, 95 μA is the DAC current while 210 μA is the OA current.

Noise simulations show that 2.2-dB NF and 80.2-dB in-band DR can be obtained with a DAC full-scale current of 140 μA. The estimated capacitance and power consumption are the same as those of GSM. The BB noise is contributed as follows: R_1 (35%), OA (35%), quantization (18%), DACs (6%), and others (6%). The in-band gain (in high-gain mode) is 44 dB. This is obtained from the 50-mS transconductance of the LNA, the -7-dB mixer conversion gain, and the 7.15-kΩ equivalent transimpedance of the BB. In low-gain mode, the gain is reduced by 6 dB, acting on BB only, and the NF of the receiver becomes 3.6 dB.

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