20.4 A 36mW/9mW Power-Scalable DCO in 55nm CMOS for GSM/WCDMA Frequency Synthesizers

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The RF front-ends of modern smart phones are becoming more complicated as newer standards are introduced (e.g. LTE). Reconfigurability can be used to reduce their size, provided that power consumption is not adversely affected. For 2G/3G transceivers, local oscillator (LO) generation requires significant area and power. Reconfigurable voltage-controlled oscillators (VCOs) are generally used to maximize the achievable tuning range to reduce their number in the presence of many supported bands. However, no VCO capable to support both WCDMA and GSM has been reported that is also competitive with the power consumption achieved using two separate oscillators. In fact, the very demanding GSM phase-noise specs require a current up to four times higher (depending on the duplexer selectivity) than that used in the WCDMA case. In the design of an LC-tank harmonic oscillator, phase noise normalized to power consumption (i.e. the figure-of-merit, FOM), reaches an optimum at the maximum oscillation amplitude compatible with the supply voltage V_{dd} [1]. This condition impairs the power re-configurability of a VCO, since there is only one value of bias current yielding the highest FOM, once tank and V_{dd} are chosen. On the other hand, making the tank reconfigurable invariably results in a degradation of its Q, i.e. a reduced FOM.

In this paper, a VCO whose power consumption can be reconfigured while maintaining an almost constant FOM is presented. The idea is to keep the same (optimized) tank while switching the VCO topology from n-only to p-n (Fig. 20.4.1). As theoretically derived in [1], for the same tank and the same V_{dd}, n-only and p-n VCOs have the same maximum FOM, which, however, is reached using 4 times more current in the n-only VCO. In this case, the oscillation amplitude is twice as large, and the phase noise is 6dB lower. This can be intuitively understood observing that, on the one hand, the FOM increases with the LO swing, and this can be twice as large for an n-only VCO, compared to a p-n VCO; on the other hand, a p-n VCO has a current efficiency twice that of an n-only VCO (Fig. 20.4.1). These observations indicate a clear path to power reconfiguration, i.e. use an n-only VCO for the lowest phase-noise case, and switch to a p-n VCO when a higher phase noise can be accepted. More specifically, if the n-only VCO current is 4 times that of the p-n VCO, the LO amplitude is optimal in both cases, the phase noise is 6dB higher in the p-n VCO, and the power efficiency (FOM) is the same.

Although in principle a reconfigurable n-only to p-n VCO seems straightforward, its implementation is not trivial. In fact, the PMOS transistors must be completely switched off in the n-only case, or the tank Q becomes seriously degraded. Ensuring that this is true over a full oscillation period is difficult, since the VCO output voltage swings well above V_{dd}. This problem is solved by adopting the bias scheme depicted in Fig. 20.4.2 for the PMOS transistors. Drains and gates are ac-coupled through a tunable RC network, whose cut-off frequency is reconfigured acting on switch M5. The ac-coupling has two purposes: to easily reconfigure the dc bias of the PMOS gates, and to connect/isolate them to/from the VCO outputs. In the n-only VCO, both sources and gates are biased to V_{dd} and M5 is switched on (Fig. 20.4.2.a). In this case, the ac-coupling network has a high-pass cut-off frequency given by $2/(CR_{on})$, where R_{on} is on-resistance of M5. R_{on} is chosen small enough to guarantee a sufficient attenuation between the VCO outputs and the gates of M3 and M4, thereby keeping them off. Notice that minimizing R_{on} also maximizes the Q of the series connection of C and M5, making its impact negligible on the overall tank Q. An additional issue is that the voltage across the drain-to-bulk diodes of the turned-off PMOS transistors should never exceed the activation voltage V_D=0.7V. This is achieved with margin, if we consider a 0.5V voltage drop (V_{DROP} in Fig. 20.4.2) across the current source (carrying a maximum of 24mA), together with a V_{dd} of 1.5V. For the p-n VCO, the sources of the PMOS devices are connected to the bias current, while the dc voltage at their gates is equal to the common-mode voltage at the VCO outputs. This is achieved by connecting the center tap of the PMOS bias resistors (R_{bias}) to the center tap of the tank inductor (Fig. 20.4.2.b). Transistor M5 is now turned off, making the new high-pass cut-off frequency equal to $1/(CR_{bias})$. Choosing an R_{bias} large enough to decrease the high-pass cut-off frequency well below w_{LO} ensures proper operation of the PMOS pair without extra tank losses.

In the proposed VCO, power re-configurability has been combined with the flexibility of a digitally controlled oscillator (DCO). The scheme adopted is the ditherless one proposed in [2], which consists of a capacitively-degenerated NMOS pair. As reported in Fig. 20.4.3, the capacitance C_{fine} is reflected in parallel to the tank shrunk by a factor proportional to $g_{mN}/(\omega_{LO}C_{cal})$, where g_{mN} is the NMOS transistor transconductance averaged over one LO period, while C_{cal} is the total capacitance between the NMOS sources. The scheme of Fig. 20.4.3 differs from the one reported in [2] with respect to the trimming of the shrinking factor. In Fig. 20.4.3, the frequency is tuned acting on C_{cal} as opposed to the NMOS bias current (i.e. g_{mN}). In this way, DCO frequency resolution and current consumption can be scaled independently.

The reconfigurable DCO has been integrated in a standard 55nm CMOS process. The tank has been realized using a differential inductor of 250pH with a simulated quality factor of 15 at 7GHz. The DCO is buffered with a divider-by-2 that uses the topology proposed in [3]. Coarse tuning is the same for both n-only and p-n VCOs, and is performed at the resonant load using two capacitor banks with different resolution, controlled by 7 and 6 bits respectively. The frequency at the output of the divider-by-2 can be tuned between 3.25GHz and 4.5GHz (Fig. 20.4.4.a), with a frequency resolution of 700kHz. The fine-tuning bank, placed between the sources of M1 and M2, is controlled by a 12b digital word, whose 8 MSBs control a matrix of 16x16 varactors, connecting them either to V_{dd} or ground, while the 4 LSBs control the output voltage of a DAC that acts on the control node of a varactor [2]. Figures 20.4.4.b and 20.4.4.c report the fine-tuning characteristics of the p-n and n-only DCOs for different values of the capacitance C_{cal} (defined in Fig. 20.4.3). The fine tuning range can be programmed from 2.5MHz to 7.5MHz in p-n mode, with a frequency resolution of 0.6 to 2kHz, and between 4MHz and 10MHz in n-only mode, with a resolution of 1 to 2.5kHz. The DCO phase noise at the output of the divider-by-2, measured with a phase-noise meter, is reported in Fig. 20.4.5. In the middle of the tuning range (3.92GHz), the phase noise at 2MHz offset from the carrier is -129.3dBc/Hz for the p-n DCO and -134.7dBc/Hz for the n-only DCO, for a bias current of 6mA and 24mA respectively and V_{dd}=1.5 V. The phase noise difference between the two DCOs is 5.4dB, very close to the theoretical value of 6dB. The p-n DCO achieves a FOM of 185.6Bc/Hz, only marginally better than the n-only DCO FOM of 185.0dBc/Hz. The DCO performances are summarized in Fig. 20.4.6, while a chip micrograph is shown in Fig. 20.4.7.

Acknowledgments:
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References:
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[2] L. Fanori et al, "Capacitive Degeneration in LC-Tank Oscillator for DCO Fine-Frequency Tuning", *IEEE J. Solid-State Circuits*, vol. 45, pp. 2737-2745, Dec. 2010.
[3] S. Pellerano et al, "A 13.5-mW 5GHz Frequency Synthesizer With Dynamic-Logic Frequency Divider" *IEEE J. Solid-State Circuits*, vol. 39, pp. 378-383, Feb. 2004.

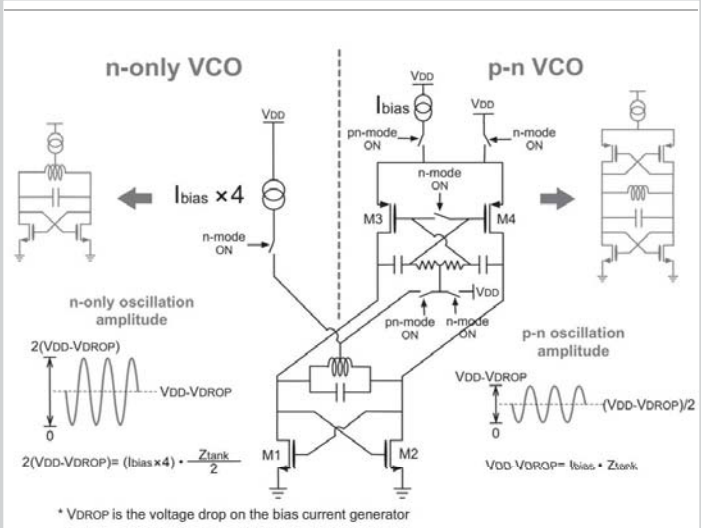

Figure 20.4.1: Power-scalable VCO with constant FOM.

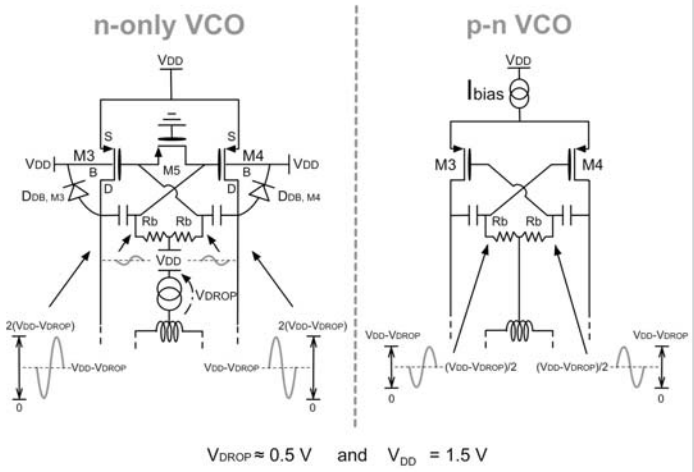

Figure 20.4.2: PMOS bias scheme.

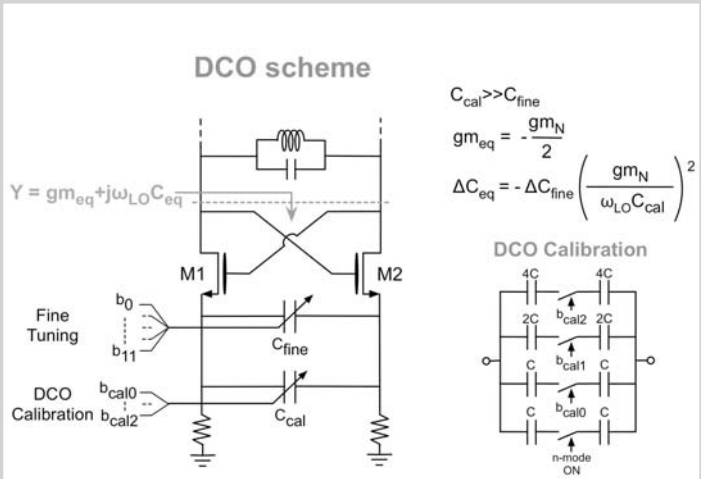

Figure 20.4.3: DCO scheme and calibration.

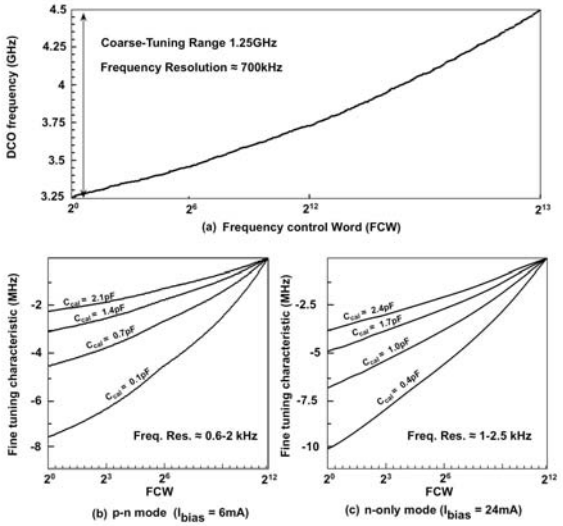

Figure 20.4.4: Tuning characteristics: a) coarse tuning, b) fine tuning p-n mode, c) fine tuning n-only mode.

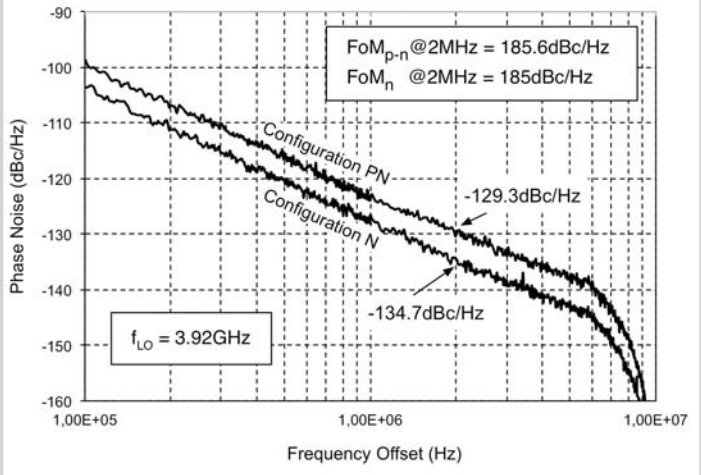

Figure 20.4.5: Phase noise measurements of the two DCO configurations after the divider.

	p-n Mode	n-only Mode
DCO Frequency	6.5-9 GHz	
Coarse Tuning Range	2.5 GHz (33%)	
Coarse Frequency Resolution	1.4 MHz	
Fine Tuning Range[a]	5 to 15 MHz	8 to 20 MHz
Fine Frequency Resolution[a]	1.2 to 4 KHz	2 to 5 KHz
Power Supply	1.5 V	1.5 V
Current Consumption	6 mA	24 mA
Phase Noise @ 2MHz[b]	-129.3dBc/Hz	-134.7dBc/Hz
FoM[b]	185.6dBc/Hz	185dBc/Hz
Technology	55 nm CMOS	

(a) Programmable by the capacitance C_{cal}
(b) After an on-chip divider by 2

Figure 20.4.6: Summary of the measurement results.

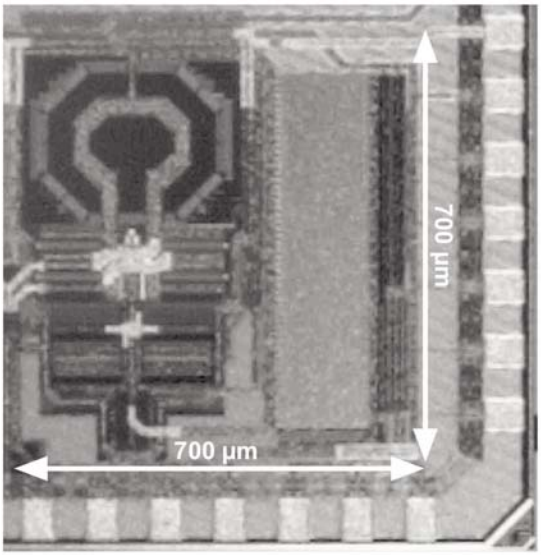

Figure 20.4.7: Die micrograph of the DCO (core dimensions: 700µm x 700µm).

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