20.7 A 6.7-to-9.2GHz 55nm CMOS Hybrid Class-B/Class-C Cellular TX VCO

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The design of very-wide-band CMOS voltage-controlled oscillators (VCOs) compliant with the phase-noise specifications of cellular transmitters is non-trivial, especially considering the GSM standard, where the phase noise exhibited by the local oscillator (LO, generated by the cascade of VCO, buffers, and usually frequency dividers) should be several dB below -162dBc/Hz at 20MHz frequency offset from the carrier. As shown in [1], challenging phase-noise requirements can embrace the WCDMA transmitter as well (e.g. -166dBc/Hz at 45MHz frequency offset for WCDMA band VIII), if cheap antenna duplexers are chosen to minimize costs. In such scenarios, and particularly in the very relevant case of WCDMA transmitting at moderate power levels, the LO power efficiency is still one of the limiting factors for a long-lasting battery life, motivating the ongoing quest for VCO power optimization.

Besides improving the quality factor (Q) of the LC-tank, which is of fundamental importance but represents a technological rather than a circuit limitation, the Class-C oscillator of Fig. 20.7.1(a) is an attractive candidate for power reduction. In fact, as demonstrated in [2], Class-C operation results (ideally) in a 36% lower bias current, compared to the commonly used Class-B oscillator, for the same oscillation amplitude and phase noise. This is because the conversion of bias current into fundamental current harmonic is more efficient in Class-C (with an ideal conversion factor $_C$ equal to 2) than in Class-B (ideal conversion factor $\alpha_B=4/\pi$).

There are, however, issues that must be solved before a low-phase-noise Class-C oscillator can be used efficiently. The primary concern is that the oscillator should indeed work in Class-C, which entails that the drain-to-source voltages of M1/M2 should not drop below their overdrive voltage. This is accomplished with the shift of the dc bias voltage V_{bias} at the gate of M1/M2, which works very well in a low bias-current scenario, where V_{bias} may be as low as the threshold voltage V_t of M1/M2 [2]. This, in turn, allows the oscillation amplitude to be a large fraction of the available supply voltage V_{dd}, before M1/M2 are pushed into the linear region. Thus, the oscillator figure-of-merit (FOM) may be extremely high, and at the same time the phase-noise performance may be inadequate for cellular standards [2]. If we now decrease the LC-tank impedance and increase the bias current, in an attempt to achieve a much lower phase noise, we are forced to increase V_{bias} as well, with the adverse consequence of decreasing the maximum allowed oscillation amplitude.

It should be noted, however, that the value of V_{bias} needed to ensure startup is in this case much higher than its steady-state value [2], since the oscillation begins in Class-A, but settles in Class-C. This key observation was used in [3] to design a composite oscillator made of a Class-C oscillator core with a very low V_{bias}, together with an additional transistor pair working much closer to Class-B, whose task is to start up the Class-C pair (Fig. 20.7.1(b)). The approach in [3], itself targeting an ultra-low-voltage, high-phase-noise application, can be modified to achieve a low phase noise as well, by introducing suitable bias networks for the two transistor pairs (in fact, in the absence of an explicit current-limitation mechanism [3], current consumption is in practice checked only by the Class-C transistors entering the linear region, defeating the goal of Class-C operation itself).

Figure 20.7.2 shows the schematic diagram of the proposed hybrid Class-B/Class-C oscillator. The bias current is injected into the LC tank by M_{bias}, while the amount of current drained by the Class-B core (M_{B1}/M_{B2}) is set by the switchable resistance R_{tail}. The large capacitor C_{top} is instrumental for operating M_{C1}/M_{C2} in Class-C, in the same fashion as C_{tail} in Fig. 20.7.1(a). Since the role of M_{B1}/M_{B2} is primarily to ensure a reliable startup of M_{C1}/M_{C2} across PVT variation, only 20% of the (maximum) bias current is diverted into M_{B1}/M_{B2}. At the same time, V_{bias} is allowed to be as low as the threshold voltage of M_{C1}/M_{C2}, i.e. approximately 500mV. It should be noted that the lack of source feedback pushes M_{C1}/M_{C2} slightly out of the saturation region when carrying the maximum current; however, the current waveforms are still effectively Class-C for all operational current levels. Assuming conservatively that the Class-C conversion factor α_C is 1.8 (instead of 2), while α_B stays at $4/\pi$, a 25% bias current reduction is achieved, compared to a purely Class-B oscillator with identical performance.

In fact, a lower bias current results in a more ideal design as well; furthermore, the impact of bias current noise is lower in the hybrid oscillator, where most of it is filtered by C_{top} [2]. The phase-noise expression for the hybrid oscillator in the $1/f^2$ region is found employing the theory in [2], and is reported in Fig. 20.7.3(a).

As already mentioned, an important difference between the oscillator of Fig. 20.7.1(a) and the proposed one is that M_{C1}/M_{C2} in Fig. 20.7.2 lack source feedback. As a consequence, in the absence of R_{dcpl}, the low-frequency noise from R_{C1}/R_{C2} finds a straightforward path to the tank, where it is converted into phase noise by unavoidable AM-to-PM conversion mechanisms. A 5MΩ R_{dcpl} pushes such noise at low (offset) frequencies, where it is easily removed by the phase-locked loop where the VCO is going to work.

The VCO has been designed in a standard 55nm CMOS process and tested. The single-turn 0.25nH inductor has an estimated Q of 15 at 7GHz. Since M_{B1}/M_{B2} carry a small fraction of bias current, their width is only 1/8 of that of M_{C1}/M_{C2}, which minimizes the parasitic capacitances. All transistors are thick-oxide devices with a length of 200nm.

The VCO is tunable from 6.7GHz to 9.2GHz with a 7b coarse MOM capacitor bank, a 6b fine MOM capacitor bank, and an AMOS varactor for continuous tuning having an average range of 15MHz. After division by 4/8, all GSM bands and several WCDMA bands are covered. The value of V_{bias} at the gates of the Class-C pair M_{C1}/M_{C2} was set to 500mV, and it was checked that increasing it to 600mV did not deteriorate appreciably the VCO performance.

Figure 20.7.3(b) shows the phase noise plot at minimum, middle, and maximum frequency, for a power supply of 1.5V and a current consumption of 18mA, after on-chip frequency division by 2 (using the divider presented in [4]) to ease measurements. The phase noise at 2MHz offset for the middle plot (with a carrier frequency of 3.95GHz) is -137dBc/Hz, which extrapolates to -157dBc/Hz at 20MHz offset, and to -169dBc/Hz after further frequency division by 4. This shows that the GSM/WCDMA phase-noise specifications mentioned in the introduction are met with margin. The $1/f^3$ noise corner varies between 100kHz and 300kHz.

Figure 20.7.4 shows a phase noise plot when M_{C1}/M_{C2} operate in Class-B, obtained by raising V_{bias} to 1.2V. The penalty compared to Class-C operation is slightly higher than 2dB at 2MHz.

Figure 20.7.5 displays the phase noise at 400kHz/2MHz offset and figure-of-merit (FOM) vs. oscillation frequency (divided by 2). The maximum FOM is above 189dBc/Hz, and varies approximately 1dB across the tuning range. This is comparable to the FOM of the VCO in [1], which was designed in an RF CMOS process. Finally, Fig. 20.7.6 summarizes the VCO performance as well as comparing it with other published VCOs meeting cellular specification. A die micrograph of the VCO, with core dimensions 700μm×700μm, is shown in Fig. 20.7.7.

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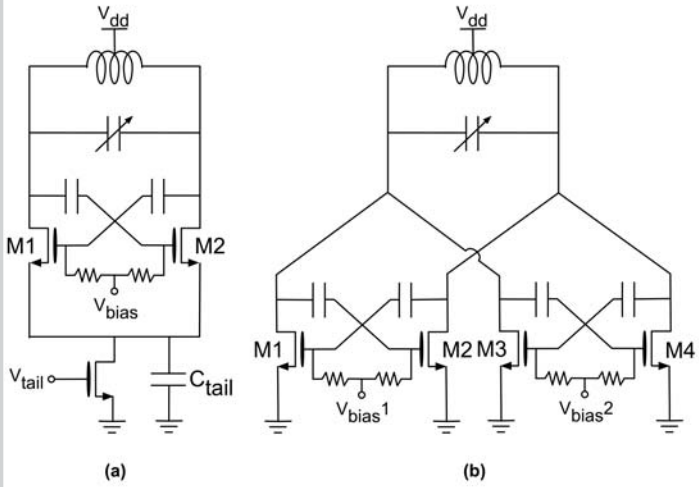


Figure 20.7.1: a) Original Class-C oscillator [2]; b) dual-conduction oscillator [3].

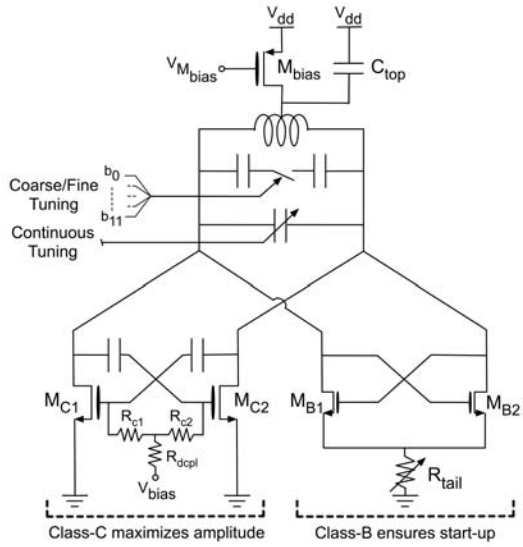
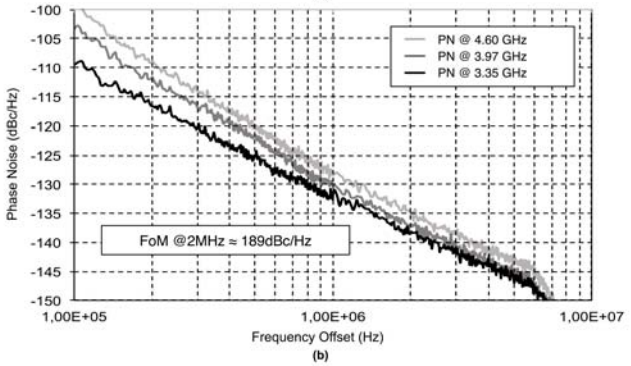


Figure 20.7.2: Proposed hybrid Class-B/Class-C oscillator.

$$L(\Delta\omega) = 10\log\left[\frac{\kappa_B T}{C^2A^2R^2(\Delta\omega)^2}\left(1+\gamma_n\right)\right] \quad \text{with} \quad A = \frac{1}{2}\left(\alpha_C I_{bias,C} + \alpha_B I_{bias,B}\right)R$$

where C (R) is the tank capacitance (parallel resistance), A the differential peak oscillation amplitude, $I_{Bias,C}$ ($I_{Bias,B}$) the bias current in the class-C (class-B), α_C (α_B) the conversion factor of bias current into fundamental current harmonic in class-C (class-B).

(a)



(b)

Figure 20.7.3: a) Phase noise equation in the 1/f² region; b) phase noise measurements at the min., middle, max. oscillation frequency (notch at 10MHz offset is an artifact of the measurement system).

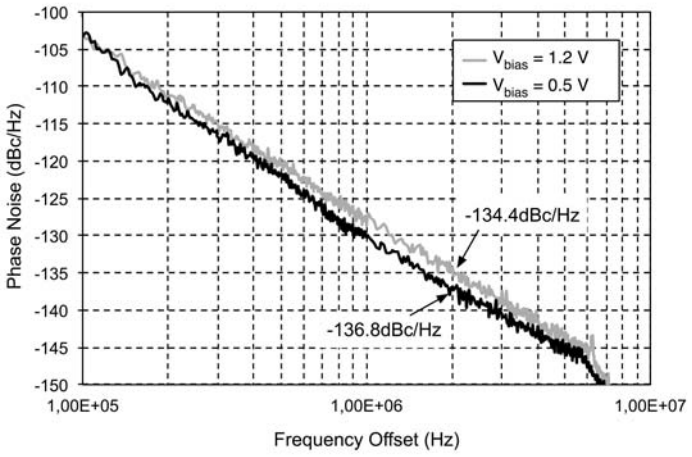


Figure 20.7.4: Phase noise measurements at mid-band, for V_{bias} = 1.2V (M_{C1}/M_{C2} operating in class-B), and V_{bias} = 0.5V (M_{C1}/M_{C2} operating in Class-C), keeping a constant power consumption.

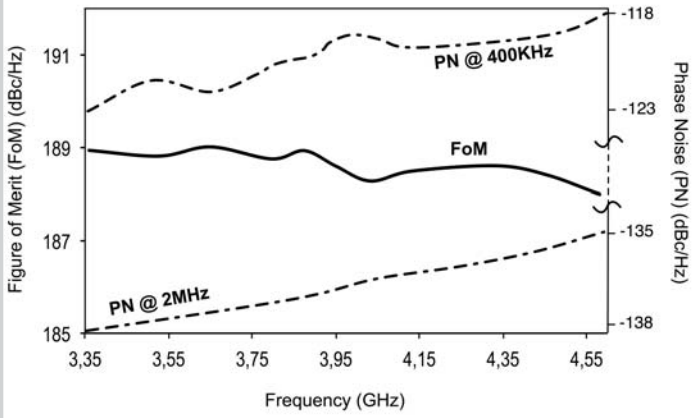


Figure 20.7.5: Phase noise at 400kHz/2MHz offset from the carrier, and figure-of-merit (FOM), vs. oscillation frequency (divided by 2).

	This work	[1]	[5]	[6]	[7]
Frequency Range [GHz]	6.7-9.2 (31%)	2.55-4.08 (46%)	3.29-3.98 (19%)	13-15 (15%)	2.9-5.4 (60%)
Phase Noise [dBc/Hz] at mid-band	-137 @ 2MHz after division by 2	-156 @ 20MHz	-149 @ 3MHz after a division by 4	-133 @ 3MHz after a division by 4	-126 @ 1MHz
Estimated Phase Noise @ 20MHz from 915MHz [dBc/Hz]	-169	-168	-167	-162	-164
Power Supply [V]	1.5	1.2	1.4	1.2	1.8
Current Consumption [mA]	18	19	18	7	7.5
FOM [dBc/Hz]	188-189	188	186	185	185-190
Technology (CMOS)	55 nm	RF 90 nm	90 nm	65 nm	130 nm

Figure 20.7.6: Comparison with the state-of-the-art in cellular TX VCO design

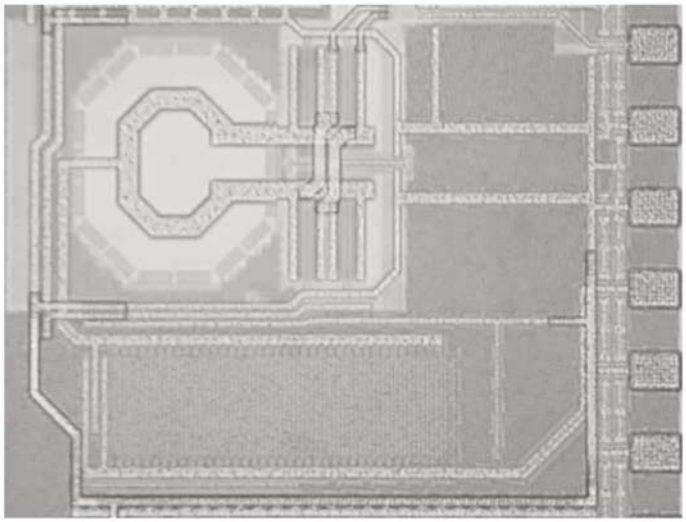


Figure 20.7.7: Die photograph of the VCO (core dimensions: 700μm x 700μm).

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