A 3.6 mW, 90 nm CMOS Gated-Vernier Time-to-Digital Converter With an Equivalent Resolution of 3.2 ps

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***Abstract*—Two gated ring oscillators (GROs) act as the delay lines in an improved Vernier time-to-digital converter (TDC), where the already small quantization noise of the standard Vernier TDC is further first-order shaped by the GRO operation. The TDC has been implemented in a 90 nm CMOS process and consumes 3 mA from 1.2 V when operating at 25 MHz. The native Vernier resolution of the TDC is 5.8 ps, while the total noise integrated over a bandwidth of 800 kHz yields an equivalent TDC resolution of 3.2 ps.**

***Index Terms*—Gated ring oscillator, time-to-digital converter, Vernier delay line.**

I. Introduction

MAINSTREAM CMOS technology scaling in modern silicon ICs favors digital circuits, as they allow for more flexibility and programmability compared to their analog counterparts. As a result, phase locked loops (PLLs), which provide precise generation and/or alignment of timing signals, have been recently explored towards a mostly digital architecture for both wireless and wireline applications. Unlike an analog PLL, a digital PLL (DPLL) potentially benefits from eliminating the area consuming passive components and leakage currents associated with a large MOS capacitor in the loop filter [1]. In addition, a DPLL offers the opportunity to employ highly efficient digital algorithms performing a continuous background calibration of the DPLL performance [2], instead of the foreground calibration typical of analog PLLs. Finally, all truly digital DPLL blocks are straightforwardly ported to further scaled process nodes. These reasons make the DPLL an attractive and relevant research topic in both academia and industry.

In a DPLL, the phase/frequency detection is carried out by a time-to-digital converter (TDC), which delivers a digitized version of the phase error between the reference clock and the feedback signal (possibly scaled in frequency) coming from the digitally-controlled oscillator (DCO, Fig. 1).

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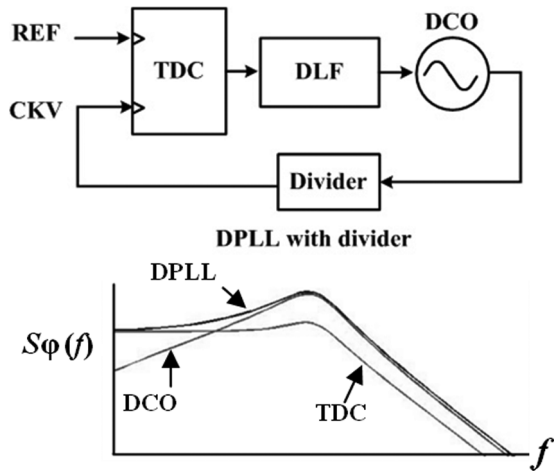

Fig. 1. top: DPLL with TDC; bottom: main noise contributions at DPLL output.

Generally, the TDC quantization noise and the DCO phase noise dominate the DPLL in-band and out-of-band noise, respectively. At the DPLL output, the power spectral density S_{TDC} contributed by the TDC quantization noise within the PLL bandwidth can be expressed as

$$S_{TDC} = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{delay}}{T_{DCO}}\right)^2 \frac{1}{f_{REF}} \tag{1}$$

where $\Delta t_{\rm delay}$ denotes the quantization time error of the TDC, T_{DCO} is the period of the DCO oscillation, and f_{REF} is the frequency of the reference clock [3]. Obviously, a smaller $\Delta t_{\rm delay}$ results in a lower in-band PLL noise.

In a straightforward delay-line TDC [4], where the time resolution is determined by the delay τ_1 of an inverter loaded by another (identical) inverter (Fig. 2(a)), the TDC quantization noise is inevitably limited by the CMOS process used, since in this case $\Delta t_{\rm delay} = \tau_1$. To overcome this limitation, more advanced approaches, based on pulse shrinking [5]–[7], passive phase interpolation [8], time amplification [9], [10] and Vernier differential delay [11], [12] have been proposed, to achieve a time resolution well below the delay of the inverter itself.

A pulse-shrinking TDC, which utilizes the difference $(= \Delta t_{\rm delay})$ between the rise time and the fall time of e.g., an inverter, is severely affected by process-voltage-temperature (PVT) variations. A passive phase-interpolating TDC uses passive devices to achieve a sub-gate-delay without increasing

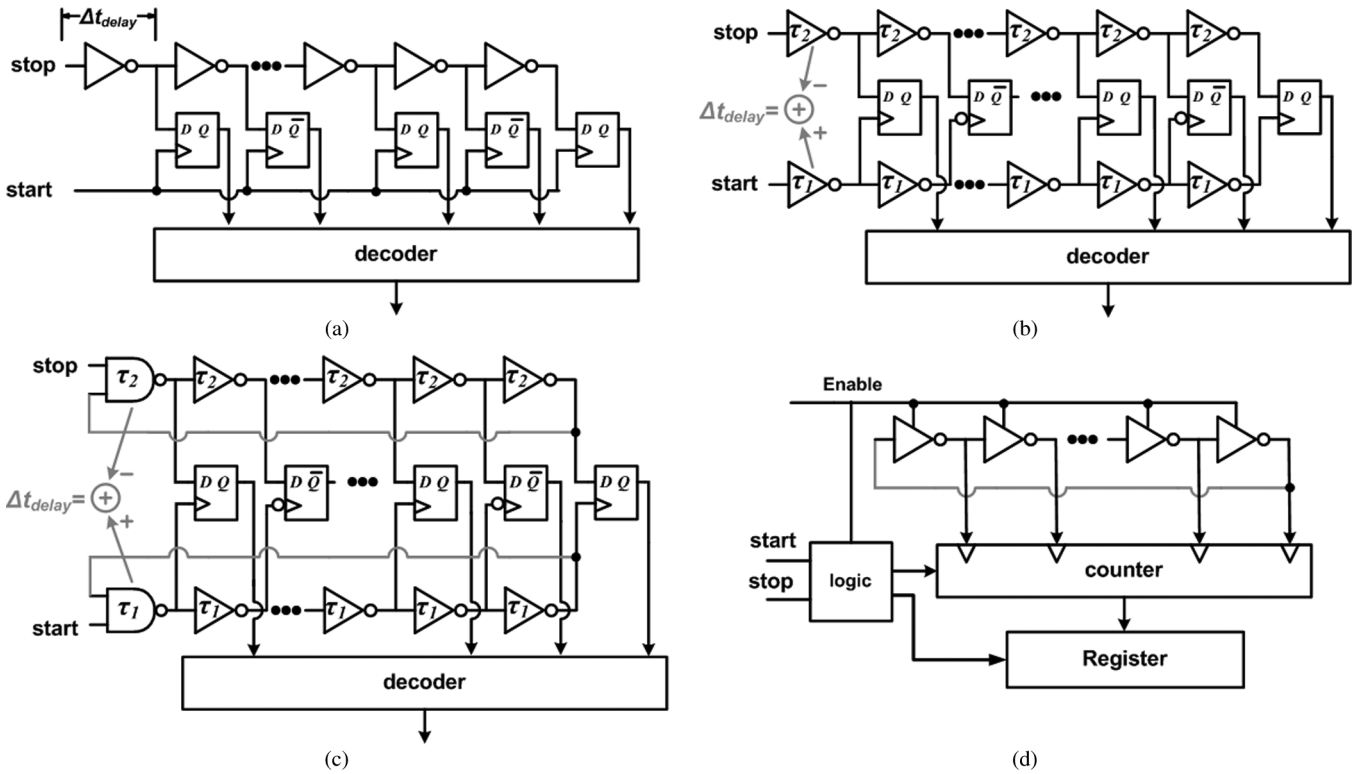

Fig. 2. Different TDC architectures: (a) basic delay-line TDC, (b) Vernier TDC [11], (c) Vernier ring-oscillator TDC [14], (d) gated-ring-oscillator TDC [15].

the output latency, but its precision is limited by parasitic capacitances on the output nodes between interpolating resistors [13]. A time-amplifying TDC amplifies the time residue from a coarse TDC, which is then resolved in a fine TDC, in the same fashion as a two-step A/D converter, with the same attending linearity issue (critically dependent on PVT variations).

A Vernier TDC uses two (rather than one) delay lines, with respective inverter delay of τ_1 and τ_2 (Fig. 2(b)). The effective time resolution $\Delta t_{\rm delay}$ is now given by the delay difference $\tau_1 - \tau_2$ (assuming $\tau_1 > \tau_2$), which can of course be designed much smaller than τ_1. Furthermore, $\Delta t_{\rm delay}$ is now first-order tolerant of PVT variations if the two lines are well matched [14]. However, since time resolution is now determined by a very small delay difference, a very large number of inverter stages is required to cover a large detection range. To solve this issue, a Vernier TDC based on ring oscillators (rather than delay lines) has been successfully demonstrated [14] (Fig. 2(c)). Since a ring oscillator can be viewed as a delay line terminated on itself, the signal can travel more than once along the delay line (i.e., the oscillator), in principle extending the detection range without bounds. However, the resolution of a ring-Vernier TDC is the same as the resolution of a Vernier TDC having the same $\Delta t_{\rm delay}$.

Noise shaping is yet another method for reducing the in-band TDC noise contribution in a DPLL. This type of TDC uses a gated ring-oscillator (GRO, Fig. 2(d)) instead of a delay line [15]–[17], with the result that the quantization error is accumulated across successive measurements. The relatively large quantization noise is therefore shaped in frequency as in a first-order $\Delta\Sigma$ modulator, i.e., it is largely pushed towards higher frequencies, where it is suppressed by the low-pass filter in the DPLL. Nevertheless, the native resolution of the GRO TDC is still set by the inverter delay, i.e., it is relatively poor.

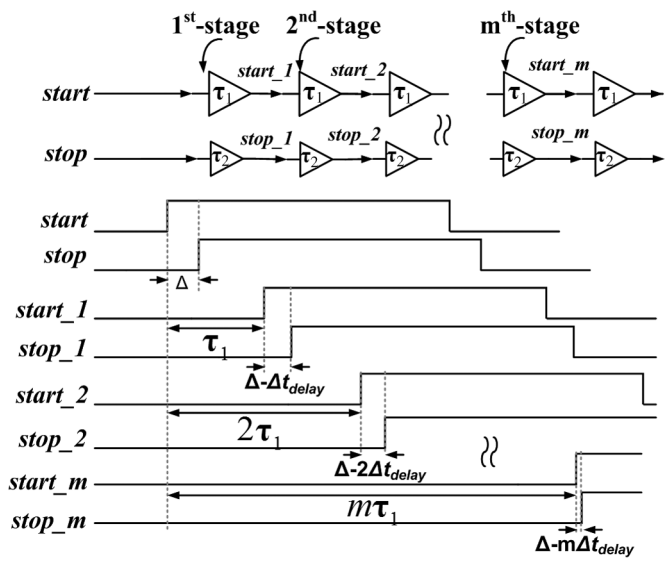

Fig. 3. Signal evolution in a Vernier TDC.

In this work, we introduce a new TDC (gated-Vernier TDC, GVTDC) that combines the ring-Vernier TDC with the GRO TDC by replacing the two ring oscillators in the ring-Vernier TDC with two GROs. As it will be shown in this paper, this merging introduces several improvements with respect to the two stand-alone architectures. Compared to a ring-Vernier TDC, the quantization noise is shaped, allowing either a lower effective quantization noise power for the same Vernier delay, or a

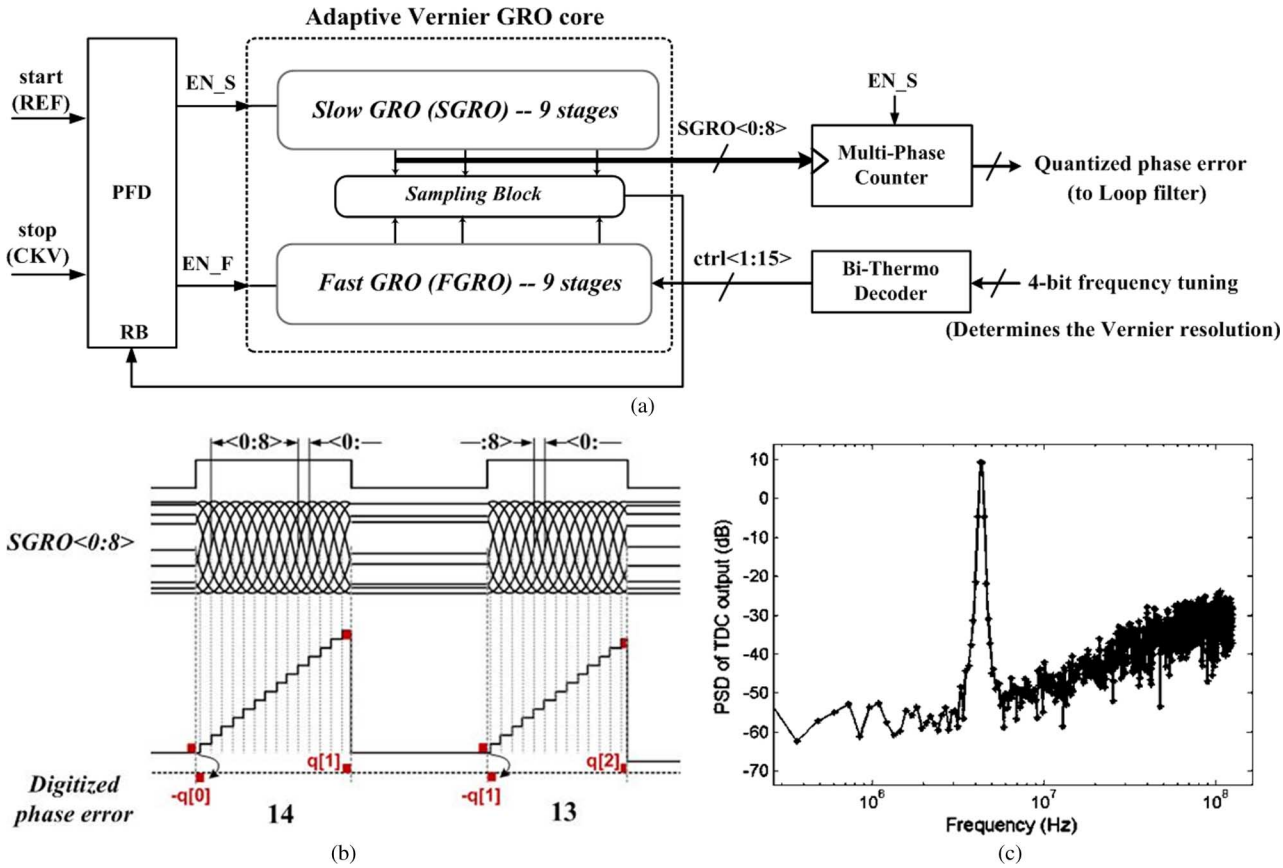

Fig. 4. The proposed TDC: (a) block diagram, (b) multi-phase counting and noise-residue accumulation, (c) first-order quantization noise shaping in frequency.

higher Vernier delay (which enables a faster TDC conversion, decreasing the typically high Vernier TDC latency) for the same effective quantization noise power; compared to a simple GRO, a GVTDC improves the (unshaped) quantization noise and reduces the number of GRO stages, simplifying the read-out of the TDC output.

This paper is organized as follows: Section II describes the proposed gated-Vernier TDC (GVTDC), Section III details the implementation of the major circuit blocks, and Section IV reports the most relevant measurement results on a fabricated prototype of the TDC. Conclusions are finally drawn in Section V.

II. Gated-Vernier TDC

As we have already mentioned, a Vernier TDC uses a sub-inverter time delay, given by the difference of two unequal inverter delays, to quantize the duration of an input pulse (Δ in Fig. 3). Referring to Fig. 3, the time width of the input signal decreases by $\Delta t_{\mathrm{delay}}$ after passing through each delay-stage pair, and the minimum time needed to detect a time width of Δ becomes $\tau_1 \times \Delta/\Delta t_{\mathrm{delay}}$, where $\Delta/\Delta t_{\mathrm{delay}}$ yields the number of delay-stage pairs needed by the operation. Although a smaller time resolution can be obtained, well beyond the one possible with a single delay line, the number of quantization levels is still proportional to the number of delay cells and time comparators (e.g., flip-flop). This limits severely the maximum full scale achievable, due to a complexity that grows exponentially with the number of bits. In the literature this problem is partially solved by adopting a 2-dimensional Vernier architecture, where the number of stages per delay lines is drastically reduced [18]. Nevertheless, a time comparator for each quantization level is still required.

The proposed GVTDC is illustrated in Fig. 4. It includes an adaptive Vernier GRO core (which can work in two different modes), a phase-frequency detector (PFD), and a multi-phase counter. The GVTDC leads to a significant reduction of the number of delay stages and time comparators, rearranging the two delay lines into a couple of ring oscillators [14]. With respect to [14], the two ring oscillators are here transformed into a couple of GROs exploiting the noise-shaping properties described in [15].

The PFD senses the delay between the two inputs *start* and *stop* (in a DPLL, these would e.g., be the reference clock and the feedback DCO signal, respectively) and generates two enable pulses, EN_S and EN_F, controlling the Vernier GRO core. The quantized delay generated by the GRO core is then read out by the multi-phase counter. To ensure the correct operation of the GRO core, EN_S always leads EN_F (as explained in detail in Section III).

The Vernier GRO core consists of two GROs (Fig. 4, each with 9 delay stages) and a sampling block. One GRO (fast GRO, FGRO) has a slightly higher oscillation frequency than the other GRO (slow GRO, SGRO). The SGRO is started by EN_S, so that the FGRO, started by EN_F, can catch up with it in Vernier-like fashion, since the delay between the leading phase in the SGRO and the leading phase in the FGRO decreases by $\Delta t_{\mathrm{delay}}$ across each new delay-stage pair. When the FGRO has

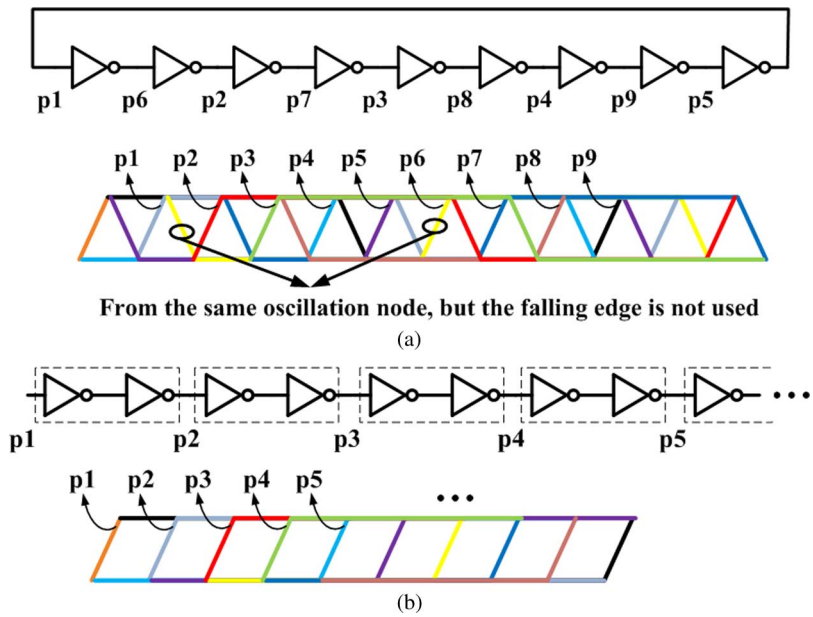

Fig. 5. The phase sequence concerning only rising edges (a) in a ring oscillator; (b) in a delay line.

caught up with the SGRO, the state of both GROs is frozen by a falling EN_S/EN_F, and the number of delay cells that have experienced one (or more) rising transitions yields the quantized delay output. The capacitance at each node in both SGRO and FGRO holds now the voltage value at the freezing instant (Fig. 4(b)); during the next measurement cycle, each GRO starts from this state, rather than discarding it, as would be the case in a standard Vernier TDC. In this way, the quantization error is accumulated across all measurements, resulting in the expected first-order shaping shown in Fig. 4(c), obtained through high-level simulations in a Simulink platform.

Of course, an important challenge in the GVTDC is that each measurement starts from a different SGRO/FGRO delay-cell pair, rather than always from the first pair as in a normal Vernier (or ring-Vernier) TDC. On the other hand, the ideally random rotation of the starting delay-pair cell has the additional momentous advantage of avoiding harmonic tones due to the mismatch between the delay cells in the GROs [15].

The number of delay cells used by the GROs during the measurement is counted by a multi-phase counter clocked by all staggered phases from the SGRO. An enable pulse allows an accumulator to be triggered by the rising edge of the SGRO phases; at the falling edge of the enable, the counter saves the result and resets the accumulator for the next measurement.

It should be noticed that only the rising edge of the GRO phases is used in the sampling block, in order to avoid the mismatch between inverter rise time and fall time. This means that there are two GRO inverters between neighboring phases, as shown in Fig. 5(a), where consecutive numbers denote neighboring phases. It is worth noticing from Fig. 5(a) that a 9-stage oscillator is capable of producing a 9-phase interpolation of the oscillation period. If such non-inversion phases are used in a delay-line TDC, two inverters are needed in each delay cell [18], and twice as many inverters are required to obtain the same number of phases, as shown in Fig. 5(b).

The sampling block of Fig. 4(a) has the task of determining when the FGRO has caught up with the SGRO. A straightforward solution would be to feed each start/stop input pair to a D flip-flop [4], [19]; however, the rather poor metastability performance of the D flip-flop would impact on the frequency noise shaping of the quantization time error. A sense-amplifier-based flip-flop can be used to improve the flip-flop performance [3], at the cost of a higher power consumption. In this work, a simple SR latch is inserted before the D flip-flop, which enables the detection of an input delay with a much narrower metastability region. The drawback of this choice is that the level sensitivity of the SR latch results in a narrower maximum detection range in the GVTDC.

To recover a wider detection range, we introduce a second working mode for the GVTDC, where only one GRO is active. In this way, we revert to a single-GRO TDC operation [15], with an unlimited detection range. This will be explained in more detail in the next Section.

III. Circuit Implementation

This section discusses the detailed circuit implementation of the proposed TDC, analyzing the constitutive building blocks: the Vernier GROs, the sampling bock (i.e., the time comparator), the phase and frequency detector and the multiphase counter.

A. Vernier Gated-Ring-Oscillator Core

To get a high Vernier time resolution, two 9-stage ring oscillators with different frequency tunings are used in the GRO core, as shown in Fig. 6. The frequency of both is controlled acting on each delay cell by a 15 thermometer-coded capacitor bank, which allows to control Δt_{delay} with a resolution of 1.2 ps (Fig. 6(b)). The delay cells include also 2 gating switches that turn the ring oscillator into a GRO [15]. When both gating switches are on, SGRO and FGRO are running like regular ring

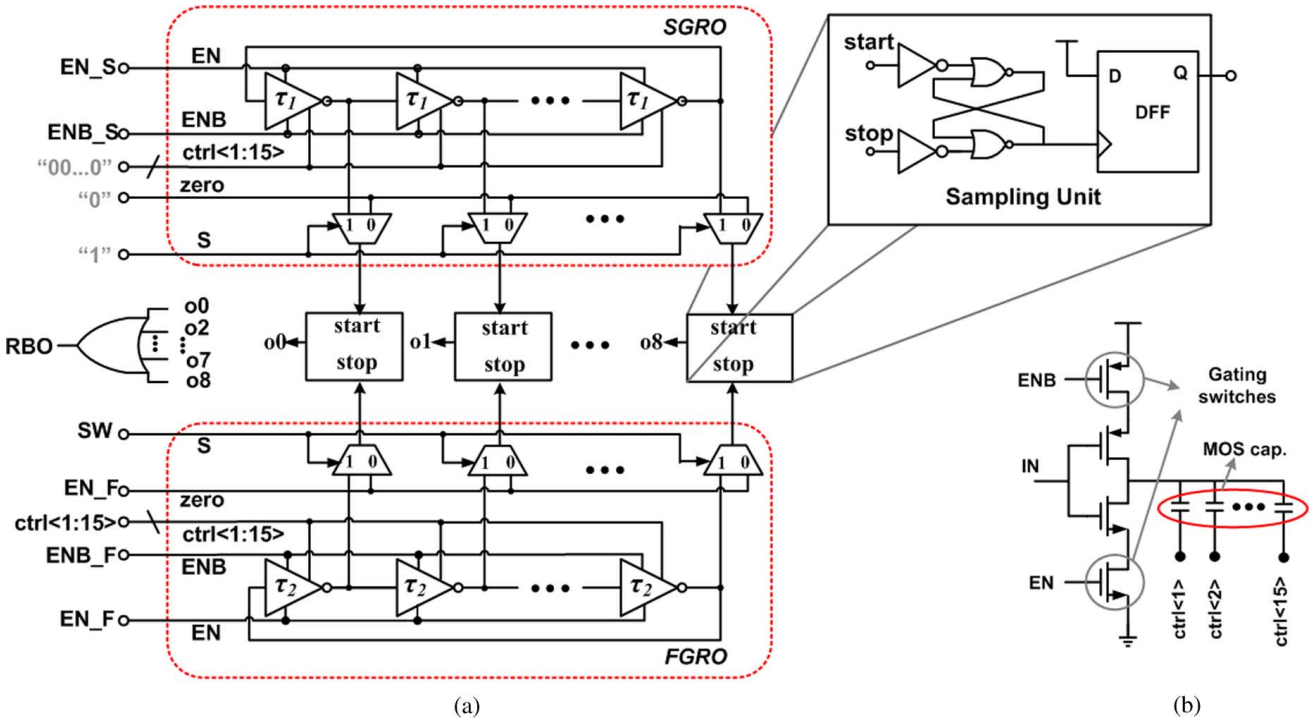

Fig. 6. Vernier GRO (a) core part, (b) gated inverter (cell) with capacitive delay control.

oscillators; when they are off, SGRO and FGRO hold the oscillator state, as previously illustrated in Fig. 4(b). For simplicity, the Vernier resolution is set by acting on the control signal of the FGRO, keeping the oscillation frequency of the SGRO as low as possible (corresponding to the maximum capacitance load for the delay cells).

Notice that, compared to the solution presented in [15], the large latency accumulated along the GROs in the GVTDC allows a reduction of the number of stages required by the GROs, minimizing the complexity of both GRO and multiphase counter. Indeed, in a simple GRO the number of stages is univocally set by the ratio between the GRO oscillation period, $\mathrm{T_{GRO}}$ (proportional to the length of the self-loaded delay line), and the (unshaped) time resolution. Since the multiphase counter limits the GRO frequency (i.e., $1/\mathrm{T_{GRO}}$) and the unshaped time resolution must be kept as high as possible, the result is generally a large number of stages. On the contrary, in the GVTDC, the oscillation frequency of each GRO does depend on the absolute delay per stage (i.e., τ_1 and τ_2 in Fig. 6), but not on $\Delta \mathrm{t_{delay}}$, and thus the unshaped resolution can be set independently of the oscillation frequencies of the GROs.

Another issue in the GVTDC is to ensure that the SGRO phases lead the FGRO phases at the beginning of each measurement window. This is a challenge in presence of device delays. If, as an example, phase $FGRO\langle n\rangle$ (see Fig. 7(a)) has caught up with $SGRO\langle n\rangle$, the sampled result $o\langle n\rangle$ is supposed to become active immediately. In fact, some propagation time is unavoidable, as illustrated in Fig. 7(a). This gating delay may accumulate to up to 200 ps before EN_S and EN_F respond. During this time, the two GROs are still active; however, no further rising edges (right bottom of Fig. 7(b)) should be generated by the GRO core, otherwise an incorrect sampling operation may occur in the following measurement (left bottom of Fig. 7(b)). A straightforward solution is to increase the absolute delays in the cells of the GROs, so that the delay between adjacent rising edges in each GRO is larger than the total time lag in the feedback path. An additional large fixed load capacitance is therefore added to each GRO cell. The resulting long absolute delays help converting the gating delay to a small dc offset, avoiding wrong samplings. The large load capacitance, in addition, is beneficial for holding charges of oscillator nodes between measurements [20]. On the other hand, a large absolute delay-cell delay results in a large delay mismatch and jitter, compared to the Vernier resolution, which increases both noise and non-linearity. In this work, 400 ps has been adopted for adjacent rising edges. The simulated rms jitter of the GRO, integrated over the bandwidth 100 Hz-1 GHz, is 0.38 ps, which is much below the time resolution of the GVTDC, shown in Section IV.

B. Sampling Block

The sampling block consists of nine identical units that are used to read the phase information for each delay-stage pair, finding the instant when the FGRO catches up with the SGRO. As mentioned before, the sampling unit is realized by inserting an SR latch before a standard D flip-flop (top right of Fig. 6(a)). In a delay-line TDC, having only non-inversion delay cells, no falling signal edges are produced during the detection process, provided the input pulse is much smaller than half of the sampling period. An SR latch can therefore be used as an arbiter (sampling unit) [9], [18].

However, in a ring-oscillator TDC, where falling edges alternate with rising edges, the level sensitivity of the SR latch will limit the maximum detection range. A correct sampling is

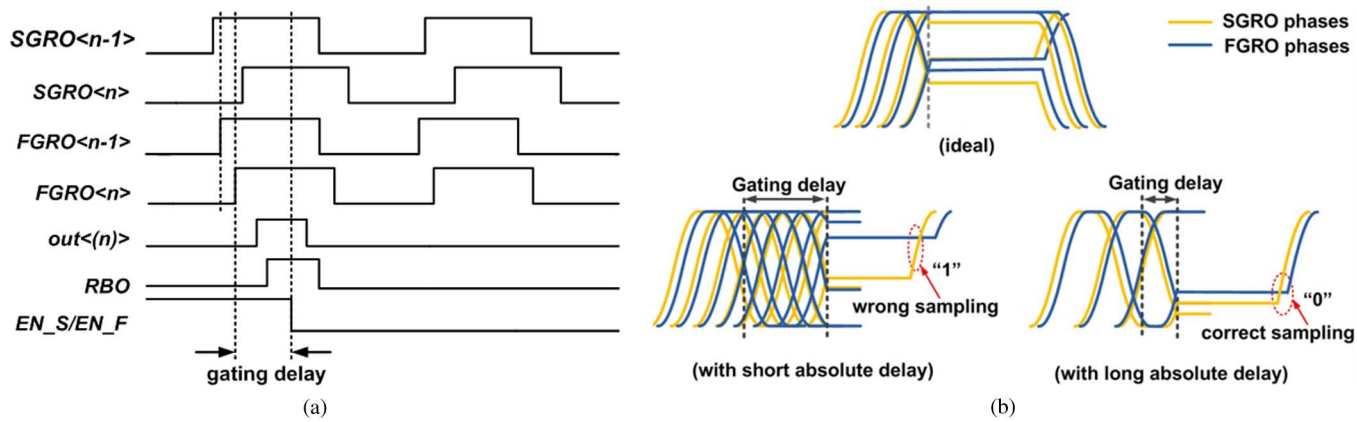

Fig. 7. Gating delay: (a) waveform illustration, (b) effects for short and long absolute delay.

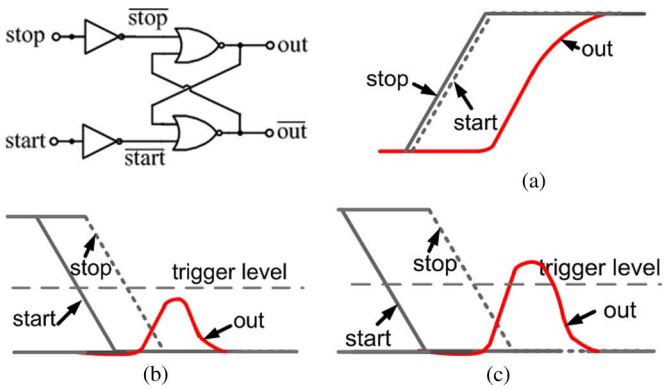

Fig. 8. SR latch: (a) correct sampling when *stop* catches up with *start*, (b) acceptable *start-stop* delay.

shown in Fig. 8(a), where a rising edge of *stop* just catches up with a rising edge of *start*. Simulations show that even a very small lead (<1 ps) for *stop* is enough to generate a valid trigger (*out*) for the D flip-flop. However, too large a lag for *stop* (often occurring at the beginning of each measurement) may generate a faulty signal for the D flip-flop: Fig. 8(b) shows a falling-edge *start-stop* delay that allows *out* to rise close to the trigger level of the D flip-flop, yet without passing it; however, if the *start-stop* delay increases further, the D flip-flop will be incorrectly triggered (Fig. 8(c)). As clear from Fig. 8, this happens because falling signal edges are used for sampling. With the time-comparator architecture used in the test chip, the maximum acceptable value of the *start-stop* delay, i.e., the detection range of the GVTDC, is approximately 120 ps.[1]

Since the faulty sampling is caused by the falling edge of the *stop* signal, a second operation mode is introduced, removing the falling *stop* edges within the measurement window when the pulse at the TDC input is very wide (e.g., during the acquisition of the PLL lock). This is realized buffering the GRO outputs with 9 multiplexers with control signal SW (Fig. 6). When SW is enabled, the TDC is transformed into a plain GRO, where only the SGRO is used, while the FGRO is disabled. This results in an unshaped resolution equal to an inverter delay. This approach leads to a TDC characteristic with different resolution segments, similar to the one proposed in [22].

[1]Notice that this limit is not intrinsic of the GVTDC architecture itself, but of the sampling block adopted in the prototype. A more efficient approach, which solves the problem of the limited detection range of the GVTDC, can be found in the solution presented in [14], or in the customized flip-flop proposed in [21].

C. Phase & Frequency Detector

In a typical PLL architecture, a static delay is used in front of the TDC to guarantee the presence of a phase offset between the two inputs REF and CKV, ensuring a linear operation. Such a delay is equal to one or more DCO periods, covering the time range spanned by the sigma-delta divider in a fractional-N PLL during lock. However, during lock acquisition it is generally not possible to guarantee that REF always leads CKV. On the other hand, the GVTDC works properly only if EN_S always leads EN_F.

This issue is solved by the adaptive phase-frequency detector (PFD) of Fig. 9, which generates an EN_S always leading EN_F, independently of the phase relation between REF and CKV. The PFD makes use of two true-single-phase-clock flip-flops having an always-high internal "D" input [23], and of an SR latch used as an arbiter. The arbiter senses the leading edge between REF and CKV, and generates a *sign* signal controlling four multiplexers. When REF is leading, EN_S corresponds to REF, while when CKV is leading, EN_S corresponds to CKV. The *sign* signal should also be sent to the digital loop filter when the TDC is working in a DPLL, to indicate a positive or negative phase error.

D. Multi-Phase Counter

In a GRO TDC the number of delay stages is given by the ratio of the GRO oscillation period to the (unshaped) time resolution. Thus, there is a trade-off between speed and complexity of the digital read-out circuitry. In fact, if the GRO has only a few stages (down to a minimum of three), its oscillation frequency is high (for a given time resolution), as so must be the speed and power consumption of the read-out. If the GRO has many stages, the speed of the read-out decreases, but the number of phases that must be read increases [17].

This trade-off is overcome by the GVTDC, since its time resolution is independent of the choice of GRO oscillation frequency and number of stages, which means that the read-out circuitry is relatively simple and operated at moderate speed.

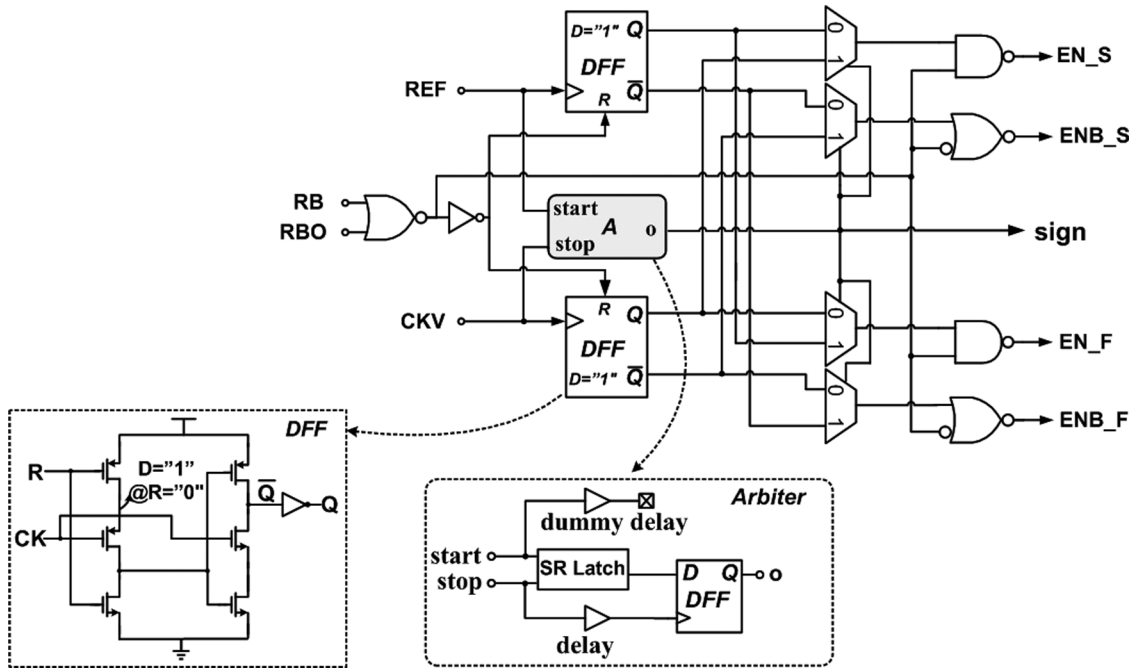

Fig. 9. Adaptive phase-frequency detector.

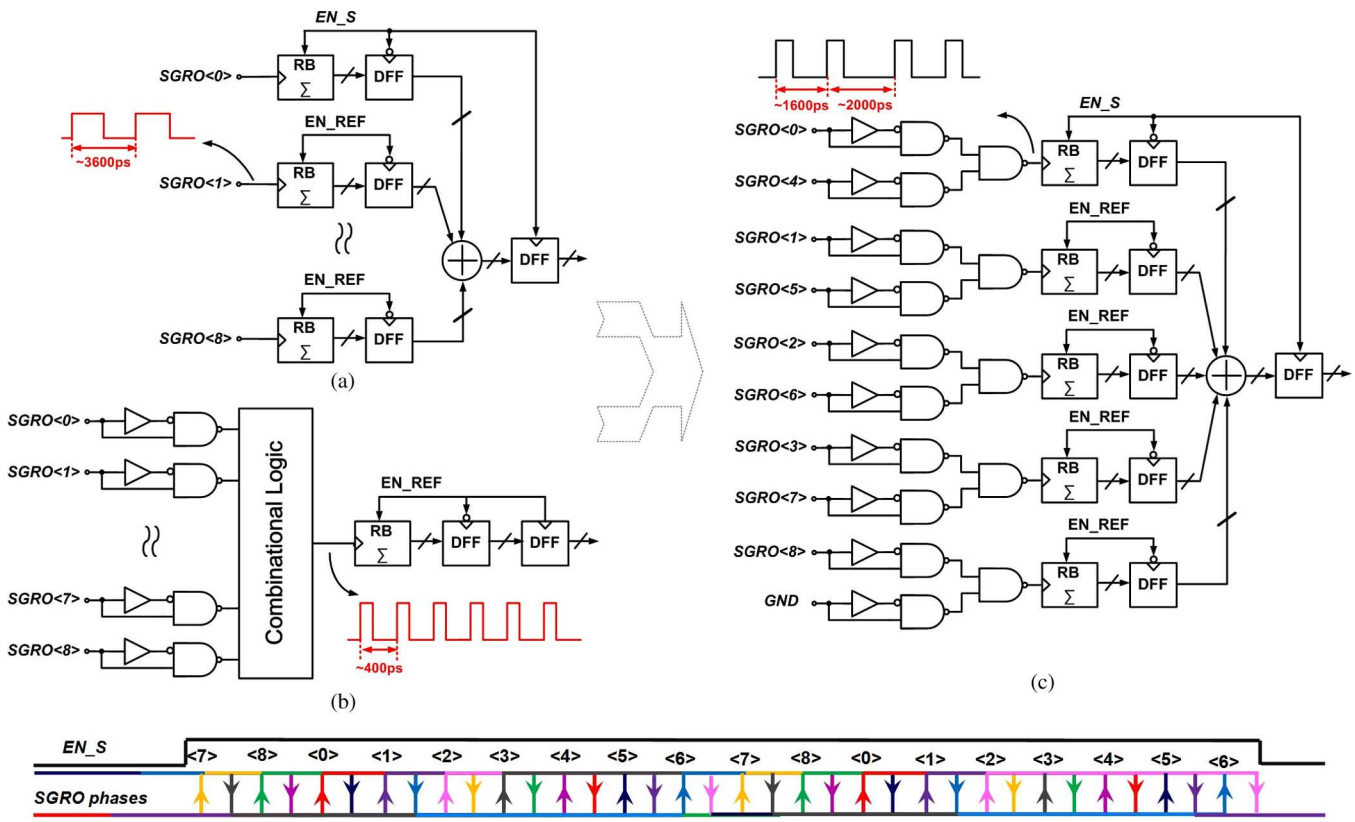

Fig. 10. Multi-phase counter with (a) an individual accumulator for each SGRO phase, (b) only one accumulator with all SGRO phases combined to a single one, (c) proposed trade-off solution.

In this work, the TDC output is read by a multi-phase counter. For a multi-phase counter, an obvious approach is to assign an individual accumulator to each phase (it will be remembered that each phase can become active more than once during each measurement), a choice requiring as many adders and flip-flops as the number of output phases (Fig. 10(a)); however, the speed of each accumulator does not have to be very high, since it only needs to work correctly at the fundamental oscillation frequency of SGRO. If, on the other hand, all SGRO phases are combined into a single signal containing all edges, only one ac-

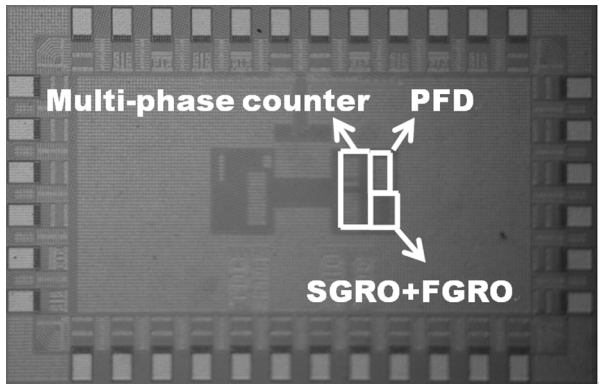

Fig. 11. Chip micrograph.

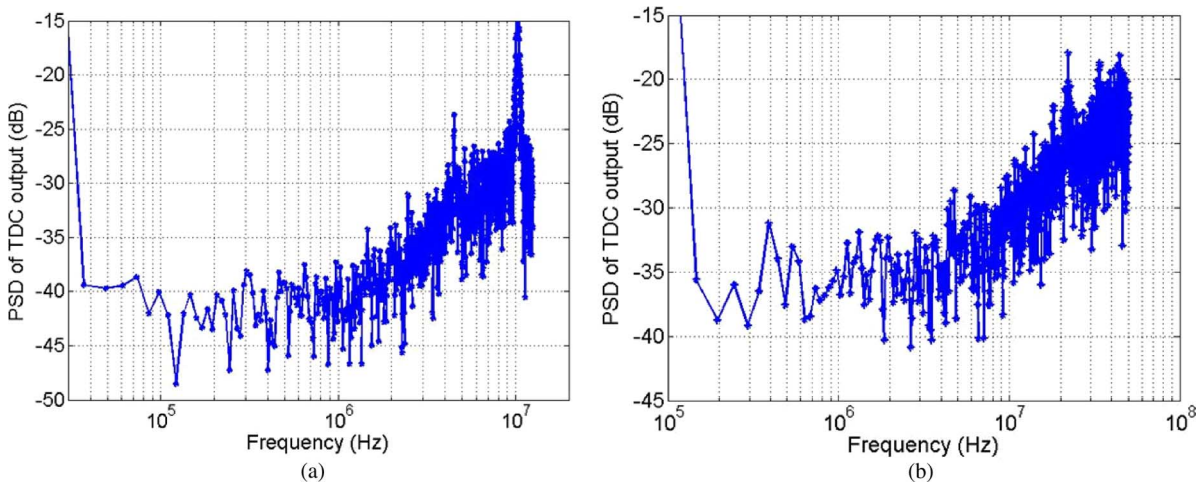

Fig. 12. Measured TDC output PSD with dc delay input of 20 ps: (a) Vernier resolution of 5.8 ps @25 MHz, (b) Vernier resolution of 6.5 ps @100 MHz.

cumulator would suffice (Fig. 10(b)), but this composite signal would be at a higher frequency, bearing on the accumulator speed. In the prototype, we combined the two above solutions by grouping the 9 SGRO phases in pairs, where the two phases in each pair are separated by the largest possible delay. In this way, a good compromise between hardware complexity and speed/power consumption is obtained.

IV. Measurement Results

The GVTDC has been implemented in a 90 nm standard CMOS process. Fig. 11 shows the die photo of the GVTDC, where the active area is 0.18 mm · 0.15 mm.

The most straightforward way of testing the TDC is by measuring the delay between two input signals *start* and *stop* having the same frequency, but different phases. Since the delay between the two signals is constant, this measurement yields a dc value in the spectrum of the TDC output. Fig. 12 shows the power spectral density (PSD) of the Hann-windowed TDC output (normalized with respect the quantization resolution) for a dc delay of approximately 20 ps and two different values of the Vernier resolution, when the input signals have a frequency of 25 MHz and 100 MHz, respectively. The two plots clearly show the effectiveness of the proposed TDC, were most of the quantization noise is pushed toward high frequencies (since the frequency of the input signals is the sampling frequency as well, the resulting Nyquist frequency in Fig. 12 is 12.5 MHz and 50 MHz), although with a slope slightly lower than the 20 dB/decade expected from theory. Assuming that the TDC is used in a DPLL having a bandwidth of 800 kHz (i.e., operating the TDC with an oversampling ratio OSR of ∼16), the in-band SNR for the PSD in Fig. 12(a) is approx. 40 dB, corresponding to an in-band rms noise of approximately 200 fs. To achieve the same SNR with the same OSR but assuming a white noise PSD, the required Δt_{delay} is 3.2 ps, which is clearly below (although not by a large amount) the Vernier delay of 5.8 ps employed in the measurement. It should be noticed that the in-band noise in the PSDs of Fig. 12 is not shaped but rather white, indicating that its origin is most likely thermal, either in the form of jitter on the input signals, or from power-supply generation, or possibly from other noise sources in the measurement setup.

Fig. 13 illustrates the measured PSD of the TDC output when the delay between REF and CKV varies sinusoidally in time, which is made possible by a Tektronix DTG5274 Data Timing Generator. Two Vernier resolutions (15 ps and 6 ps) and sampling frequencies (50 MHz and 62.5 MHz) are used for these measurements. Unfortunately, a relatively large 2.5 MHz spur and its harmonics are present on the generated sinusoidal delay (Fig. 14), making a quantitative analysis of the PSDs in Fig. 13 unreliable. Nevertheless, by removing the high-frequency spurs from the PSD, it can be appreciated that the sinusoidal input

TABLE I
TDC PERFORMANCE AND COMPARISON WITH STATE-OF-THE-ART

	[17]	[14]	[8]	[4]	[18]	[9]	This work
Type	GRO	Vernier-ring	Passive interpolation	Delay-line	2-D delay-line	Time amplifier	Vernier +GRO
Sampled Rate (MS/s)	50	15	180	26	50	10	25~100
Resolution (ps)	1*	8	4.7	20	4.8	1.25	3.2*
Power Supply (V)	1.5	1.5	1.2	1.3	1.2	1.5	1.2
Range(ns)	12	32	0.6	0.64	<0.6	0.64	40**
Power (mW)	2.2-21	7.5	3.6	6.9	1.7	3	3.6/4.5***
Area (mm^2)	0.04	0.26	0.02	0.01	0.02	0.6	0.027
Technology (nm)	130	130	90	90	65	90	90

* Effective resolution with OSR of 25([17]) & 16 (this work)
** Full-period detectable range with plain-GRO working mode
*** Gated-Vernier / plain-GRO working mode for the full scale at 25MHz sample rate

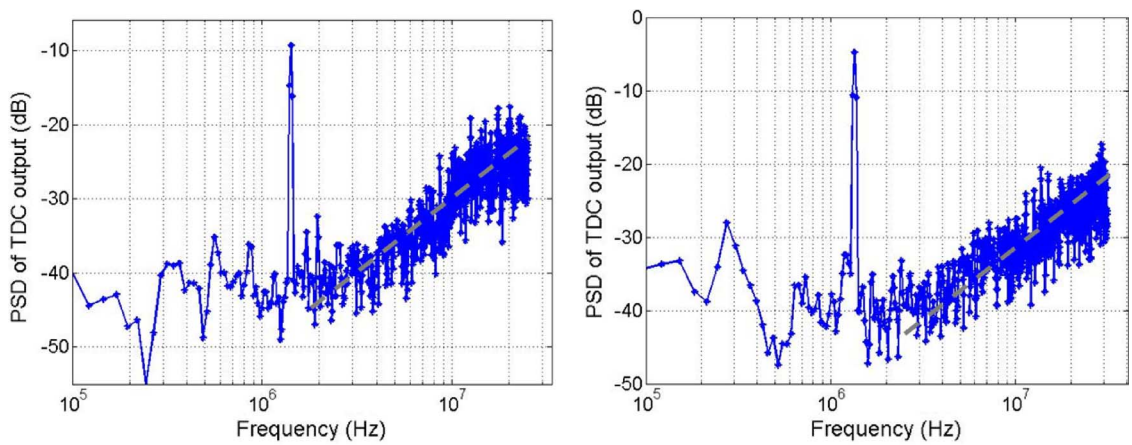

Fig. 13. Measured TDC output PSD with sinusoidal delay input (a) Vernier resolution = 15 ps@50 MHz, (b) Vernier resolution = 6 ps@62.5 MHz.

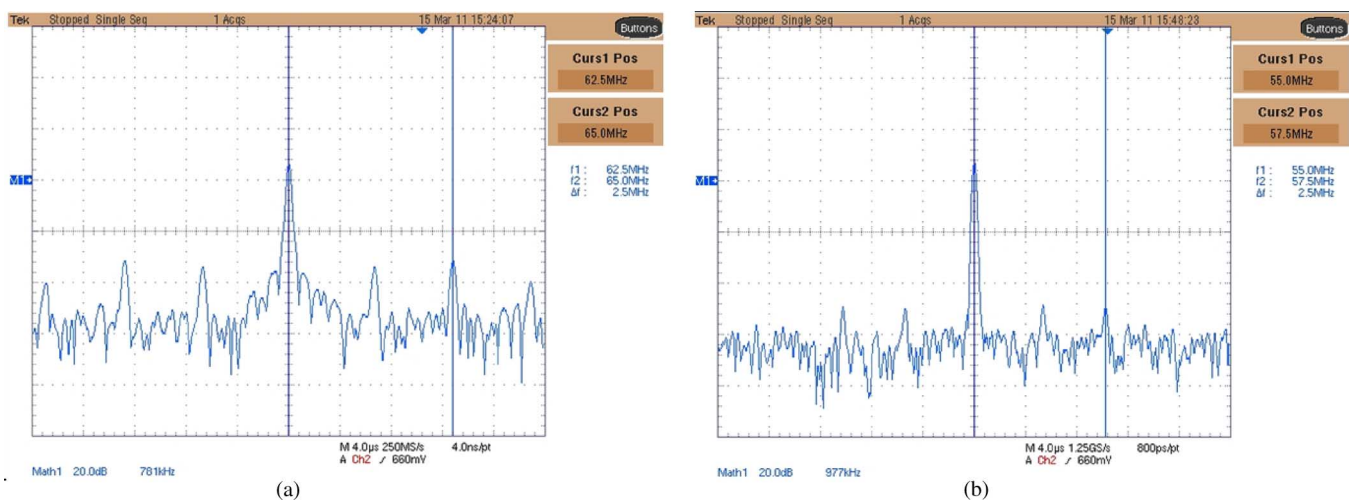

Fig. 14. Measured 2.5 MHz spur at reference clock for different input frequencies: (a) 62.5 MHz, (b) 55.0 MHz.

results in a quantization noise shaping following the expected first-order 20 dB/decade slope.

Working at a 25 MHz sampling frequency, the current consumption of the GVTDC is 3 mA from 1.2 V. A summary

of the TDC performance, together with a comparison with the state-of-the-art, is displayed in Table I.

V. Conclusions

We have presented a Vernier TDC that makes use of two gated-ring oscillators instead of two delay lines. The TDC, fabricated in a standard 90 nm CMOS process and consuming 3 mA from 1.2 V, displays a first-order shaping of the quantization noise. Compared to a ring-Vernier TDC, the proposed GVTDC shapes the quantization noise, improving the trade-off between time resolution and conversion speed. With respect to a GRO TDC, the GVTDC improves the trade-off between the (unshaped) time resolution and the absolute delay of GRO stages. This results in a more flexible TDC design, where the GRO frequency, the number of stages and the time resolution can be set independently of each other. The above described TDC is well suited for use in a high-speed digital PLL.

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