# A Dither-Less All Digital PLL for Cellular Transmitters

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***Abstract*—An all-digital frequency synthesizer for cellular transmitter is presented. Low phase-noise is achieved both in-band and out-of-band exploiting a 2-dimensional Vernier time-to-digital converter and a dither-less digitally controlled oscillator. These building blocks heavily rely on digital calibration techniques to precisely and efficiently implement two-point modulation and spur cancellation in the presence of implementation impairments. The presented prototype shows an in-band phase noise of −108 dBc/Hz, an out-of-band phase noise of −160 dBc/Hz @20 MHz and in-band fractional spurs below −50 dBc. These results are obtained for an output carrier of 1.8 GHz, a reference clock of 26 MHz, with a power consumption of 41.6 mW.**

***Index Terms*—All digital PLL, calibration, digitally controlled oscillator, frequency synthesis, phase locking, time to digital converter.**

## I. Introduction

In RECENT years, digital frequency synthesizers have become very popular thanks to the flexibility offered by digital signal processing. Performances equivalent to analog solutions have been combined with the possibility of exploiting efficient digital-calibrations and fast frequency-phase locking acquisitions (e.g., gear shifting) [1].

To preserve comparable performance with analog implementations, the conversion of an analog phase-locked-loop (PLL) into a digital one requires a very fine quantization of time and frequency. For example, the digitally controlled oscillator (DCO) frequency resolution must be lower than 1 kHz for a 900 MHz carrier to achieve a phase noise (PN) of $-165\ \mathrm{dBc/Hz}$ @ 20 MHz (from GSM transmitter specs) [1]. At the same time, if an in-band phase noise below $-105\ \mathrm{dBc/Hz}$ is sought, a time-to-digital converter (TDC) time resolution close to 5 ps is required for a 2 GHz output carrier and a 26 MHz reference clock. The fractional-N all-digital PLL (ADPLL) presented in this paper reaches both targets exploiting a dither-less DCO and a 2-dimensional highly linear Vernier TDC.

The modulation of the transmitted signal through direct control of the frequency synthesizer is becoming a widely adopted technique using phase or frequency modulations (e.g., for GSM transmitters) [1]. For these applications, the advantages given by a digital approach in terms of calibration and re-configurability allow replacing the traditional direct-up architecture with the use of polar or out-phasing techniques even when non-constant envelope modulations are used (e.g., WCDMA) [2]. In this paper we present an ADPLL for GSM transmitter featuring wideband direct phase modulation.

This paper is structured as follows. An overview of the proposed ADPLL architecture is given in Section II. The 2-dimensional Vernier TDC and the dither-less DCO are described in Sections III and IV respectively. Section V reports the frequency-phase locking acquisition schemes. The calibration algorithms implemented in the system are discussed in Section VI referring issues. In Section VII the measurements results of the ADPLL prototype are reported. Finally, the appendix provides some stability remarks on the TDC gain calibration loop.

## II. ADPLL Architecture Overview

Digital PLLs are usually obtained from analog ones splitting the loop into two domains, an analog one, which contains the oscillator, and a digital one, which typically includes the loop filter. The position and the characteristics of the A/D and D/A interfaces define the architecture of the digital PLL giving rise to several alternative topologies [3]–[6].

In this paper we present a digital PLL where the D/A interface is placed at the DCO input and the A/D interface is placed at the phase-frequency detector (PFD) level, using a high resolution TDC to perform phase comparison [3]. The DCO has enough resolution not to require dithering. The analog path from the RF output to the divided edge is exactly the same as in a classic PLL. The architecture is shown in Fig. 1 and implements a type II fractional-N loop. There is a straightforward analogy with the analog PLL, the main differences being that in the digital domain an accurate $\Sigma\Delta$ noise cancellation can be achieved and that the loop filter can be easily reconfigured. The latter possibility [1] allows not only reconfiguration to different standards but also the use of gear shifting to achieve very fast locking times.

An alternative approach to implement a digital PLL consists in placing the A/D interface directly at RF, using a counter at the output of the DCO (or after a few divider stages to decrease the counting frequency). This solution eliminates the need for a multi-modulus divider chain replacing it with an RF-counter [1], [4]. The operation of a multi-modulus divider however does not differ in any fundamental way from that of an edge counter,

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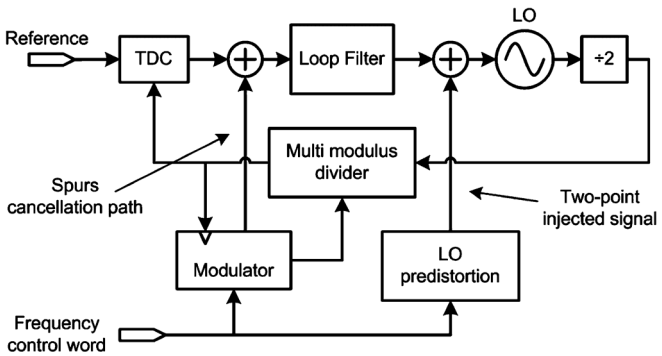


Fig. 1. Fractional-N, two-points modulation ADPLL architecture.

even though some differences on power consumption and synchronous behavior might apply. The comparison between the two digital PLL topologies is further carried out in [3], where the conclusion is reached that for the same TDC and DCO dynamic ranges, the two architectures are completely equivalent when a 1st order $\Sigma\Delta$ modulator is used to drive the fractional-N divider. In this work, we use a first-order $\Sigma\Delta$ modulator to control the fractional-N loop since it requires the smallest range for the TDC. With respect to the D/A position, some solutions implement an analog VCO controlled through a DAC [5], thus shifting the interface at the filter output. Even though conceptually straightforward, this solution maintains the same issues of coupling and sensitivity of an analog PLL and requires a very careful DAC design in terms of noise and supply rejection.

The ADPLL presented in this paper is targeted for a GMSK transmitter using direct phase modulation. As previously mentioned, 2G transmission poses extreme challenges on the DCO phase noise profile. The choice of using a direct modulation path led to a two-point modulation scheme that ideally provides flat phase modulation response no matter which loop bandwidth (BW) is selected. This extra degree of freedom allows the PLL bandwidth to be kept small to achieve low noise and low spurs without implications on the modulation accuracy. In principle this feature can also be leveraged to implement a polar transmitter for non-constant envelope standards (e.g., EDGE or WBCDMA).

As a final remark, it is easily understandable that the overall operation of the ADPLL must rely on multiple calibration loops. The most important one is TDC gain calibration to achieve accurate $\Sigma\Delta$ noise cancellation. Any gain mismatch here translates into possibly large fractional spurs, as it will be explained in Section V. Another important calibration is DCO linearization, as the dither-less DCO used in this PLL [21] exhibits a systematic non-linear characteristic that would make accurate modulation unachievable.

## III. Vernier Time to Digital Converter

The A/D and D/A blocks in an ADPLL set most of its characteristics when compared to an analog PLL. The time-to-digital converter represents one of the key building blocks since its resolution limits the in-band noise, while its linearity sets a lower bound for the level of fractional spurs [4].

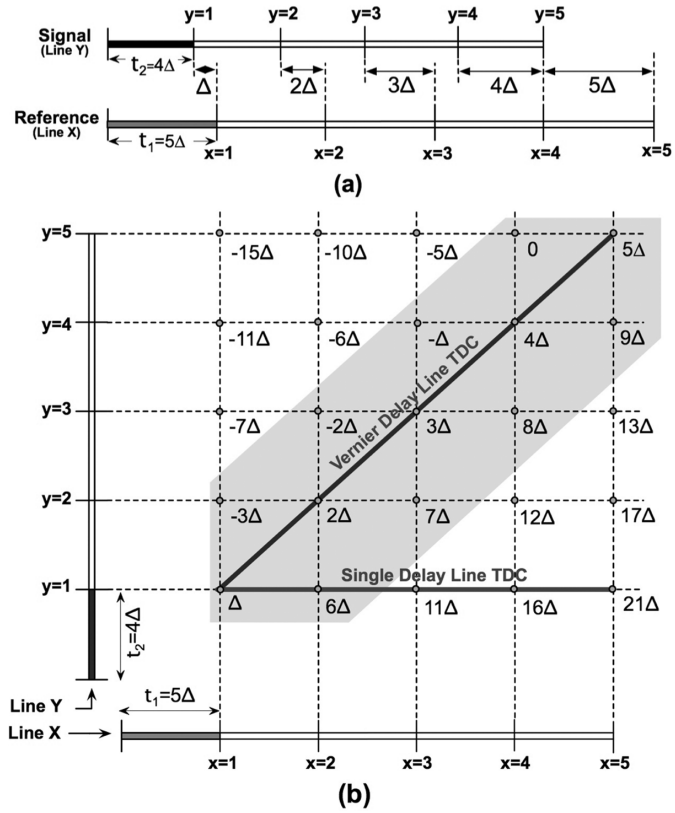


Fig. 2. (a) Linear and (b) 2-dimensional Vernier TDCs.

### A. State of the Art

The resolution of the TDC must be a small fraction of the DCO period to guarantee an acceptable in-band noise. To overcome the limit set by the minimum delay available in the technology, several architectures have been proposed in the literature. Linear Vernier TDCs quantize time differences exploiting the cumulative delay difference of two lines based on elements whose delay is greater than the target resolution [7], [8]. This technique breaks the trade-off between minimum stage delay and TDC resolution, but the number of delay elements grows exponentially with the number of bits limiting the advantages when a large resolution is required. Multi-path approaches [9]–[11] perform interpolation between several parallel delay lines and, as for the linear Vernier, their effectiveness is inversely proportional to the number of delay stages required. A larger number of bits can be obtained adopting more complex architectures directly derived from voltage-to-digital converters. Some examples are the GRO based TDCs [13], [14], that provides a shaped quantization noise like in $\Sigma\Delta$ ADCs, and the two-steps TDC based on a time amplifier [12]. However these approaches are less power efficient for a reduced number of quantization levels where other topologies like flash TDCs become competitive.

### B. From Linear to 2-D Vernier

Linear Vernier TDCs are probably the simplest topology to implement fine resolution converters. However, the large number of delay stages increases the TDC integral non-linearity (INL). In the classic linear Vernier, the time quantization is

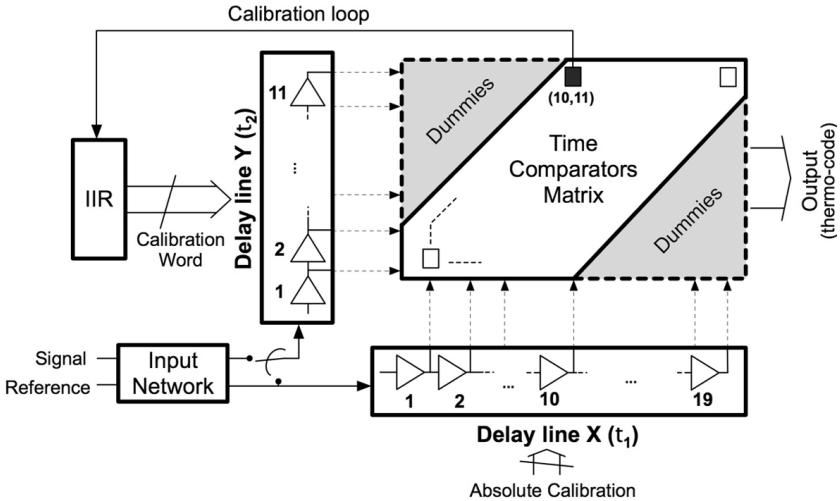


Fig. 3. TDC scheme.

realized by taking time differences only between taps located in the same position of the two delay lines (Fig. 2(a)). Since a delay $\Delta$ is accumulated after each stage, a signal edge that lags a reference edge by $n\Delta$ at the input of the lines will lead it after $n$ stages. Inserting one flip-flop at each stage of the delay line it is possible to produce a digital thermometric code that represents the digitalization of the time difference [7]. This provides uniform quantization with a total of N different codes (N being the number of stages of each delay line), each representing a time step $\Delta$ (the TDC resolution).

When all possible time differences between the taps of the two lines are considered, it is possible to define a plane (named *Vernier plane*) as the one reported in Fig. 2(b) [16]. In this way, starting with two lines with N elements each, $N^2$ quantization levels with the same resolution $\Delta$ are defined. For the same number of bits this approach decreases the number of stages of the delay lines, reducing not only the complexity and the power consumption of the structure, but also the INL compared to linear Vernier [16].

### C. Implementation

The schematic diagram of the realized 2-D Vernier TDC is shown in Fig. 3. The two delay lines define the *Vernier plane* that is completely covered by a matrix of SR latches used as a time comparators. Each latch produces a 1 or a 0 depending if the rising edge of the reference leads or lags the rising edge of the signal [16].

To allow proper operation over process and temperature variations, a background calibration based on a DLL is used to force the correct ratio between the taps of the two delay lines ([16]). In the calibration mode, the reference feeds both lines and the calibration loop adjust the tunable delay elements of line Y (Fig. 3) until the $10\tau_1$ on line X become equal to $11\tau_2$ on line $Y(\tau_1/\tau_2 = 11/10)$. The background operation is achieved since the acquisition and calibration phases are time-interleaved, the former operating on the clock rising edge and the latter on the falling edge. The tuning elements of line X are controlled at the PLL system level defining the TDC gain, as detailed in Section VI.

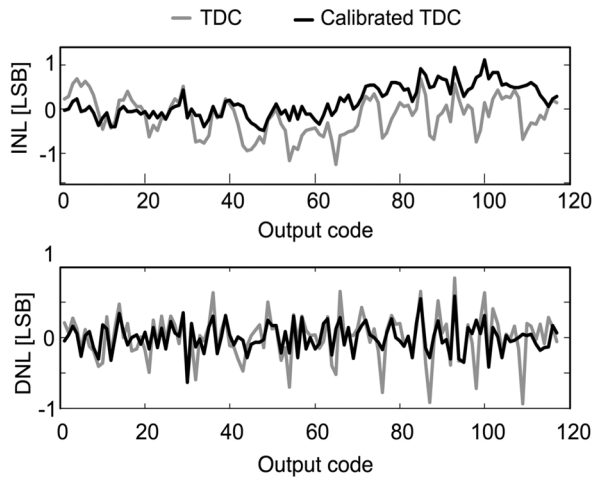


Fig. 4. TDC INL and DNL measurements.

Overall, the TDC is a 7-bit structure with 119 quantization levels. The target resolution of $\Delta = 5$ ps is obtained choosing $\tau_1 = 55$ ps and $\tau_2 = 50$ ps, achieving a full scale of 590 ps, from $-45$ ps to 545 ps. The TDC uses 30 delay elements, 11 for line X and 19 for line Y, much less than a linear Vernier for the same full-scale and resolution (238 delay elements, 119 for each delay line). Having drastically reduced the maximum accumulated delay, it is possible to achieve an un-calibrated INL less than 1 LSB, as shown in Fig. 4.

## IV. Digitally Controlled Oscillator

It is widely recognized that a challenging requirement of GSM TX PLLs is phase noise at 20 MHz offset, which should be below $-165$ dBc/Hz for low bands. Because of this, the reference architecture for the VCO is forced to be an LC tank based one. When a DCO is realized instead of a VCO, an additional quantization noise source is introduced. Quantization noise has to be kept more than 10 dB lower than the analog noise not to degrade the overall phase noise of the oscillator [15]. The unit capacitor that needs to be switched in and out of the LC tank becomes of the order of a few atto-Farads

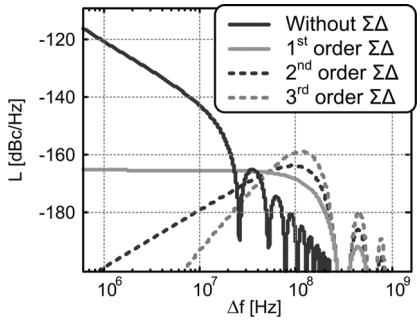


Fig. 5. Quantization noise of the DCO for different dithering techniques.

[17], which is quite difficult to achieve with standard CMOS processes.

### A. DCO State of the Art

A possible solution proposed in the literature is the use of a capacitive divider [18]. This approach potentially improves the DCO frequency resolution but is severely limited by parasitic capacitance. A more reliable solution, proposed by Staszewski et al., leverages dithering, as typically used in $\Sigma\Delta$ DACs [19]. This solution considerably reduces the equivalent DCO frequency resolution (e.g., down to 30 Hz) but moves the quantization noise to higher frequencies where phase noise specs may be even more challenging. Fig. 5 shows the theoretical DCO quantization noise obtained without any dithering and with different dithering techniques (the DCO resolution is assumed to be 64 kHz, the output frequency 2 GHz, the reference frequency 26 MHz, the dithering frequency 312 MHz). The higher the order of the $\Sigma\Delta$ modulation used to dither the DCO control word, the higher the phase noise at high frequency offsets. Due to this problem, the dithering frequency must be very high (a fraction of the DCO frequency) to satisfy the emission mask requirements far away from the carrier, thus increasing the power consumption. Furthermore, retiming of the digital control word is required to minimize the charge injected in the tank while to avoid any additional contribution to the DCO phase noise [20].

### B. Capacitively Degenerated LC-Tank DCO

In this work, we exploit the DCO topology proposed in [21] and reported in Fig. 6. The fine-tuning capacitor bank is moved from the tank to the sources of the two transistors implementing the negative resistance of the LC oscillator exploiting an intrinsic shrinking effect present in the capacitive degeneration of transistors M1–M2. If the value of the capacitance $C$ is much greater than the ratio between the MOS transconductance $g_m$ and the local oscillator (LO) frequency $\omega_{LO}$, the admittance $Y$ appearing in parallel to the tank is

$$Y = -\frac{g_m}{2} - j\omega_{LO} C Q_f^2 \tag{1}$$

where $Q_f = g_m/(2\omega_{LO}C)$.The real part of $Y$ is still the classic negative conductance used to compensate the tank losses, while the reactive part is the tunable capacitance shrunk by the square of its quality factor. For instance, setting $g_m = 10$ mS, $C = 4$ pF and $f_{LO} = 3.2$ GHz, the shrinking factor $1/Q_f^2$ is about 250. This means that a $\Delta C$ of 5 fF at the sources of M1–M2 is equivalent to a capacitor $\Delta C$ of 20 aF directly in parallel to the tank, thus achieving the required resolution without dithering.

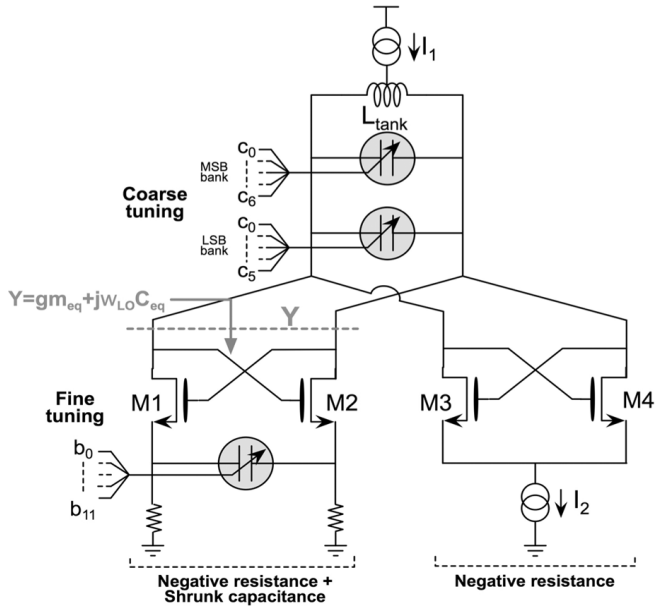


Fig. 6. ADPLL digitally controlled oscillator scheme.

### C. Implementation

The DCO topology in Fig. 6 differs from the original one proposed in [21] as the oscillator is biased through a current generator connected between the voltage supply and the center tap of the tank inductor. Placing the current source between the power supply and the DCO improves the Power Supply Rejection (PSR). This is a very important step to reject noise originating from the voltage regulator (1.5 V) that supplies the oscillator. The current generator $I_1$ biases the whole DCO, while the second generator $I_2$ sets the current $I_1$–$I_2$ that flows in the degenerated switching pair, thereby controlling the transconductance of M1–M2 (defining $Q_f$ and the DCO frequency resolution). It is thus possible to set the DCO gain while minimizing the parasitic capacitive load at the sources of M1–M2 that would limit the fine-tuning range. Moreover, the $I_2$ current source can be designed large enough to minimize the up-converted 1/f noise.

The implemented DCO frequency can be tuned between 5.8 GHz and 8.1 GHz achieving a tuning range of 2.3 GHz (33%). The coarse-tuning of the frequency is achieved acting on two different switched capacitor banks (MSB and LSB banks, which are not controlled by the PLL loop), while the fine-tuning bank placed between the sources M1–M2 is a matrix of $16 \times 16$ varactors, controlled by 12 bits. All the matrix elements except one are digitally switched in and out according to the 8 MSBs so as to generate a thermometric fill of the matrix. The remaining varactor is connected to the output of a 4-bit digital-to-analog converter (DAC) that provides 16 levels between $V_{\rm DD}$ and ground and allows a fine control of the varactor unit.

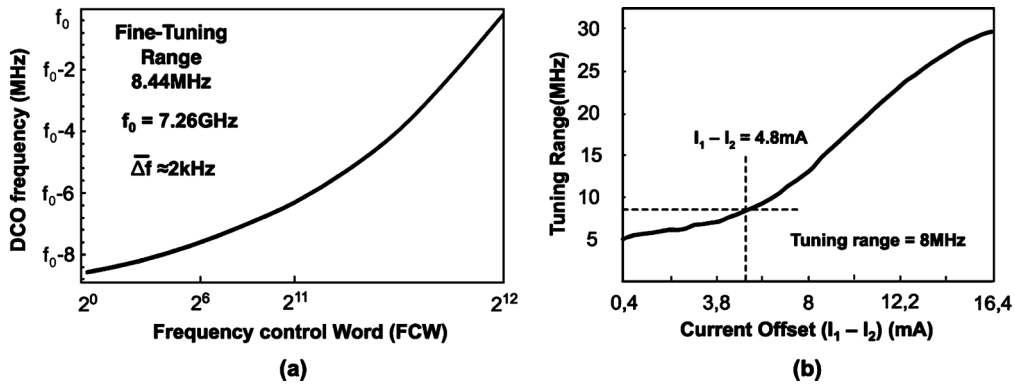


Fig. 7. (a) DCO characteristic, (b) Fine tuning-range vs. I1-I2.

### D. Resolution and Re-Configurability

The current in the degenerated switching pair (i.e., $I_1$–$I_2$) is set to provide a nominal fine-tuning range of 8 MHz (Fig. 7(a) with an average resolution of 2 kHz. The corresponding quantization noise lays more than 10 dB below the intrinsic phase noise of the DCO. Different settings of $I_1$–$I_2$ imply different $g_m$ in (1) thus altering the DCO fine-tuning range, which can be varied between 5 MHz and 30 MHz as reported in Fig. 7(b). The capability to change the shrinking factor allows reusing the same oscillator for different standards that may require the same number of bits but different tuning range and frequency resolution (e.g., GSM and UMTS).

## V. Frequency and Phase Locking Acquisition

The PLL locking process is usually achieved through a two-phase scheme, a first coarse frequency tuning to re-center the LC tank resonance around the target frequency to the requested tuning range and a second finer frequency tuning to obtain the proper phase/frequency locking. Although this last phase is generally performed with the simple activation of the PLL loop, in the presented system some additional issues must be considered. The TDC adopted in this work does not behave as a PFD for locking purposes and its full scale saturates at a DCO period (i.e., 600 ps), covering just 1.6% of the reference period (38 ns). For these reasons, two additional loops are introduced (Fig. 8): a frequency-locked-loop (FLL) to compensate for the PD-only behavior of the TDC and an Edge-Search loop to compensate for the very small linear range of the TDC. Finally, linear locking is accelerated through gear shifting.

### A. AFCAL Calibration

The coarse frequency calibration (AFCAL-Amplitude and Frequency calibration) is performed before activating the PLL. An RF counter is used to measure the DCO output frequency, with a maximum resolution of 120 kHz. While the LC-tank center frequency is being tuned, the DCO bias is trimmed to guarantee proper oscillation amplitude and with it the required phase noise performance. In a typical LC-tank VCO, frequency and amplitude are not orthogonal, so this calibration step requires achieving a fixed-point between amplitude calibration and frequency calibration. Amplitude and frequency calibrations steps are alternated, first the DCO bias current is adjusted to satisfy the amplitude requirements and then a frequency step is taken to increase/decrease the oscillation frequency. The process is iterated until the capacitor unit swapped in/out has negligible effect on the oscillation amplitude. Then, the amplitude loop is frozen and calibration proceeds determining the status of the rest of the capacitor array. In this work we opted for a robust, cold-start locking process that is able to calibrate both amplitude and frequency starting from a powered-down VCO, with the goal of minimizing locking time while maintaining the VCO in safe operating mode (without exposing it so excessive swings that are possible because of the bias tuning range required to cover locking over all PVT corners). The overall calibration time it constrained by the need to allow settling of the analog transients when changing bias levels, and by the RF counter, which is necessarily limited in terms of operating speed. A 2 GHz counter is implemented that operates for several reference cycles to take the frequency measurement error to the required accuracy. Moreover, as a bisection search is performed over the capacitive banks, an error recovery mechanism is required to make the process robust and reliable. In fact, a canonical bisection algorithm cannot compensate for a decision errors made during the bisection process. Any error results in an over-range in the following step, so that the algorithm does not converge with the required accuracy. If the search range is not divided by 2 at each step, but a smaller radix is used, a certain degree of margin is established that allows a (small) decision error not to exceed the next iteration input range, so that the error can be recovered. When compared to canonical bisection, the cost is a small increase of iterations for the same accuracy. As a result, AFCAL requires an average of 42.6 $\mu$s to converge, which even if quite aggressive makes it the largest contributor in the ADPLL locking time. More sophisticated and expensive algorithms can be used to implement faster AFCAL (e.g., LUT based approaches followed by incremental calibrations), but this was out of the scope of this work.

### B. Frequency Locked Loop

The frequency locked loop (FLL) is activated after AFCAL, when the LC tank has been centered and the frequency error is smaller than the fine tuning range of the DCO. The FLL is realized through the RF counter. The counter output is compared to the frequency control word (FCW) and the resulting frequency

TABLE I
ADPLL LOCKING TIME

| | Time duration | | | average fraction of locking time | maximum end time |
|---|---|---|---|---|---|
| | Minimum | **Average** | Maximum | | |
| AFCAL | 42.5 µs | **42.6 µs** | 42.7 µs | 57.7% | 42.7 µs |
| FLL | 2.6 µs | **2.9 µs** | 3.8 µs | 4.0% | 46.5 µs |
| Edge Search | 0.2 µs | **2.4 µs** | 4.7 µs | 3.3% | 50.5 µs |
| PLL WB | 1.3 µs | **5.4 µs** | 9.3 µs | 7.4% | 59.1 µs |
| Gear Shift | 3.5 µs | **3.5 µs** | 3.5 µs | 4.7% | 62.6 µs |
| DCO calibration | 17 µs | **17 µs** | 17 µs | 23.0% | 79.6 µs |

error is fed to the loop filter, which consists of a simple integrator to make the FLL unconditionally stable. The ADPLL stays in FLL mode until the frequency errors falls within the linear range of acquisition of the TDC.

### C. Edge Search Loop

The narrow TDC linear range requires that the divided LO edge and the reference edge are closer than one DCO period from each other to operate linearly, otherwise, the TDC saturates and the loop dynamics become highly non linear and much slower. This problem can be solved keeping the system in FLL mode and controlling the multi-modulus divider to make it swallow LO edges until the TDC enters the linear region. If the divided edge is lagging (leading) the TDC is saturated high (low) and the divider ratio is incremented (decremented) by one until the TDC enters its linear region. The multi-modulus divider does not affect the output frequency as the DCO is controlled by the FLL that senses its output through the RF counter.

A linear search algorithm is implemented in the prototype; this solution is capable of bringing the TDC within its linear region within at most N-1 reference cycles (N being the actual multimodulus divider ratio), depending on the initial phase offset (as shown experimentally in Table I). This can be easily improved with more sophisticated search algorithms, but in this prototype simplicity was given priority, as the overall improvement on locking is not critical.

### D. Phase Locking and Gear Shift

After the Edge Search phase is completed, the FLL is disabled and the PLL is activated with a very large bandwidth. A maximum of 4 gearshift steps can be programmed to achieve the final bandwidth. The first gearshift is triggered as the DCO input variation becomes smaller than a programmable threshold, thus indicating steady state operation. However, the following gearshifts are time triggered to avoid the long observation time required to detect the steady state condition. Gearshift intervals are then chosen according to their respective time constants. The coefficients of the PLL loop filter are changed at each gearshift step, resulting in different transfer functions (the ADPLL bandwidth can be programmed to vary from 1 MHz to 50 kHz). This operation produces perturbations on the settling process that can not be avoided. The state variables of the filter are manipulated to minimize such perturbations as follows. The initial conditions for each step are chosen to enforce output continuity and such that all the derivative terms are zero. The gear shift technique is not only required to speed up the phase lock acquisition process but to ensure reliable locking. In fact, the tiny dynamic range of the TDC (2% of the reference period) represents a severe nonlinearity in the ADPLL loop that may affect locking. Both simulation and measurement results show that if the PLL is activated with narrow bandwidth the locking transient may produce multiple TDC saturation; resulting in an unpredictably long phase locking time.

The overall locking process is reported in Fig. 9 and the relative locking time in Table I. Since the locking procedure is adaptive, it depends on the initial locking conditions, with a variation of 10% over the mean locking time. The greatest part of the locking time is required by the AFCAL, which is the most conservative part of the locking process and whose time duration is almost constant. On the contrary, the FLL, the Edge Search and the PLL WB sections show the highest variability due to the high sensitivity to the initial conditions.

## VI. CALIBRATIONS

Advanced digital features in an ADPLL rely on a seamless interface between analog and digital components. For example, $\Sigma\Delta$ noise cancellation and 2-point modulation require excellent matching between the gain of the analog and the digital paths. Because of analog non-idealities and process spread, it is thus fundamental to perform calibration steps to take the mismatch between analog and digital components below a threshold that allows achieving the performance required to satisfy all the ADPLL specs.

### A. TDC Gain Calibration

The proposed ADPLL architecture is based on the cancellation of $\Sigma\Delta$ noise, whose accuracy is mainly dominated by the gain of the time-to-digital conversion [3]. Therefore we rely on an accurate background calibration scheme to track gain variations. This technique is used in Automatic Gain Control (AGC)

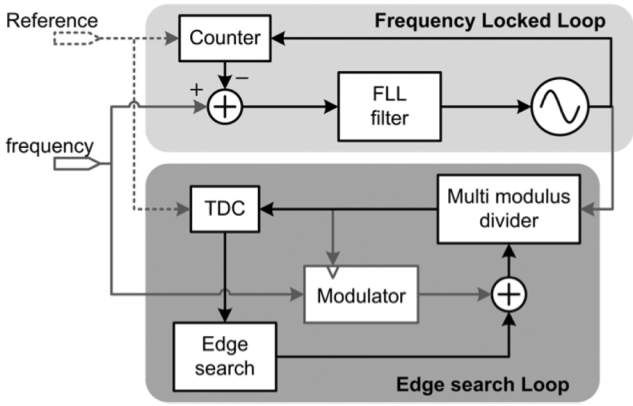


Fig. 8. FLL and edge search loop.

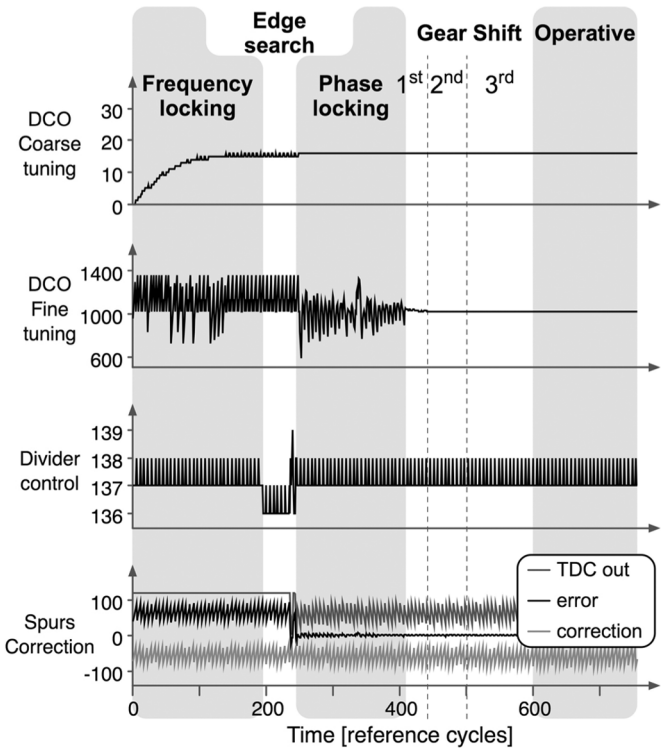


Fig. 9. Frequency -phase locking acquisition.

circuits, where it is known as "Zero-Forcing gain control" [31]. Furthermore this scheme is widely used in ADC calibrations and has already been applied to TDC calibration as well [22]. Background operation is achieved correlating the signal after cancellation with the fractional cancellation signal, as in Fig. 10. The granularity of the gain correction that is applicable to the TDC limits the calibration accuracy. The TDC gain is controllable in the analog domain with 10 ps resolution (1.6% accuracy), therefore the TDC output is further corrected in the digital domain to achieve a finer resolution. The calibration machine implements the necessary logic to merge the analog and the digital paths. Since the TDC gain varies during the calibration settling, the system depicted in Fig. 10 is fundamentally nonlinear. Its nonlinearity is due to the presence of both the variable gain TDC and of the multiplier (correlator). In Appendix I, we provide a simplified theoretical analysis of the calibration loop that shows

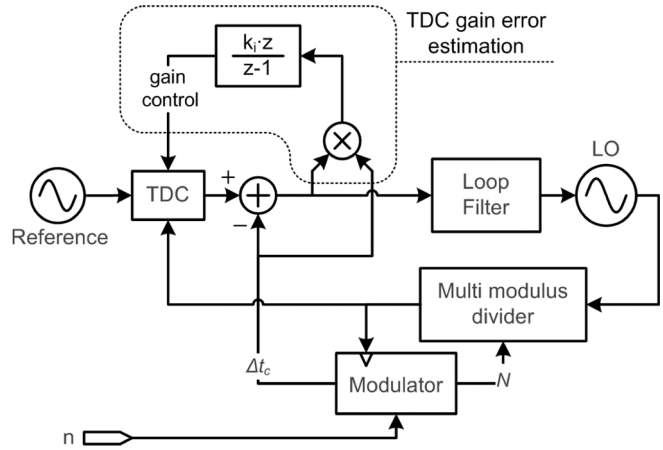


Fig. 10. TDC gain calibration loop.

that the loop stability can be guaranteed only if the spur tones are outside of the PLL bandwidth. Therefore the TDC Gain Calibration loop must be disabled when the fractional spur falls in the band of the PLL.

### B. TDC Linearity Calibration

In a PLL implementing first-order $\Sigma\Delta$ residue cancellation, the TDC linearity has a deep impact on the fractional spurs that are generated in the PLL (as detailed in VII.B). Therefore, TDC linearity has to be corrected to achieve INL well below 1 LSB. Because of this, we perform linearity calibration with a foreground process that is aimed at identifying individual threshold discrepancies and correcting them. Threshold identification is achieved through a histogram method that is borrowed from the ADC literature [23], [24]. Once the actual thresholds have been estimated, the mismatch on the X and Y delay lines are estimated as well. This can be achieved averaging through least squares fitting of the measured thresholds the thresholds obtained in a model that only includes the TDC X and Y inverter line delays. Once the errors in the X and Y delay lines are calculated, each delay element is trimmed to compensate for mismatch effects. The whole process is iterated until convergence is achieved. However this is still a coarse adjustment (Fig. 4). Then, a digital fine correction is further performed, where each individual TDC output code is digitally shifted to maximize the linearity. This operation represents a quantization levels adjustment and quantization thresholds are not affected. The overall linearity is enhanced (as shown by the reduced fractional spurs (Fig. 14)) but the INL (as computed through the standard code density test [25]) can not be calculated because of the non-uniform quantization levels. Because of a digital limitation in the current silicon, the amount of fine correction is limited to 0.5 LSBs which nonetheless provide 5 to 10 dB improvement in the lab on the spurs level, as shown in Fig. 14. Simulation results with 6 bit digital correction indicate a margin of improvement of at least 10 dB, which would take spurs below $-60$ dBc.

### C. DCO Calibration

Wideband two-point modulation relies on accurate DCO gain. In the presented PLL, as shown in Section IV, the DCO

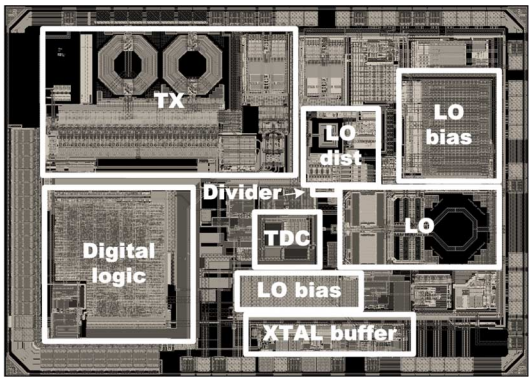


Fig. 11. ADPLL prototype.

fine-tuning characteristic is non-linear. During two-point modulation, the instantaneous frequency deviation is coded as a control word and fed to the DCO assuming a linear relationship. Therefore, it is of uttermost importance to calibrate not only gain, but also non-linearity so as to provide a "nominal" DCO to the modulation engine. We also remark that during modulation the DCO input signal cannot be regarded as a "small" signal since large portion of the DCO input range might be explored.

In all digital PLLs, the DCO gain is generally calibrated with a digital normalization process based on a background algorithm that measures the phase error present in the loop [1]. The same approach could be extended to provide the predistortion of the entire DCO characteristic. However this operation inside the PLL loop is non trivial and would be too expensive in terms of computation. The solution proposed in this paper provides the signal predistortion only on the path that directly drives the DCO (Fig. 1), reducing the computational complexity. This is the only component of the two-points modulation that, acting outside the loop band, is not linearized by the loop.

Polynomial fitting is used for LO predistortion. The higher the degree of the polynomial, the more accurate the approximation is. However, the cost of performing predistortion and of determining its coefficients increases with the polynomial degree. Not only polynomial fitting becomes more cumbersome with increased polynomial order, but also the time required for calibration becomes longer, which generates a more important constraint for the implementation. As a consequence, a second order approximation has been selected for the LO predistortion. Polynomial coefficients can be efficiently computed measuring the DCO control word variations when a given frequency shift is imposed through the sigma-delta modulator; therefore is not compatible with background operations. As shown in Table I, the DCO calibration step adds 17 $\mu$s to the calibration time, resulting in an ADPLL with an off to start time of TX of 79 $\mu$s.

## VII. ADPLL Prototype

The ADPLL prototype, fabricated in 55 nm low power CMOS TSMC process is inserted in a complete transmitter for GSM application (Fig. 11). The entire transmitter occupies an area of 3.5 $\mathrm{mm}^2$ while the total active area reserved to the ADPLL is 0.7 $\mathrm{mm}^2$. The output carrier frequency corresponds to 1.8 GHz/900 MHz after a division by 4/8 of the DCO oscillation frequency. The use of a 7.2 GHz DCO core is motivated at the system level to minimize the pulling with other oscillators when integrated in a full transceiver, at the cost of increased power consumption for a given phase noise performance.

The total power consumption of the frequency synthesizer is 41.6 mW, where 32.5 mW are consumed by the DCO, 5.4 mW by the dividers, 0.75 mW by the TDC and 3 mW by the digital processor.

### A. Phase Noise and ADPLL Transfer Function

In a digital PLL, there are two dominant in-band noise contributors, the phase noise coming from the reference oscillator and the quantization error introduced by the TDC, which can be approximated as white noise [6].

$$PN_{out}(f) = \frac{1}{12}\left(2\pi\frac{\tau_{TDC}}{T_{REF}}\right)^2 \cdot \frac{1}{F_{REF}} \cdot N^2 = \frac{\pi^2}{3}\left(\frac{\tau_{TDC}}{T_{DCO}}\right)^2 \cdot \frac{1}{F_{REF}} \quad (2)$$

With a carrier at 1.8 GHz and the implemented TDC ($\tau_{TDC} = 5$ ps), the expected plateau is $-109.9$ dBc/Hz. At this level, even a reference contribution of $-120$ dBc/Hz increases the overall PN by 0.4 dB. Since inside the PLL band the gain between the reference oscillator phase noise and the PLL output noise is $N^2$, the corresponding reference oscillator phase-noise should be $-156.8$ dBc/Hz, which is a challenging requirement at low offsets ($\sim 100$ kHz). With the on-board GSM-grade crystal, we measured $-106.5$ dBc/Hz in-band phase noise, thus 3.4 dB away from the theoretical value. We repeated the measurement with a more expensive crystal, which we could only obtain for a frequency of 27 MHz. As reported in Fig. 12, the measured PN was $-108.1$ dBc/Hz in band, which is now only 1.9 dB away from the target (the expected PN with a 27 MHz reference is $-110$ dBc/Hz). The measurement was taken with an Agilent E5052B-M1 phase noise meter using a loop bandwidth of 800 kHz. It is possible to note that the reference oscillator is dominant for frequencies lower than 10 kHz. The DCO has a negligible impact at high offsets. Assuming ideal, quantization dominated, TDC noise, we could infer a PN of $-145.9$ (26 MHz reference) and $-149$ dBc/Hz (27 MHz reference) at 100 kHz offset for the reference oscillators [33]. These numbers are compatible with the reference oscillators specs, so the exact TDC contribution to the in-band floor could not be assessed.

In Fig. 13 the ADPLL transfer functions with and without the two-point modulation are reported. When the two-point is activated, the modulation bandwidth is limited by the zero order hold transfer function due to the reference clock of 26 MHz. This curve represents the ultimate limit to the two-point modulation bandwidth. The two-point modulation transfer function is remarkably flat also in the surroundings of the ADPLL bandwidth, where an inaccurate signal injection at the input of the DCO could produce a discontinuity in the signal transfer function. It is worth noting that, although the frequency response of the two-point modulation scheme extends almost to the Nyquist

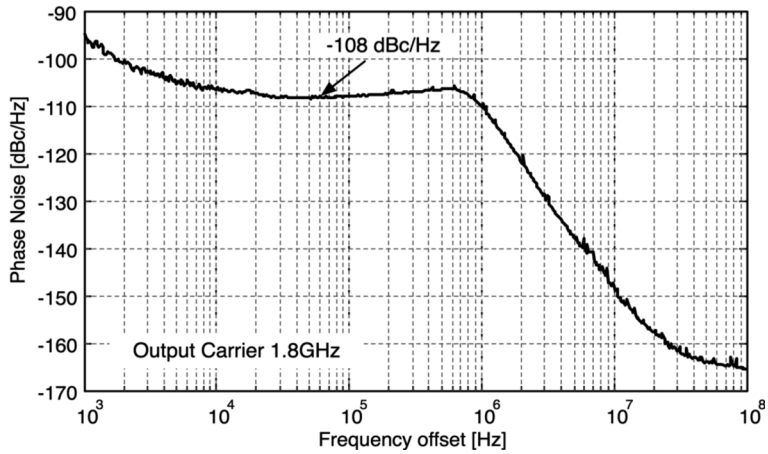


Fig. 12. PLL output phase noise (bandwidth enlarge compared to operative condition).

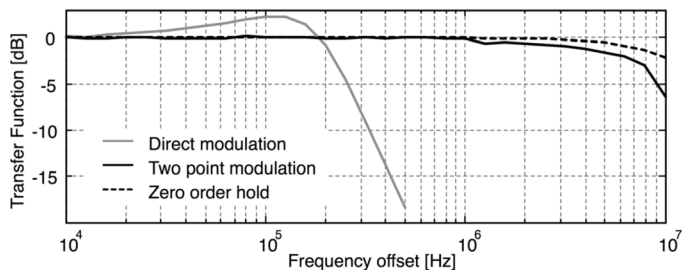


Fig. 13. PLL transfer function. Experimental setup limitation decrease measurement accuracy above 1 MHz.

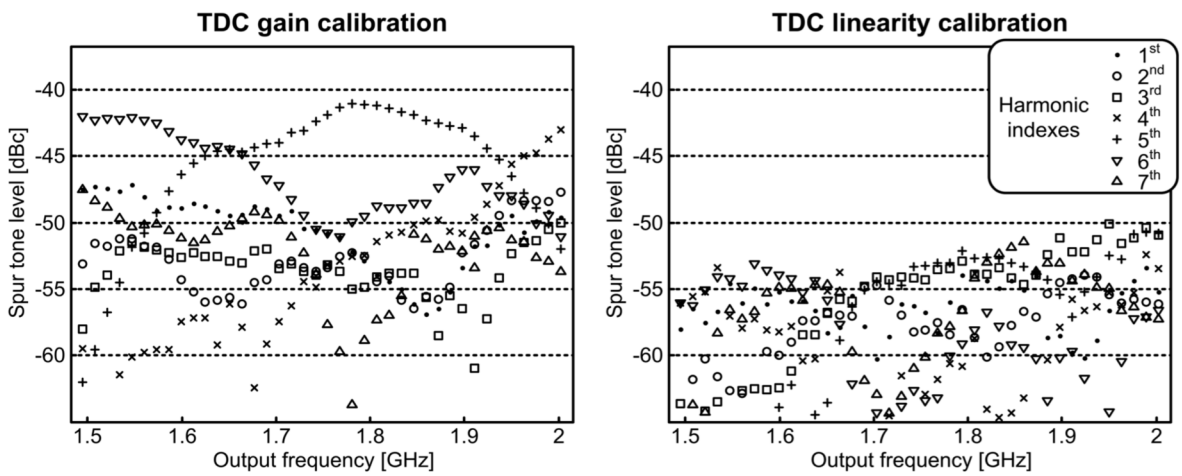


Fig. 14. Fractional spurs.

frequency of the sampled loop, the deployment of wide-band phase modulation needs to comply with the dynamic range of the DCO in terms of instantaneous frequency deviation which is related to fast phase trajectories.

### *B. Spurs*

All fractional-N PLLs are affected by fractional spurs. There are many mechanisms at the origin of fractional spurs, usually related to analog coupling issues. A digital PLL should be less vulnerable to analog couplings, even though the TDC is indeed an analog block at its input ports. However the choice of a first order Sigma Delta modulator with residue cancellation (taken to minimize the required TDC full-scale) limits the spurs suppression [3]. In order to understand the effect of a partial cancellation, we can analyze the consequences of the absence of cancellation. In this case, a saw-tooth residue would appear at the input of the loop filter with amplitude $2\pi$ (in the phase domain (Fig. 15)) and frequency $f_{fract}$ equal to the synthesized fractionality,

$$res(t) = \sum_{k=1}^{\infty} \frac{2}{k} \sin(2\pi k f_{fract} t) \tag{3}$$

If $\mathrm{BW}_{PLL} > f_{frac}$, the spurs appear at the output without attenuation, which means that a 0 dBc fractional spur would

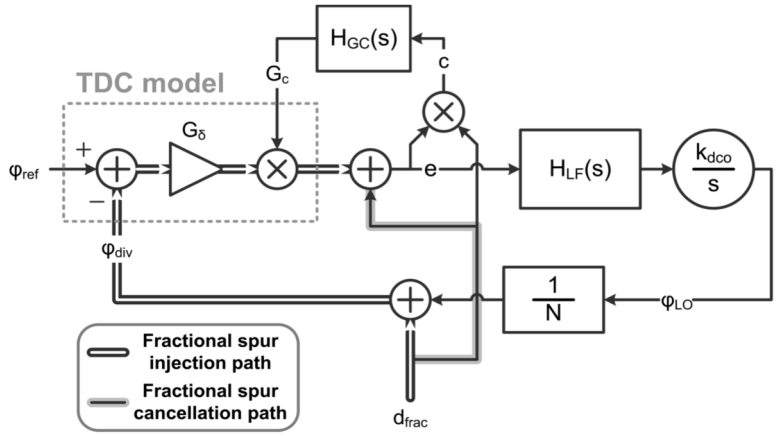


Fig. 15. TDC gain calibration system phase domain model.

TABLE II
SUMMARY RESULTS AND STATE OF THE ART

| | This work | Borremans [34] | Hsu [22] | Tasca [26] | Zanuso [3] | Temporiti [27] | Lee [28] | Pavlovic [29] | Yao [30] |
|---|---|---|---|---|---|---|---|---|---|
| Reference (MHz) | **26** | 40 | 50 | 40 | 40 | 25 | 50 | 48 | 80 |
| Output Carrier Frequency (GHz) | **1,8** | 7,0 | 3,7 | 3,2 | 3,6 | 3,5 | 1,7 | 5,3 | 5,8 |
| Tuning Range | **33%** | 83% | - | 32% | - | 29% | - | 34% | 30% |
| Out-of-band phase noise (dBc/Hz) | **-160@20MHz** | -144@20MHz | -150@20MHz | -121@3MHz | -118.8@10MHz | -123@3MHz | - | -114@1MHz | -133@10MHz |
| Normalized PN at 1.8GHz (dBc/Hz) | **-160@20MHz** | -156@20MHz | -156@20MHz | -126@3MHz | -125@10MHz | -129@3MHz | - | -123.4@1MHz | 143.2@10MHz |
| In-band Noise (dBc/Hz) | **-108** | -90 | -108 | -101 | -104 | -101 | -114 | -97 | -108 |
| TDC power (mW) | **0,75** | 1,8 | 3,5 | - | - | - | 70 | - | - |
| Max PLL Bandwidth (MHz) | **3** | 2 | 0,5 | 0,3 | 3,2 | 3,4 | 0,8 | - | 0,5 |
| In-band spurs (dBc) | **-50** | - | -42 | -42 | -57 | -58 | -48 | -45 | -70 |
| Power Dissipation (mW) | **41,6** | 30 | 39 | 4,5 | 80 | 9 | 121 | 20 | 36 |
| Area ($mm^2$) | **0,7** | 0,3 | 0,9 | 0,2 | 0,4 | 0,4 | 2,3 | 1,3 | 0,7 |
| Process (nm) | **55** | 40 | 130 | 65 | 65 | 65 | 90 | 65 | 55 |

appear.[1]Residue cancellation relies on the accuracy of the TDC gain compensation. If we assume the nominal TDC gain to be 1 and the compensated gain to be $(1-\delta_{gain})$, we get

$$res_{canc}(t) = \delta_{gain} \sum_{k=1}^{\infty} \frac{2}{k} \sin(2\pi k f_{frac} t) \tag{4}$$

Therefore, we need to compensate TDC gain to a precision of 0.1% if we want to keep fractional spurs below $-60$ dBc. TDC non linearity makes the picture even worse, as $res_{canc}(t)$ goes through a non-linear block. If we assume a polynomial non-linearity, the amplitude of harmonics is affected but not their frequencies. However, since the PLL is sampled at the reference frequency $f_{REF}$, higher harmonics of $res_{canc}(t)$ are folded in-band. For this reason, the evaluation of the worst spur cannot be limited to $f_{frac}$, but must considered all the harmonics that compose $res_{canc}(t)$.

We measured fractional spurs for $f_{frac}$ well within the PLL bandwidth so that a significant number of harmonics could be evaluated without any attenuation. Fig. 14 reports results as a function of the carrier frequency, taking the first seven harmonics. The measurement results are reported for the entire tuning range of the DCO. The TDC gain calibration algorithm resulted in a $-41$ dBc worst-case spurs level while a worst-case spur level of $-50$ dBc was obtained after linearity calibration was included. The total spur power depends on the number of spur harmonics falling in band, which is 2.2 dB larger than the fundamental power in the asymptotic case that all spurs fall in band without non-linear distortion. As a final consideration, we note that the use of higher order $\Sigma\Delta$ modulators would remove this spur generation mechanism at the expense of increased TDC complexity. Alternatively, the insertion of a dithering sequence at the $\Sigma\Delta$ modulator level, with consequent digital cancellation, would whiten the residue sequence. The same idea could be applied in an analog manner on the reference clock and once more digitally cancelled, with the same consequence of whitening the residue signal [4].

[1]Actually the spur is even higher since the narrow-band frequency modulation approximation can not be applied.

### C. State of the Art Comparison

The main characteristics of the proposed ADPLL are summarized in Table II and compared with state of the art digital frequency synthesizers. For a fair comparison, the out-of-band phase noise should be normalized to the output carrier frequency while the in-band noise also to the reference frequency. After the proper normalization, the presented ADPLL shows the lowest out-of-band phase noise i.e., $-160$ dBc/Hz at a frequency offset of 20 MHz. In this case, the major contribution comes from the DCO and depends mainly on the analog noise sources since the digital quantization noise has been minimized adopting the dither-less architecture presented.

The ultimate limit for the in-band phase noise is the quantization introduced by the TDC and the reference oscillator. In this case the solution proposed shows one of the best compromise between in-band phase-noise and TDC power consumption (Table II). Although the solution proposed by Lee *et al.* reaches

the lowest in-band phase noise ever reported ($-114$ dBc/Hz for a reference of 50 MHz), this outstanding performance is paid consuming up to 70 mW. On the contrary, thanks to the 2-dimensional Vernier TDC, the proposed ADPLL shows an in-band phase noise of $-108$ dBc/Hz consuming just 0.75 mW. Similar performances are obtained also by the GRO-based ADPLL proposed by Hsu, but also in this case the power consumption in much higher (3.5 mW).

## VIII. Conclusions

In this paper a high performance ADPLL for cellular transmitters has been presented. It combines the noise performance of the best analog PLLs with the flexibility of digital circuits, allowing wideband two-point modulation and fast locking, meeting the demanding 2G TX requirements. Measurements and FoM classification confirm the soundness of the proposed solution.

## Appendix
## Calibration Loop Stability

Both measurement and simulation results show that the TDC gain calibration loop becomes unstable when the fractional spurs fall within the PLL bandwidth. The aim of this appendix is to derive an intuitive theoretical explanation of this phenomenon based on the analysis proposed in [31] for the "Zero-Forcing gain control" technique.

The TDC gain error calibration loop is embedded in the PLL loop and interacts with it (Fig. 15). The system is non trivial to analyze since the TDC loop is non-linear. While there is no rigorous meaning in defining a TDC gain calibration loop bandwidth, it is intuitive to model it as a low-pass loop that needs to compensate DC gain variations and therefore is very slow compared with the PLL dynamics. Because of this, if we assume the system to be in steady state, the analysis of the PLL loop can be carried out assuming the TDC gain calibration is steady and constant, thus effectively opening its loop.

During normal operation, the phase error $\varphi_{ref} - \varphi_{div}$ caused by the first order $\Sigma\Delta$ modulator can be represented as a saw-tooth signal with frequency $f_{frac}$ and amplitude $2\pi$ that we label $d_{frac}(t)$. The same signal is digitally subtracted at the output of the TDC (after proper scaling); therefore we can define a residue $r(t)$

$$r(t) = d_{frac}(t)(G_\delta G_c - 1) \tag{5}$$

that is equivalent to $d_{frac}(t)$ once injected at the loop filter input. $G_\delta$ is the ratio between the actual TDC gain and its nominal value, and $G_c$ is the applied gain correction factor. Because of the previous assumption on the interaction between the loops, the transfer function between $r(t)$ and $e(t)$, at the loop filter input, is

$$H_e(s) = \frac{e(s)}{r(s)} = \frac{1}{1 + G_{loop}(s)} \tag{6}$$

where $G_{loop}(s)$ is the PLL open loop transfer function. The phase error $e(t)$ can then be expressed as:

$$\begin{aligned} e(t) &= r(t) * h_e(t) \\ &= (G_\delta G_c - 1) \sum_{k=1}^{\infty} a_k \\ &\quad \cdot \sin(k\omega_{frac} t + \angle H_e(jk\omega_{frac}) + \varphi_k) \\ &\quad \cdot \mid H_e(jk\omega_{frac}) \mid \end{aligned} \tag{7}$$

where $a_k$ and $\varphi_k$ are the coefficients of the series expansion of the saw-tooth signal $d_{frac}(t)$. The analysis of the correlator output $c(t)$ becomes cumbersome in general terms. If we restrict it to the first order harmonics of $e(t)$ and $d_{frac}(t)$, we obtain

$$\begin{aligned} c(t) &= d(f) \cdot e(t) \\ &= \frac{\mid H_e(j\omega_{frac}) \mid \cdot a_1^2 \cdot (G_\delta G_c - 1)}{2} (\cos(\angle H_e(j\omega_{frac})) \\ &\quad - \cos(2(\omega_{frac} t + \phi_1) + \angle H_e(j\omega_{frac}))) \end{aligned} \tag{8}$$

Assuming the calibration loop filter to be an integrator (with gain $k_i$), we can neglect the term at $2\omega_{frac}$ and obtain the following equation for the gain correction loop output

$$\begin{aligned} G_c(t) = \frac{k_i \cdot \mid H_e(j\omega_{frac}) \mid \cdot a_1^2 \cdot G_\delta \cdot \cos(\angle H_e(j\omega_{frac}))}{2} \\ \times \int_{\infty}^{t} \left( G_c(x) - \frac{1}{G_\delta} \right) dx \end{aligned} \tag{9}$$

Equation (9) represents a first order feedback system that is stable only if the multiplying coefficient is negative. When $\omega_{frac}$ is higher than the PLL bandwidth the dependency on $H_e(s)$ can be neglected, as it is a high-pass function. The dynamic response of $G_c(t)$ is dependent on $G_\delta$, resulting in a slow settling if $G_\delta$ is low and a fast settling if $G_\delta$ is high. In our design the PVT spread of $G_\delta$ is limited so the speed of convergence is not heavily affected. If this were not the case, an exponential gain control technique can be applied as in [31], [32]. When $\omega_{frac}$ becomes lower than the PLL bandwidth, the attenuation due to $|H_e(j\omega_{frac})|$ slows down the dynamics of the calibration loop. The term $cos(\angle H_e(j\omega_{frac}))$ further reduces the speed of the loop when $\angle H_e(j\omega_{frac})$ approaches 90°. Furthermore, in a PLL of order higher than one, $\angle H_e(j\omega_{frac})$ exceeds 90° as $\omega_{frac}$ becomes smaller, resulting in a sign change of the loop which becomes unstable. This analysis, which is based on simplified assumption, is nonetheless confirmed by both simulation and measurements. As a result, since the TDC gain does not depend on $\omega_{frac}$, we need to calibrate the TDC gain when $\omega_{frac}$ is outside the PLL bandwidth, and disable the loop when it falls inside.

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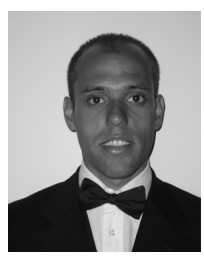

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