A 90nm CMOS Gated-Ring-Oscillator-Based 2-Dimension Vernier Time-to-Digital Converter

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***Abstract*—Two branches of gated ring oscillators (GRO) act as the delay lines in 2-dimension Vernier time-to-digital converter (TDC). The proposed architecture reduces dramatically the inherent latency of vernier structure. The already small quantization noise of the standard Vernier TDC is further first-order shaped by the GRO operation. The TDC has been simulated in 90nm CMOS technology. Operating from 50MHz reference frequency, it achieves a resolution better than 2ps assuming a signal bandwidth of 1.56MHz (OSR=16), for a minimum current consumption of 1.8mA from 1.2V.**

I. Introduction

Time-to-digital converters have been a hot research topic over a few years. They support the industry trend of replacing analog/mixed signal by digital realizations. High-resolution TDCs have obtained more and more popularity due to their increasing implementation in digital PLL, ADCs, jitter measurement and time-of-flight measurement units. However, the time resolution provided by self-loaded inverters does not always satisfy the requirements, and thus different kinds of solution based on Vernier algorithm and noise-shaping were investigated.

A classic Vernier TDC improves the time resolution by using two delay lines with different inverter delays [1]. The effective time resolution is given by the difference of two delays, which can be designed much smaller than a single inverter delay. However, in traditional Vernier architecture, the number of stages grows exponentially with the number of bits and it results in grows in sensitivity to device mismatch. A modified 2-dimension Vernier approach is implemented to reduce significantly the length of delay lines for a given full scale [2].

Noise shaping technique is another method for increasing effective TDC resolution [3]. In a GRO TDC, each new measurement starts with the ending voltages of the last measurement (by charge holding), rather than discarding them. Thus both the delay mismatches and quantization error experience the first order noise shaping, leading to an improvement of effective resolution and linearity. Considering that raw resolution in GRO-based TDC is still limited by an inverter delay, a GRO-based Vernier TDC combining the Vernier approach with GRO TDC is implemented [4]. Two delay lines in linear Vernier architecture are replaced by two GROs, which can achieve both a high raw resolution and a first-order frequency shaping of the quantization noise. However, as the same with other linear Vernier structures, the long latency limits the detection range and highest sampling frequency of TDC [5].

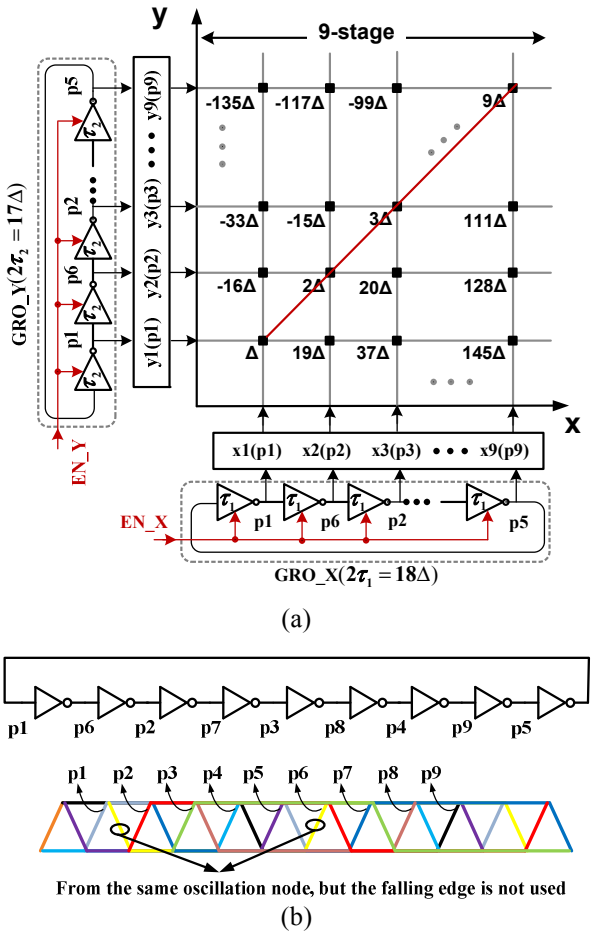

Fig. 1 (a) Proposed GRO-based 2-D Vernier TDC and (b) phase sequence in delay line

The proposed TDC in this paper combines the 2-dimension Vernier approach with GRO manner, i.e., the two delay lines in 2-dimension TDC are replaced by two GROs. Unlike previous GRO-based Vernier TDC [4], the scheme of 2-dimension Vernier structure not only achieves a very low time quantization beyond the inverter delay but also reduces dramatically the output latency time and extends the detection range of TDC for a given sampling frequency.

An overview of the paper is as follows. Section II describes the proposed the GRO-based 2-dimension Vernier TDC. Section III details the circuit implementation. Section IV gives the simulation results. Conclusions are drawn in Section V.

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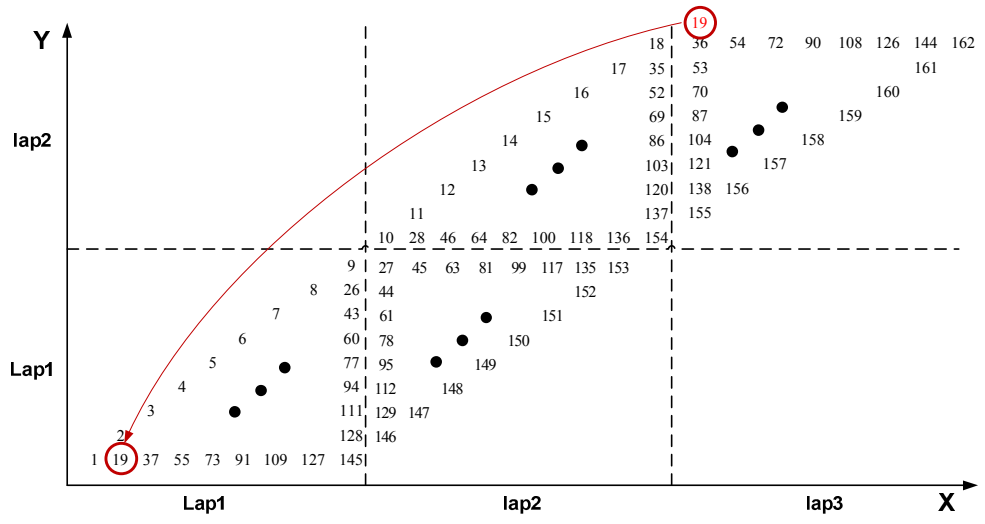


Fig. 2 Two-dimension Vernier plane of proposed TDC

II. GRO-BASED 2-DIMENSION VERNIER TDC

A. *Principle of 2-dimension Vernier*

To explain the concept of the proposed GRO-based 2-dimension TDC, Fig. 1(a) illustrates a Vernier-plane that is composed of a 9-stage slow-delay GRO and a 9-stage fast-delay GRO, with the inverter delay time τ_1 and τ_2, respectively. It should be noted that only the rising edge of GRO phases is used in sampling block, in order to avoid the mismatch between rise time and fall time of the inverter. That means, the Vernier time resolution (raw resolution of TDC) is equal to twice the difference between SGRO inverter delay and FGRO inverter delay, as shown in Fig. 1(b).

The plane XY is arranged into a vector to obtain an ordered set of time references with a constant quantization step Δ (i.e., the raw resolution of TDC). The slow GRO (SGRO) is first started by *EN_X,* so that the fast GRO (FGRO, started by *EN_Y*) can catch up with it in Vernier-like fashion. As shown in Fig. 1(a), the operation of Vernier plane is performed by a function $i = i(x, y) \in \mathbb{N}$, which associates the position i in the vector with the coordinates (x, y). It is noted that the values of x and y are limited between 1 and 9 due to the ring operation of GROs. For convenience, let us first consider x and y with an infinite range, so that

$$i \cdot \Delta = X_{abs} \cdot 2\tau_1 - Y_{abs} \cdot 2\tau_2 \tag{1}$$

$$i = X_{abs} \cdot k - Y_{abs} \cdot (k-1) \tag{2}$$

Where X_{abs} and Y_{abs} represent the absolute taps of SGRO and FGRO delay, respectively. A particular set of 2-D Vernier plane is given in equation (2), $2\tau_1 = k \cdot \Delta = 18\Delta$, $2\tau_2 = (k-1) \cdot \Delta = 17\Delta$. According to [2], the equation (2) can be inverted obtaining

$$\begin{cases} X_{abs}(i) = i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot (k-1) \\ Y_{abs}(i) = i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot k \end{cases} \tag{3}$$

Where $\lfloor a \rfloor$ is the inferior integer of a. Then, considering the ring operation of 9-stage GRO, the modular operation is introduced, as modified in (4).

$$\begin{cases} X(i) = \mathrm{mod}\{X_{abs}(i), 9\} \\ \qquad = \mathrm{mod}\{i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot (k-1), 9\} \\ Y(i) = \mathrm{mod}\{Y_{abs}(i), 9\} \\ \qquad = \mathrm{mod}\{i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot k, 9\} \end{cases} \tag{4}$$

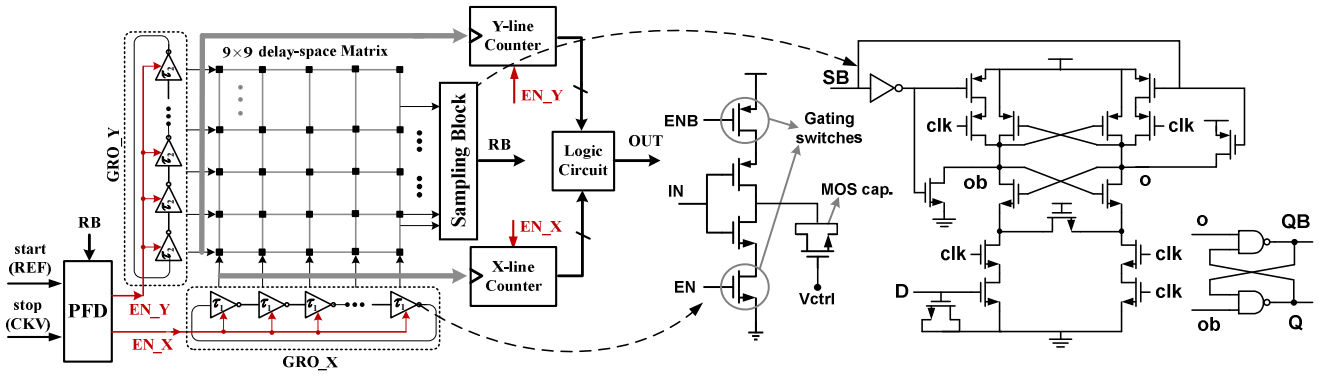
As mentioned in [2], $Y_{abs}(i)$ is periodic and limited between *0* and *k*. It is possible to verify that the *Y(i)* is also periodic if *k=18* (the multiply times of mod operator, 9), as shown in Fig. 2. From (4) and Fig.2, we can see the same coordinate *(x,y)* may correspond different delays (e.g *(x,y)=(9,9)* maps to 9, 18……), which depends on how many laps the GROs have run. The number of laps, combining a coordinator *(x,y)* determines the TDC output. It is the same with the 3-D Vernier Ring TDC [6].

An important challenge in the 2-D Vernier GRO TDC is that each measurement starts from a different SGRO/FGRO delay-cell pair, rather than always from the first pair as in a normal Vernier TDC. For example, as shown in Fig.2, if the measurement starts from *(3,2)* and stop at *(5,3)*, the counter will give the relative coordinate *(2,1)*. Then the next measurement will start from *(5,3)* rather than the origin *(0,0)*.

Equation (4) also implies that the Vernier plane can be mapped into a set of time reference with a constant quantization step Δ. In our case, all the positions in the 9×9 matrix are used and continuous nature numbers (TDC output) can be given. For only 3 SGRO (X-axis) laps (~2.4ns latency), the proposed TDC could cover more than $\pm$800ps without intervals. In [2] and [6], only partial matrix positions are utilized, which actually wastes some detection range.

B. *Principle of GRO operation*

Two GROs are implemented as the delay lines in Vernier plane, as shown in Fig.1. During the operation of



(a) (b) (c)

Fig. 3 GRO based 2-D Vernier TDC implementation: (a) top scheme (b) delay cell in GRO (c) D-flip flop

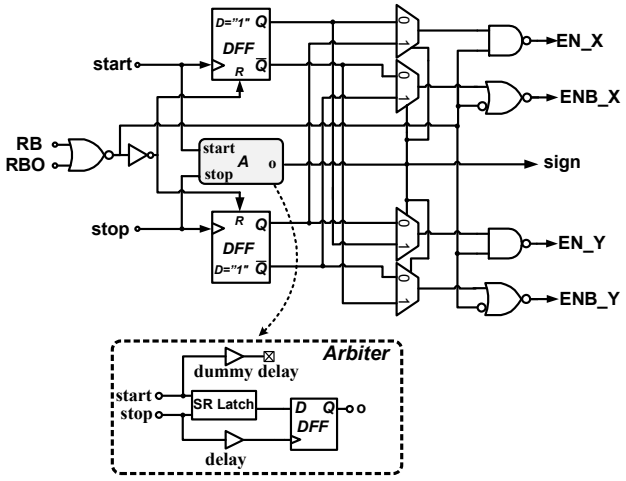


Fig. 4 Adaptive phase-frequency detector

TDC, when FGRO catches up with SGRO, the state of both GROs is frozen by falling *EN_X/EN_Y*. The capacitor at each node in SGRO/FGRO holds now the voltage value at the freezing instant, and during the next measurement cycle, each GRO starts from this state. In this way, the quantization error is accumulated across all measurement, resulting in the first-order shaping.

III. Circuit Implementation

Fig.3(a) shows the structure of the proposed TDC. It includes the core of TDC, the phase frequency detector (PFD), and two multi-phase counters. The PFD senses the time difference between two inputs *start* and *stop* and generates two enable pluses *EN_X* and *EN_Y* controlling the gating switches in GRO_X and GRO_Y, respectively. The quantized delay generated by the two GROs is then read out by the two multi-phase counters. The logic circuit, which combines the outputs of two counters, is used to map the coordinate *(x, y)* to the delay value.

A. TDC Core

The core of the TDC is constituted by the two GROs and the matrix of comparators. To obtain a high Vernier time resolution, two identical 9-stage ring oscillators with different frequency controls are used in TDC core. As shown in Fig. 3(b), in each delay cell, the loading MOS capacitor controls the oscillation frequency. For SGRO, the loading capacitance is larger than that of FGRO, which results in lower oscillation frequency, that is, long delay time. Additionally, the oscillation frequency of SGRO is tuned by the *Vctrl*, which is in the analog manner.

The sampling block (9×9 D flip-flop matrix in the Vernier plane) determines when FGRO catches up with SGRO. For a high-resolution TDC, a narrow metastability region is necessary. As shown in Fig.3(c), a modified sense amplifier-based flip-flop is adopted [7]. The path delays are matched by reordering data and clock ports in pull-down paths and adding a dummy capacitor to the data to balance the input loading. The flip-flop eliminates the big mismatch between D-to-Q and CLK-to-Q delays, which appears as a large time offset in the comparator (flip-flop). By using this new flip-flop (replacing SR latch + D flip-flops in [4]), the TDC detection range is improved greatly and not limited by GRO core.

B. Phase frequency detector

In order to guarantee the *EN_X* always leads *EN_Y* the adaptive phase frequency detector (PFD) of Fig. 4 is used [4]. It generates an *EN_X* always leading *EN_Y* regardless the phase relation between *start* and *stop*. The PFD makes use of two true-single-phase-clock flip-flops having an always-high internal "D" input, and of an SR latch used as an arbiter. The arbiter senses the leading edge between *start* and *stop*, and generates a *sign* signal controlling four multiplexers. When *start* is leading, *EN_X* corresponds to *start*, while when *stop* is leading, *EN_Y* corresponds to *stop*. A *sign* signal can be sent out for a DPLL application indicating a positive or negative phase error.

C. Multi-phase counter

In contrast to the structure in [4], the multi-phase counter in Fig.5 assigns an individual accumulator to each phase, since the delay difference between neighboring phases is very short, i.e. 90ps. The number of delay cells used by the GROs during the measurement is counted by a multi-phase counter clocked by all staggered phases from the SGRO and FGRO. An enable pulse allows an accumulator to be triggered by the rising edge of the SGRO phases; at the falling edge of the enable, the counter saves the result and resets the accumulator waiting for the next measurement.

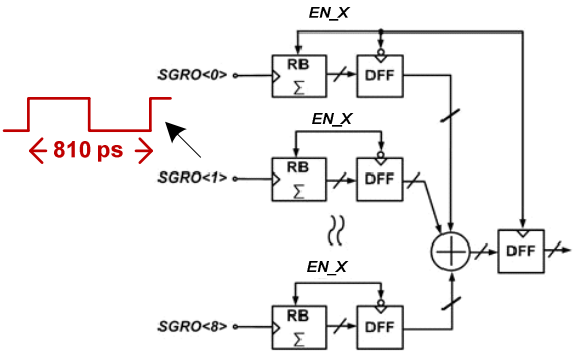


Fig.5 Multi-phase counter

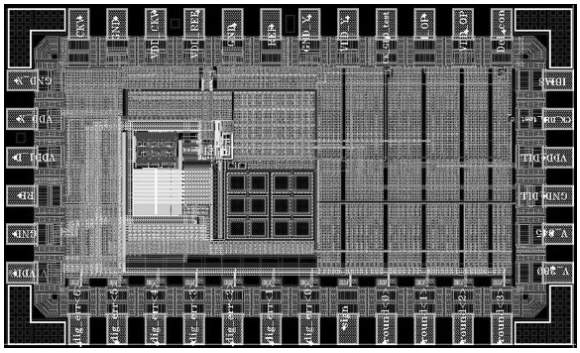


Fig.6 Layout of proposed TDC

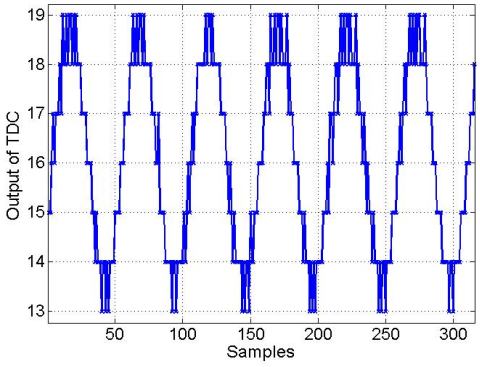


Fig.7 Transient simulation of TDC output

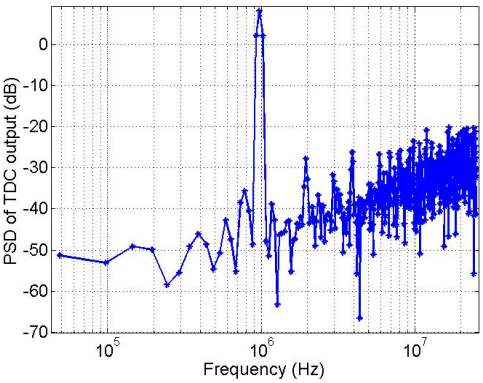


Fig.8 Simulated TDC output PSD with sin-input

IV. Simulation Results

The GRO based 2-dimension Vernier TDC has been implemented in 90nm standard CMOS process. Fig. 6 shows the complete layout, where the active area is 0.22mm·0.20mm.

The transient simulation in Fig.7 is obtained when the delay between *start* and *stop* varies sinusoidally in time with a frequency of approx. 3.9MHz. A 50MHz reference (sampling) clock is used. SGRO has the unit delay of 90ps (18Δ) and FGRO has 85ps (17Δ). The raw resolution is 5ps(Δ).

Fig. 8 illustrates the FFT analysis of Fig.7. It can be seen that the sinusoidal input results in a quantization noise shaping following the expected first-order 20dB/decade slope. The calculated SNR from Fig. 8 is approx. 39dB with an oversampling ratio (OSR) of 16. To achieve the same SNR with the same OSR but assuming a white noise PSD, the equivalent TDC resolution is 1.9ps, which is clearly below the Vernier delay of 5ps.

V. Conclusions

We have presented a GRO based 2-dimension Vernier TDC that makes use of two gated-ring oscillators (GRO) instead of two delay lines in a 2-dimention fashion. The TDC displays a first-order shaping of the quantization noise, improving the already good Vernier time resolution. It achieves ±800ps detection range, with only 2.4ns latency time. Working with 50MHz sampling frequency, the TDC consumes a minimum current of 1.8mA.

VI. References

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