5.1 SAW-Less Analog Front-End Receivers for TDD and FDD

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In cellular receivers, out-of-band blockers are generally managed by surface-acoustic-wave (SAW) filters between the antenna and the low-noise amplifier (LNA). For Time Division Duplexing (TDD), such as GSM, the SAW can be removed if the receiver can handle very large interferers (e.g. in GSM 0dBm 20 MHz away) [1]. Generally SAW filters also perform differential to single-ended (SE) conversion (balun). Once the SAW is removed an SE transceiver eliminates the external balun, reducing cost and attenuation. For the same sensitivity, a SAW-less SE transceiver can have a noise figure (NF) 2 to 3dB higher than a classical one. An SE LNA could be susceptable to couplings from supply and substrate, which are usually rejected through symmetry. Therefore it should become symmetric as closely as possible to the input pin. A SAW-less differential transceiver [2] can also be appealing if it has an NF close to that of classical transceivers. This is because it can have better sensitivity in TDD (a balun attenuates less than a SAW) and it can be very flexible, being usable for both FDD (where duplexers are differential) and TDD.

The two receiver chains reported in Fig. 5.1.1 address these issues. High linearity is obtained for both SE and differential inputs through a transformer-based blocker-tolerant LNA and a TIA with a second-order filter able to handle large downconverted interferers. Harmonic rejection at the 3rd and at the 5th harmonic of the local oscillator (LO) is improved by inserting notches in the LNA and/or mixer transfer functions. Finally a low-power, low phase noise divider, with an intrinsic 25% duty-cycle output generates the four phases for the quadrature downconversion.

The two LNAs are reported in Fig. 5.1.2. The active portion of both is a fully differential complementary Class A/B common gate. The PMOS and NMOS transistors are coupled to the input by two secondary coils of an integrated transformer that swing below ground and above the supply. In the SE case, the transformer is also a balun. This gives to the SE LNA immunity from spurious coupling close to that of the differential circuit. The secondary coils have fewer turns than the primary giving 6dB and 9.5dB current gain for SE and differential respectively. To reduce the NF of a classic common gate, the gate-source voltage of the input transistors (M1-M4) is boosted. In the SE LNA (Fig. 5.1.2.a) this is done by a fourth coil with a k of 1, while in the differential LNA (Fig. 5.1.2.b) by a capacitive feed-forward from the input. In the case of the SE LNA, two feed-forward capacitances (CF) implement a zero at $3f_{LO}$ to attenuate the blockers downconverted in-band through harmonic mixing.

A passive current mixer is ac-coupled to the LNA (Fig. 5.1.3). It includes an LC tank resonating at $4f_{LO}$ in series with the input of the base band (BB) to improve harmonic rejection. At RF, due to the bilateral gain of the passive mixer, the resonant frequency of the LC tank appears upconverted and downconverted to $5f_{LO}$ and $3f_{LO}$ respectively. This gives increased impedance at the mixer input at these frequencies that, combined with the parasitic capacitances at the LNA output, produces two frequency notches in the mixer gain. Contrary to RF filters, this technique does not increase the parasitic capacitance at the output of the LNA that affects both mixer and BB noise. As a consequence there is no noise/gain penalty. Actually, the frequency notches also reduce the in-band noise folding, improving NF. The resonant frequency of the tank can be moved around $4f_{LO}$ (by adding extra capacitance), to verify its effectiveness.

The four clock phases used to drive the I and Q mixers are generated directly by a divider able to create 25% duty-cycle signals from a differential externally supplied clock at $2f_{LO}$ (Fig. 5.1.4.a). The divider is derived from the circuit proposed by Razavi [3]. The generation of 25% duty-cycle outputs relies on the particular latch (Fig. 5.1.4.b). When the latch senses the input signal (M1-M2 are OFF) both outputs are high (one pulled up by the input and the other maintaining the high state from the previous cycle) since the NMOS pull-down devices are OFF [3]. This asymmetry in the latch response gives the 25% duty-cycle output. Compared to the original design [3], transistor pair M5-M6 has been inserted in series to M1-M2 to avoid static power dissipation when M1-M2 are ON and either of the two inputs is low. The divider gives a quadrature 25% duty-cycle clock with -174dBc/Hz phase noise at 20MHz offset for 6mA of current consumption (simulated from extracted layout).

The BB is made-up by a re-configurable TIA (Fig. 5.1.1), implementing a second order filter, whose topology was derived from [4]. While most TIAs in the literature implement only real poles [2], our TIA has two conjugates poles, making it better suited to handle large blockers with a flat response. The BB follows the system consideration reported in [4] to be compliant with GMS (SE LNA) and UMTS (differential LNA). For GSM the receiver gain is 47dB and the cutoff frequency is 1.4MHz while for UMTS they are 45dB and 3.4MHz respectively.

A chip prototype with the two receivers was fabricated in 40nm CMOS. For TDD S_{11} is below -14dB from 1.6 to 2.8GHz. For FDD an error in the PCB unbalances the hybrid coupler that feeds the differential signal and S_{11} is better than -10dB only between 1.8 and 2.1GHz. Figures 5.1.5.a-b show the NF and the gain for both receivers vs. frequency. For FDD we have shown NF only in the range between 1.8 and 2.1GHz again because we cannot feed a good signal over a wider range. Minimum NFs of 3.8 and 1.8dB respectively are obtained (2.8 and 1.7dB from simulation). The maximum gain is 45dB for both receivers (as expected for FDD and 2dB less for TDD). We believe that the 1dB extra noise and the 2dB less gain for TDD are due to a reduced gain in the third coil and/or a misalignment in the resonant frequencies at the source and gate of the input transistors. Figures 5.1.5.a-b show that when the LC BB tank frequency is lowered with respect to its nominal value the NF degrades by at least 1dB. Figure 5.1.5.c shows both NF and gain with a blocker 20MHz from the carrier vs. blocker power for TDD. Below -2dBm the generators noise floor dominates NF degradation. At 0dBm the NF reaches 7.9dB. We believe that also this value is affected by instruments noise. Notice that gain compression at 0dBm is only 1.4dB. Figure 5.1.5.d shows 3rd-and 5th-harmonic rejection vs. f_{LO}; 54dB and 65dB are obtained at 2.2 GHz (maximum gain) for TDD. The maximum rejection is around 2.7GHz where the LC BB tank was shifted. Out-of-band IIP3 and 1dB compression are 16 and -1dBm for FDD and 18 and -1dBm for TDD respectively. Uncalibrated out-of-band IIP2 is more than 64dBm for both, all at maximum gain. In both cases the LNAs consume 9mA, the BB 4mA and the LO generation draws 6.5mA at 2GHz. The die micrograph is shown in Fig. 5.1.7. The active area is $0.84mm^2$ for TDD and $0.74mm^2$ for FDD.

Figure 5.1.6 compares our receivers (narrow band) with blocker-tolerant receivers. Comparing our SE receiver with narrow band receivers [1-2] we use a fraction of the area and power to get better linearity and harmonic rejection and comparable noise. Compared with the best wideband receiver [6] we have a worse noise but better linearity, harmonic rejection and area. In addition we consume 20% less power even though [6] uses an SE LNA also making it more sensitive to coupling.

Acknowledgements:
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[6] D. Murphy et al., "A Blocker-Tolerant Wideband Noise-Cancelling Receiver with a 2dB Noise Figure", *IEEE ISSCC Dig. Tech. Papers*, pp. 74-76, Feb. 2012.

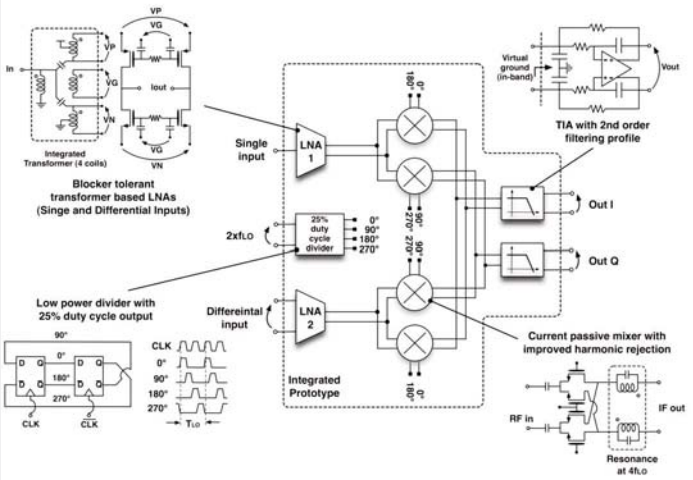

Figure 5.1.1: Integrated RX front-end architecture.

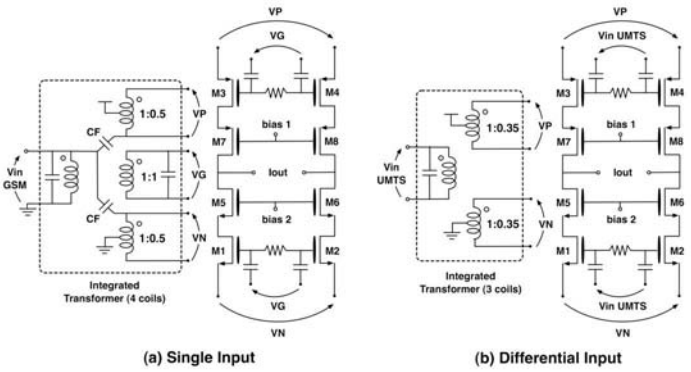

Figure 5.1.2: Transformer-based low-noise amplifiers.

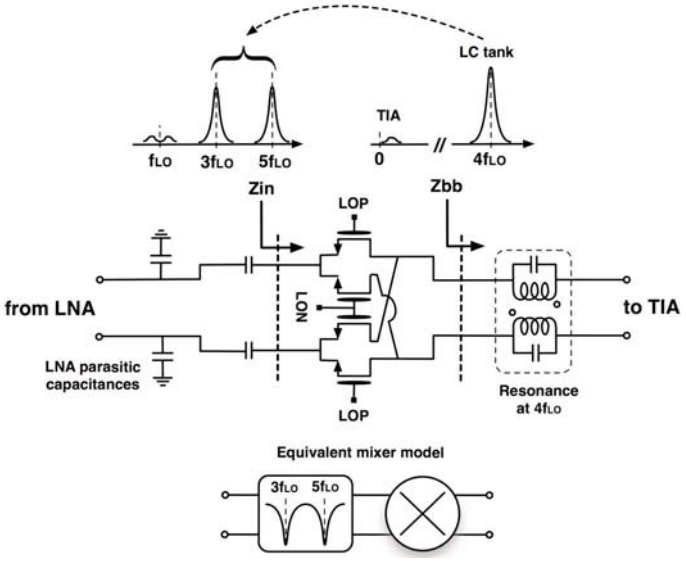

Figure 5.1.3: Current passive mixer with improved harmonic rejection.

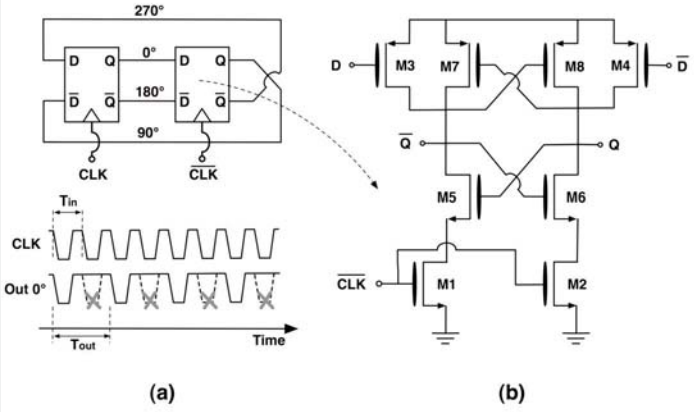

Figure 5.1.4: (a) Divider and qualitative output waveform, (b) Latch architecture.

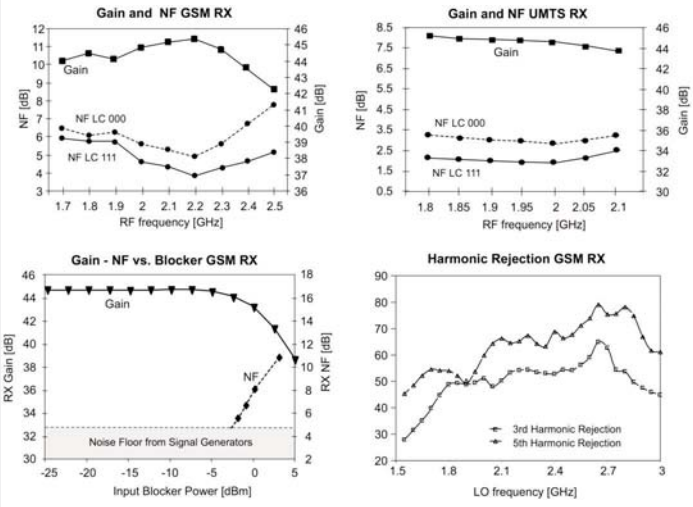

Figure 5.1.5: Measurement results.

	[1]	[2]	[5]	[6]	This work (TDD)	This work (FDD)
RF Frequency [MHz]	850-950/1800-1900	850-950/1800-1900	400- 6000	80-2700	1800-2400	1800-2100
RF input	Single Ended	Differential	Differential	Single Ended	Single Ended	Differential
Gain [dB]	77.8	60.7	70	70	45.5	45.5
NF [dB]	3.1	4.1[1]	4.4[1]	1.9	3.8	3.1[1]
0dBm Blocker NF [dB]	11.4[2]	7[2]	15[3]	4.1[2]	7.9[3]	-
3rd/5th Harmonic Rejection HB	>40/N.A.	44/N.A.	-	42/45	54/65	-
IIP3 [dBm]	>-12.4 (IB)	0 (IB)	10 (OB)	13.5 (OB)	18 (OB)	16 (OB)
IIP2 [dBm]	>45 (IB)	>44.3 (IB)	70 (OB)	54 (OB)	64 (OB)[4]	66 (OB)[4]
Active Area [mm^2]	2.4[5]	1.4	2	1.2	0.84	0.74
Supply Voltages [V]	1.3/2.7	2.8	1.1/2.5	1.3	1.2/1.8	1.2/1.8
LNA+Mixer+BB [mW]	165[6]	92[7]	30-55	31.2	24.3	24.3
LO divider current [mA]	N.A.	N.A.	N.A.	26 (2GHz)	6.4 (2GHz)	6.4 (2GHz)
CMOS technology	65nm	65nm	40nm	40nm	40nm	40nm

[1] Including 1.2dB Balun loss [2] 80MHz Blocker Offset [3] 20MHz Blocker Offset
[4] Measured from 3 samples [5] Including VCO and synthesizer
[6] Entire RX: 55mA (from the battery) multiplied for 3V [7] Including ADC

Figure 5.1.6: Measurement summary and state-of-the-art comparison.

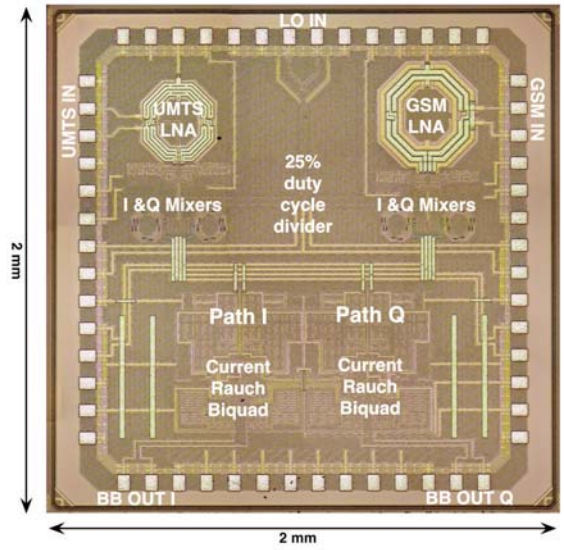

Figure 5.1.7: Die micrograph.

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