19.7 An LTE Transmitter Using a Class-A/B Power Mixer

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For an LTE transceiver it is quite challenging to reduce power and area while preserving performance. For large emitted signals the TX dominates power consumption but in the past this situation was sufficiently infrequent not to affect energy consumption. In recent times the statistical distribution of the TX power has shifted upward due to the use of data-intensive communications and the introduction of multi-gain power amplifiers. Therefore to extend battery life in fourth generation terminals, TX consumption at high power (>-10dBm) should be reduced. A second challenge of an FDD LTE TX is noise and distortion emission in the RX band since the TX-to-RX distance, relative to the channel bandwidth, can be much smaller than in previous standards [1].

A typical RF TX includes DAC, baseband filter, upconverter and pre-power amplifier (PPA). In some cases the PPA is not used and incorporated in the power mixer. This solution draws more current but reduces noise as shown in equation 1 that expresses the mixer signal-to-noise ratio (SNR) as a function of its gm stage bias current (Ibias), for Class-A operation and a given transistor overdrive voltage Vov.

$$SNR = \frac{Vov \cdot Ibias}{8kT \cdot PAR} \quad (1)$$

From equation (1), the SNR ratio varies as follows. First it increases with bias current. Second it deteriorates with signal Peak-to-Average Ratio (PAR). Third it improves with transistor overdrive. A Class-A power mixer requires a minimum bias current to deliver its target power, which decreases as the output swing is increased. If this current is higher than that required to achieve the target noise in the RX band (for a given duplexer), the use of a PPA becomes feasible. However other considerations may discourage such a choice. First the PPA degrades Counter Intermodulation (CIM) and the Adjacent-Channel Leakage Ratio (ACLR). Second lowering noise emission allows the use of a lower selectivity duplexer which may result in cost savings and/or reduced losses [2].

To reduce the bias current of a Class-A power mixer through an increase of its output swing, while limiting overall power consumption the authors in [3] have biased the mixer from 2.7V and the rest of the TX from 1.5V. This requires two high-efficiency switch-mode supplies and stresses the technology. A better solution is to use a Class-A/B power mixer that saves power and reduces noise [4]. The latter because the gm stage current noise is proportional to its average transconductance, which is equal to half of its peak value in Class A and much less in Class A/B especially for high PAR signals.

Class A/B operation is achieved by placing in front of the mixer a differential voltage-to-current converter (V-to-I) whose output transistors are biased with a current much smaller than the peak signal current. A conceptual schematic of the V-to-I converter is shown in Fig. 19.7.1. The circuit performs three main functions. First it converts (via Rin) the voltage signal at the filter output into two differential currents that are sourced and sunk by the two push-pull output stages. For good linearity both differential and common-mode signals at the OpAmp input should be kept small over the entire band of interest. This is achieved using two common-mode feedback loops, one at the drain and the other at the gate of the output n-MOS devices, and increasing OpAmp bandwidth. Second it sends the current sourced at its outputs to programmable current mirrors that feed the two mixers. A passive first-order filter is embedded in each current mirror to reduce the out-of-band baseband noise. Third it insures that the current mirrors are driven with a low impedance, purely differential signal. Low impedance driving improves EVM, making the bandwidth of the passive filters signal independent. Differential driving improves mirror linearity (so ACLR and CIM) for narrow passive filters. In fact, simulation shows that after nulling-out their common mode, each single-ended signal shows no even distortion and less odd distortion.

The overall TX architecture is shown in Fig. 19.7.2. It uses direct digital carrier modulation through a $\Delta\Sigma$ PLL for 2G and I/Q direct upconversion for 3-4G. For the latter case each (I/Q) TX path is made up of DAC, baseband filter, V-to-I converter and power mixer. The mixers' differential current outputs are combined and converted to single-ended by one of the baluns (tuned to different bands). The 10b DAC uses a current-steering segmented topology with current-source scrambling. The filter implements either a 3rd- or 5th-order transfer function with programmable cut-off from 5 to 20MHz and 6dB gain. A Tow Thomas biquad plus the passive filter are always present while a second biquad is activated only for certain critical bands. The current-mirror gain has 20 steps. The upconverters use a Gilbert architecture with MOS switches operated in the linear region. Their re-combined differential output currents are sent, via a cascade device, to one of the output baluns that drive the output pins. From 0 to 30dB of attenuation can be implemented at RF. Only 2 upconverters (for I/Q) are used for all the supported bands to save area.

The transmitter has been implemented in a 55nm CMOS technology and occupies an active area of 1.3mm^2. The output spectrum for LTE20 for both a single Resource Block (RB) and 100 RB signals with a power of 2.4 and 4dBm respectively is given in Fig.19.7.3, showing a CIMR3 of -57.1dBc, ACLR of -40.9dBc, and CIMR5 of -61.2dBc. ACLR1 and ACLR2 versus power for LTE10 are shown in Fig. 19.7.4. They stay below -46/-54dBc respectively up to 4dBm. For WCDMA they stay below -46/-65dBc respectively up to 5dBm. For small output power ACLR1 and ACLR2 are around -50 and -57dBc respectively demonstrating the excellent linearity. The linearity degradation that starts beyond about -1dBm for LTE and 2dBm for WCDMA is due to compression in the upconverter. Similar behavior is shown by EVM vs. power, e.g. for LTE20 it remains below 1.4% up to 1dBm and reaches 1.8% at 4dBm. At 0dBm the RX band noise for 3G and LTE (5, 10 and 20) varies from - 154 to -160dBc depending on the offset frequency. The worst value of -154dBc for LTE10 and an offset frequency of 31MHz is due to the baseband. The supply current for the complete transmitter (from DAC to upconverter) shown in Fig. 19.7.5 versus TX power is very low and independent of the standard. Transmitter performance is summarized in Fig. 19.7.6. Comparing with the results of [3] (Class A) for LTE20 our transmitter show similar performance but in about 1/4 area, more than a factor of 2 power saving at 4dBm and about 40% at -10dBm (notwithstanding the use of only one supply). Furthermore, going from WCDMA to LTE20 (i.e. increasing the PAR by almost 3dB) the current consumption for a given output power in our case stays practically constant (see Fig. 19.7.5) while for [3] it increases by about one third consistent with an almost ideal Class-A/B versus Class-A behavior.

Acknowledgments:
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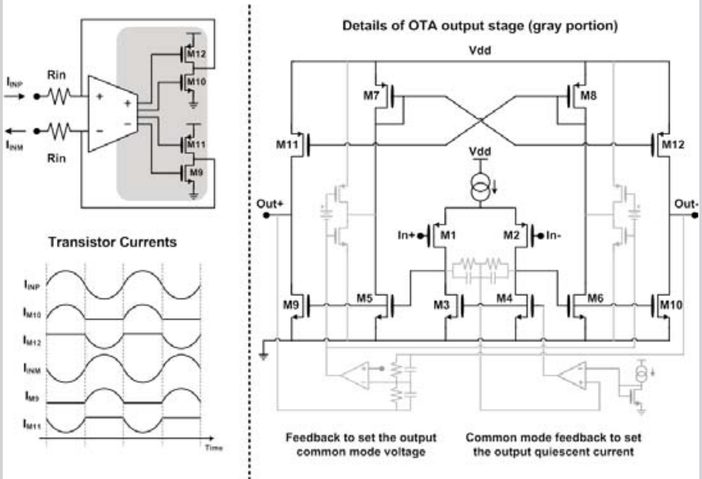

Figure 19.7.1: V-to-I converter schematic.

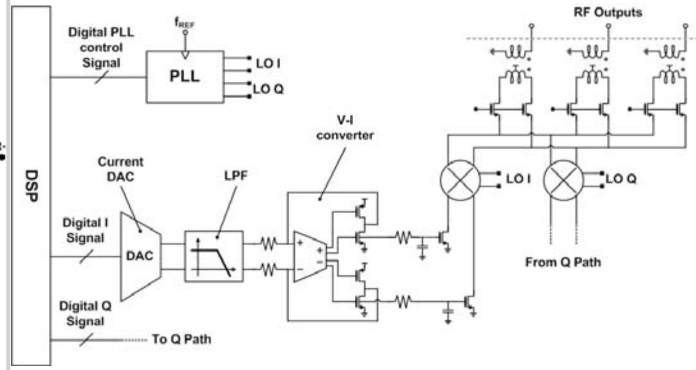

Figure 19.7.2: TX block diagram.

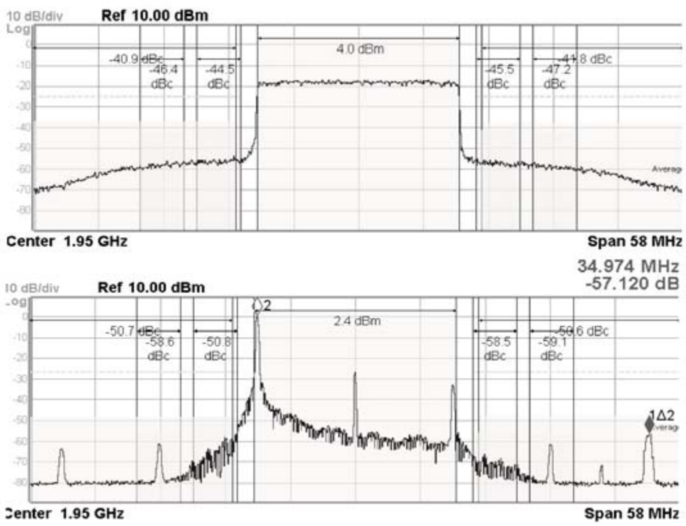

Figure 19.7.3: Output spectrum (RB = 100, RB = 1).

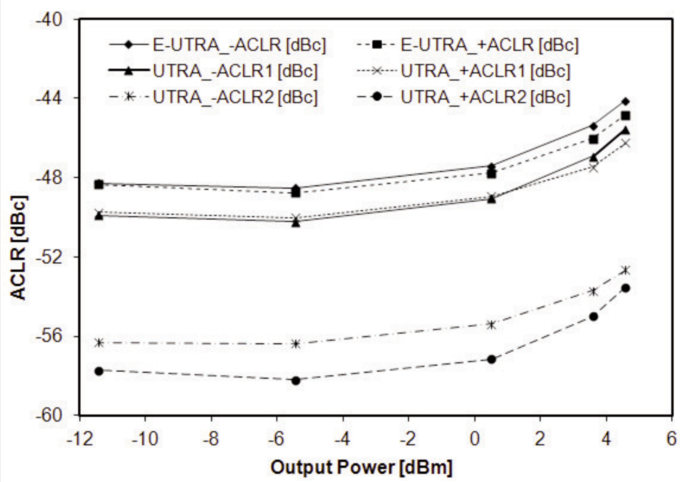

Figure 19.7.4: ACLR vs output power.

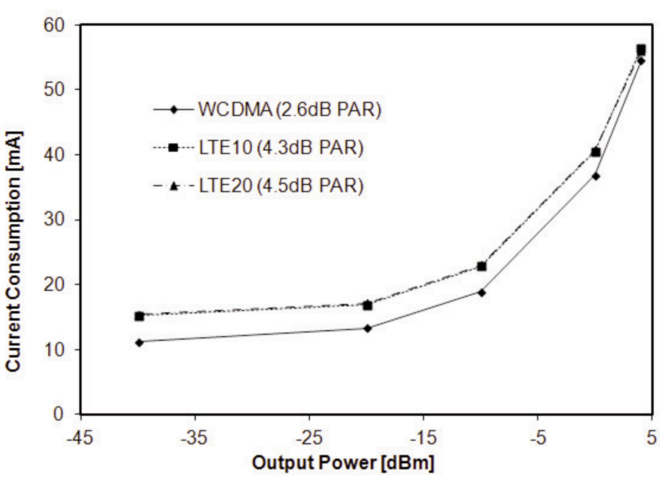

Figure 19.7.5: Current consumption vs output power.

Parameter	Units	Ref. [3]			This paper		
Standard	-	3G	LTE10	LTE20	3G	LTE10	LTE20
RF Bandwidth	MHz	5	10	20	5	10	20
Max Output Power	dBm	4.1	3.7	4	7	6	6
ACLR/ACLR2 at 4 dBm	dBc	-43.7/NA	-40.3/NA	-40.3/NA	-47/-66	-45/-55	-40.9/-55
EVM at 0dBm	%	1.54	0.66	1.05	1.4	1.4	1.4
CIMR3 at 2.3 dBm	dB	-	-	63.5	-	-	57.1
Rx Band Noise	dBc	-156/-159	-155/-164	-157/-162	< -154		
Consumption at 4 dBm	mW	150	186	199	98	101	101
Consumption at -10dBm	mW	45	56	70	29	34	34
Supply Voltage	V	1.55/2.7			1.8		
Chip Area	mm^2	5.06			1.3		
Tecnology	nm	90 CMOS			55 CMOS LP		

Figure 19.7.6: Performance summary.

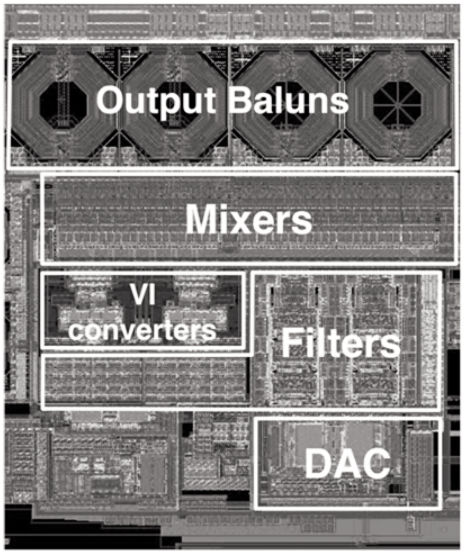

Figure 19.7.7: TX die micrograph.

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