Introduction to the Special Issue on the 38th European Solid-State Circuits Conference (ESSCIRC)

I. Introduction

THIS special issue is dedicated to some of the best papers from ESSCIRC 2012 held in Bordeaux, France. Papers in this issue cover the traditional ESSCIRC topics of analog and power management circuits; data converters, digital circuits, RF and communications, frequency synthesis, and imaging. The papers are briefly introduced in Sections II–VII.

II. Analog and Power Management

In the first paper in this section, Meyvaert *et al.* present a fully integrated 265 V_{RMS} input AC-DC interface in 0.35 μm CMOS technology, requiring only one optional external low-voltage SMD capacitor for improved performance and capable of directly interfacing the universal line voltage and outputting a regulated DC voltage of 3.3 V.

The next paper, by Masuch *et al.*, presents an RF energy harvester embedded in a low-power transceiver front-end in 130 nm CMOS. Both the harvester and the transceiver use the same antenna and operate at the same frequency of 2.4 GHz. The circuit achieves a measured peak power conversion efficiency of 15.9%. For input power levels of at least -9 dBm, it is able to charge up a supply capacitor to a regulated voltage of 1.34 V.

Xu *et al.* present a fundamental theoretical analysis and measurement of the current noise of several chopper instrumentation amplifiers, demonstrating that the charge injection and clock feed-through associated with the MOSFETs used in the input chopper give rise to significant input current and current noise.

The last paper in this section, from Jansen *et al.*, describes the design of an accurate and static complementary constant-gm biasing circuit for Nauta's transconductors in low-power low-frequency CMOS gm-C bandpass filters and their optimization and trimming for process and temperature independent filter performance. Silicon results for a 3rd-order Butterworth bandpass filter in 180 nm CMOS with a 2 MHz bandwidth and center frequency designed for a Zigbee applications show that with a single trim for process over a 120°C temperature range, less than 2% deviation is possible in the bandwidth and center frequency.

III. Data Converters

The first paper in this section, from Spiridon *et al.*, presents a 375 mW multi-mode DAC-based transmitter with 2.2 GHz signal bandwidth and in-band IM3 <-58 dBc in 40 nm CMOS. The DAC includes feed-forward pipelined digital logic and a distributed decoder which enables the DAC sampling rate to extend to 5 GHz.

Next, Christen presents a 15-bit 140 μW scalable-bandwidth inverter-based $\Delta\Sigma$ modulator for a MEMS microphone. The modulator achieves low power consumption and a small die area by using a simple digital inverter instead of OTAs.

IV. Digital Circuits

The first paper in this section, from Kim *et al.*, presents a An 86 mW 98 GOPS ANN-Searching Processor for Full-HD 30 fps Video Object Recognition with Zero-less Locality-Sensitive Hashing. Approximate Nearest Neighbor (ANN) searching is an essential task in object recognition and the authors demonstrate a high throughput ANN-searching processor which adopts an inter-frame cache architecture as a hardware-oriented approach and a zero-less Locality-Sensitive-Hashing algorithm as a software-oriented approach.

Lee and Verma present a paper demonstrating a low-power processor with configurable embedded machine-learning accelerators for high-order and adaptive analysis of medical-sensor signals. Medical applications for EEG-based seizure detection and ECG-based cardiac-arrhythmia detection are demonstrated using clinical data, while consuming 273 μJ and 124 μJ per detection, respectively. The paper shows that this represents 62.4X and 144.7X energy reduction compared to an implementation based on the CPU. A patient-adaptive cardiac-arrhythmia detector is also demonstrated, reducing the analysis-effort required for model customization by a factor of 20.

V. RF and Communications

The first paper in this section, from Fisher *et al.*, presents a reconfigurable Single-Photon Avalanche Diode integrating receiver in standard 130 nm CMOS for optical links with an array readout bandwidth of 100 MHz. A maximum count rate of 58 Gphoton/s is observed, with a dynamic range of 79 dB, a sensitivity of -31.7 dBm at 100 MHz and a BER of 1×10^{-9}. The sensor core draws 89 mW at the maximum count rate and obtains a peak SNR of 157 dB. The all-digital 32 x 32 SPAD array achieves a minimum dead time of 5.9 ns and a median dark count rate of 2.5 kHz per SPAD.

De Jong *et al.* present a fully integrated dual band Ka-band down-converter for VSAT applications. The High-Band and the Low-Band are simultaneously down converted and independently accessible by two users. With a SSB-NF better than 8 dB, a conversion gain higher than 20 dB, and a integrated PLL with an integrated phase noise of 1.2 degrees rms, the proposed architecture consumes 548 mW.

Similarly to the previous paper, the solution presented by Sundström *et al.* allows non-contiguous dual carrier reception, this time for 3 GPP standards. The paper describes a a complex IF mixer for a double conversion receiver architecture containing four harmonic rejection (HR) mixers, each of which implemented with 64 passive unit cell mixers, clocked by a ring-

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oscillator based phase-locked loop and driven by sequencers that represent thermometer-coded oversampled sinusoidal LO waveforms. The complex IF mixer supports reception of two carriers with up to 65 MHz separation using 12 samples per IF LO period and a clock frequency of 390 MHz. The IF mixer is implemented in 65 nm CMOS, has an area of 0.74 mm^2, draws 26 mA, and has a harmonic conversion lower than -68 dBc per harmonic.

The fourth paper, by Carballido *et al.*, presents a portable a flexible and portable digital framework for Built-in Self-Test (BIST) and calibration of RF/analog circuitry. The proposed reusable, flexible testing framework is composed of a centralized custom processing engine with data path, memory architecture and instruction set optimized for efficient execution of compute intensive test and calibration algorithms. This innovative BIST engine is complemented with a calibration and test sequencing methodology exploiting the embedded test hardware, to dynamically correct for transceiver imbalances and non-idealities, as well as to estimate performance parameters such as Error Vector Magnitude (EVM).

The next paper in this section, by Dasalukunte *et al.*, reports an iterative decoder for Faster-than-Nyquist (FTN) and orthogonal signaling multi-carrier systems. FTN signaling is a method of improving bandwidth efficiency at the expense of higher processing complexity in the transceiver. The decoder can switch between orthogonal and FTN signaling modes and exploits channel properties to improve bandwidth efficiency. The decoder is fabricated in a 65 nm CMOS process and occupies a total area of 0.8 mm^2 with decoder core taking up 0.567 mm^2. With a total power consumption of 9.6 mW at 100 MHz this solution represent the he first-ever silicon implementation of a decoder for FTN signaling.

Heragu *et al.* presents a Bulk Acoustic Wave (BAW) resonator-based 2.4 GHz low-power receiver. The intrinsic high quality factor of the BAW resonator is exploited to provide channel selection at RF and in the frequency synthesis to generate high spectral purity signals. The key idea is to address multiple channels (arbitrary frequency) using integer dividers and a BAW digitally controlled oscillator, avoiding the need for a PLL.

The last paper of this section, by Zheng and Luong, is a CMOS WCDMA/WLAN polar transmitter is presented. The proposed architecture is composed of a digital interpolation filter for up-sampling of the input amplitude-control word (ACW), a 9-bit switched-capacitor array for the digital polar modulation (DPM), and a 6-bit PA array to achieve the output power range for the target applications. A linearization technique is implemented by adaptively changing the PA bias voltage according to the RF envelope. Even without amplitude pre-distortion, the transmitter system measures RMS-EVM of 2.83% and 4.07% for WCDMA and WLAN 54 Mb/s 64-QAM OFDM respectively, while providing a peak output power of 20.4 dBm with PAE 32.3%.

VI. Frequency Synthesis

Three papers are dedicated to the frequency synthesis. Two PLLs and a hybrid class-C class-B VCO. Deng *et al.* propose a sub-harmonic injection-locked frequency synthesizer with frequency calibration scheme for millimeter-wave TDD transceivers. The proposed synthesizer is capable of supporting all 60 GHz channels (58.1–65 GHz) including channel-bonding defined by 60 GHz wireless standards for short-range high-speed wireless communications. In order to guarantee a robust performance over PVT variations of the conventional frequency synthesizer, a frequency calibration scheme is proposed to automatically correct a frequency drift of quadrature injection locked oscillators.

The second paper of this section, by Kim *et al.*, is a digital PLL based on a mismatch insensitive TDC. A digital frequency-locked loop is used to track and correct for PVT variations in the TDC and no additional linearization or mismatch calibrations are required. The DPLL uses a 20-bit high dynamic range digital-to-analog converter to drive a VCO in order to realize an effective DCO with 100 Hz frequency resolution. The 2.5 GHz output, locked to a 40 MHz reference, exhibits an integrated phase noise of -35 dBc (10 kHz to 10 MHz) while consuming 21 mW. The worst-case spur in the signal output is below -50 dBc without requiring TDC mismatch and linearity calibration.

Fanori and Andreani present two class-C CMOS VCOs with a dynamic bias of the core transistors, which maximizes the oscillation amplitude without compromising the robustness of the oscillation start-up, breaking the most severe trade-off in the original class-C topology. An analysis of several different oscillators is also provided, showing the evolution of the oscillator from the common class-B architecture up to the proposed class-C design.

VII. Imaging

In the final section, two papers concerning imaging are reported. The first one, proposed by Bassi *et al.*, investigates microwave radar imaging for medical applications, in particular for the detection and early diagnosis of breast cancer. The stepped frequency radar receiver introduced is composed by a wideband low-noise amplifier (LNA), linearized transconductors, quadrature current-mode passive mixers, and baseband transimpedance amplifiers (TIAs). A programmable divider/quadrature generator (DQG) provides quadrature signals to the mixers with a local oscillator signal spanning an octave.

The second paper, by Grzyb *et al.*, is focused on imaging systems around 300 GHz. A 288 GHz lens-integrated high-power source implemented in a 65 nm CMOS technology is presented. The source consists of two free-running triple-push ring oscillators locked out-of phase by magnetic coupling. The oscillators drive a differential on-chip ring antenna, which illuminates a hyper-hemispherical silicon lens through the backside of the die.

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He was a summer intern at National Semiconductor, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS LNAs. From 2008 to 2012, he was an Assistant Professor at the University of Pavia and consultant for Marvell Semiconductors in the area of integrated circuit design. In December 2012, he joined the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, as an Assistant Professor. His research interests are in the implementations of transceivers and frequency synthesizers for cellular and ultra-low-power applications.

Prof. Liscidini received the Best Student Paper Award at the 2005 IEEE Symposium on VLSI Circuits and the Best Invited Paper Award at the 2011 IEEE Custom Integrated Circuit Conference. From December 2007 to December 2011, he served as an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS. Currently, he is a member of the TPC of the European Solid State Circuits Conference (ESSCIRC) and the IEEE International Solid State Circuits Conference (ISSCC).

Douglas Smith retired from the position of Vice President and Chief Technical Officer of SMSC in 2012. During his career as an analog IC design engineer, start-up co-founder and then public corporate executive, he wrote numerous articles and journal papers and served for several years on the analog subcommittee of the IEEE International Solid-State Circuits Conference (ISSCC). He presently serves on the analog subcommittee for ESSCIRC and continues to be an enthusiastic supporter of all things analog. He holds many US and non-US patents primarily in the area of amplifier design. He received both his B.S. and M.S. degrees in electrical engineering long ago from the University of Arizona, Tucson, AZ, USA.