SAW-Less Analog Front-End Receivers for TDD and FDD

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***Abstract*—A multistandard SAW-less receiver is designed exploring a current-mode architecture. A class-AB common-gate transformer-based low-noise transconductor amplifier (LNTA) is used to provide high linearity and harmonic filtering. A resonant passive mixer is adopted in order to allow the current-mode operation and improve the harmonic rejection. A low-power divider with intrinsic 25% duty-cycle is introduced to drive the passive mixer. A second-order Rauch biquad with complex poles makes-up the IQ blocker tolerant baseband. The receiver is designed to be suitable for SAW-less TDD and typical FDD applications with 3.8 and 1.9 dB of NF and $>$ 18 and $>$ 16 dBm of IIP3, respectively, using only 32 mW for each receiver.**

***Index Terms*—25% duty cycle, baseband, blocker tolerant, current-mode, direct conversion, divider, dynamic range, frequency-division duplexing (FDD), GSM, harmonic mixing, linearity, low-noise transconductor amplifier (LNTA), low power, noise folding, reciprocal mixing, resonant mixer, SAW-less, time-division duplexing (TDD), UMTS, W-CDMA.**

I. Introduction

HIGH performance wireless receivers, invariably use external surface acoustic wave (SAW) filters to attenuate out-of-band blockers before they reach the low-noise amplifier (LNA) input. For time-division duplexing (TDD) systems, such as GSM, isolation between the transmitter (TX) and receiver (RX) is provided by the T/R switch and not by the SAW. Therefore, the external SAW can be removed if the receiver can tolerate moderately large interferers (e.g., 0 dBm 20 MHz away for GSM [1]) without degrading its dynamic range. On the other hand, in frequency-division duplexing (FDD) systems, like W-CDMA, since the external SAW performs both filtering and duplexing, it becomes much more difficult to eliminate it without incurring in drastic performance penalty. In this case, the main goal is to minimize the receiver noise figure (NF) in order to achieve high sensitivity at the antenna notwithstanding the SAW attenuation.

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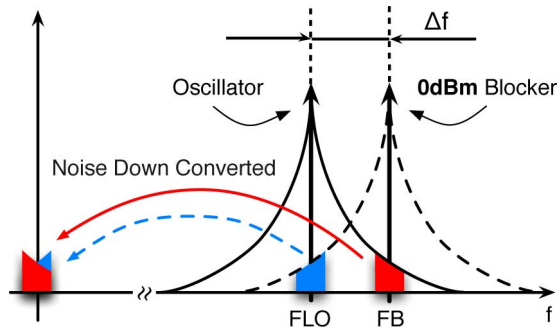

Fig. 1. Reciprocal mixing effect.

Another place where the SAW filter could potentially be removed is in front of the diversity RX chain that is present in both TDD and FDD systems for advanced standard (e.g., release 8 or higher). This is possible, however, only if 20 to 25 dB of isolation between primary and diversity antenna can be insured.

Nowadays, SAW filters perform also differential to single-ended (SE) conversion. Without external SAW, it is very desirable to use an SE input receiver and connect it to the antenna (through the T/R switch). This lowers cost, reduces complexity/form-factor, and improves sensitivity. In fact, without fixed frequency RF filters, it is possible to use a single wideband receiver in place of multiple narrowband ones. Furthermore, eliminating the attenuation associated with the SAW/balun, a SAW-less single-ended transceiver can have a noise figure (NF) 2–3 dB higher than a classical one and still achieve the same sensitivity.

On the other hand, without RF filtering, some of the classical problems of wireless receivers are exacerbated, i.e., gain compression, intermodulation, reciprocal mixing, harmonic mixing, and noise folding.

Gain compression can occur even with a continuous-wave blocker, due to either limited current range (slewing) or limited voltage range (clipping) at RF and/or at baseband (BB) causing de-sensitization. Through the same mechanisms, two or more out-of-band interferers can generate intermodulation products that fall in band. A blocker-tolerant receiver should, therefore, have the lowest LNA transconductance (to avoid slewing when a class-A LNA is used) and the smallest voltage gain throughout the RX chain (to avoid clipping) while maintaining good sensitivity. Furthermore, the BB should have the largest possible dynamic range, i.e., the ratio between the maximum out-of-band signals that it can handle and the in-band noise.

Reciprocal mixing is due to the down-conversion of the LO phase noise by the blocker, as shown in Fig. 1. It follows that, in a SAW-less receiver, to preserve the NF, the LO phase noise

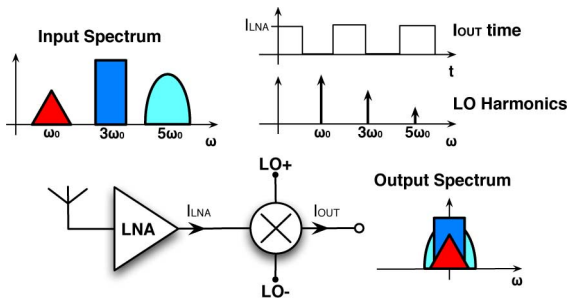

Fig. 2. Harmonic mixing effect.

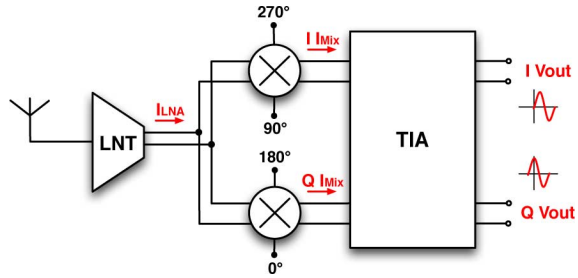

Fig. 3. Current-mode receiver chain.

must be reduced by the amount of filtering originally provided by the SAW [2]. Small LO phase noise implies large power consumption in the VCO/PLL and in the clock phases generation/distribution blocks.

Finally, harmonic mixing/noise folding occurs since down-conversion is done multiplying the RF signal by a square wave. As shown in Fig. 2, the odd harmonics (for a differential topology) of the LO frequency present in the square wave clock folds to BB any signal located at these harmonics. Three GPP requires coexistence with blockers located at all multiple frequency of the channel spacing allowing, however, some exceptions. To limit the number of required exceptions, LO phase noise should be low and harmonic rejection mixing and/or filtering at the LO harmonics should be implemented. On the other hand, noise folding occurs even when no blocker is present and can only be reduced by minimizing the noise energy at the LNA output at the clock harmonics. We will show how, through architecture and circuit innovations, all of the above critical problems can be addressed without incurring in large power consumption penalties.

The paper is organized as follows. Section II gives a brief review of prior art focusing especially on a recent blocker-tolerant, noise-cancelling receiver that represents the reference design at the present time [2]. Sections III–V present the new proposed architecture discussing the key building blocks from the antenna to base band. Section VI provides measurements results. Finally, Section VII draws the conclusion.

II. Overview of Prior Art

Over the years, there has been an evolution of the architecture of wireless receivers and today the *de facto* standard is shown in Fig. 3. It is made up of a transconductance LNA (LNTA) that drives a current-mode passive mixer followed by a low-input-impedance filter or TIA. Such an architecture was studied by Redmann-White [3] and was first implemented at GHz frequency by Sacchi *et al.* [4]. Later, many other have used it [2]–[6] to improve linearity and save power. The advantages of this architecture stem primarily from the fact that most of the voltage gain is moved to BB after a certain amount of filtering has occurred. Furthermore, the I and Q mixers are almost invariably driven by nonoverlapping 25% clock. Such an approach complicates phase generation and distribution, but its better noise for both mixer and BB [7], [8] and larger conversion gain makes it the solution of choice. More recently, the close correspondence between a multiphase passive mixer and a switched capacitor N-path filter has been pointed out [9] and its potential for implementing high-Q bandpass filters analytically demonstrated [10].

Leveraging the architecture of Fig. 3[4], [11], [12], wireless receivers have gone from narrowband to wideband at the cost, however, of increased noise and/or power consumption [2]. Examples are the so-called mixer first topology [13], [14] that eliminates the LNTA from the RX path or some SAW-less architectures [15], [16].

Recently, another step toward the so-called software defined ratio (SDR) has been taken by the blocker-tolerant, noise-cancelling receiver [2] that extends noise cancelling to the entire front-end. While the original noise-cancelling LNA [11]–[17] implements broadband voltage gain (at the risk of clipping), the new receiver uses two noise-cancelling front-ends operated in the current domain. Harmonic mixing is cancelled with an eight-phase harmonic rejection mixer whose outputs are summed in the TIA. The RF front-end achieves excellent antenna sensitivity (1 to 2 dB better than traditional receivers with external SAW), which degrades by only about 2 dB with a 0-dBm blocker. However, even with a SE signal path, it requires about 65 mW at 2 GHz and 1.2 mm^2 in 40-nm CMOS. Furthermore, the SE circuit gives only around 50 dBm IIP2 and is susceptible to spurious couplings since simple inverters are used as gain stages.

As a further step in this evolution, we report a SAW-less SE receiver with excellent linearity and blocker tolerance together with a good mix of sensitivity and bandwidth. Compared with the state-of-the-art [2], it has a narrower band and a larger NF but, provided that the correction of the transformer errors yields the expected results, has the potential to be used in commercial smart phones. On the other hand, it requires much less power and area while offering much better disturbance immunity thanks to the use of a fully differential (FD) signal path. Good harmonic rejection is obtained without the use of a very large number of LO phases. Furthermore, no noise cancellation is used to avoid duplicating the front-end.

The same architecture is used to implement a differential input receiver for FDD applications (like W-CDMA). In this case, the main goal is to take advantage of the fully differential signal to simplify the transformer structure and get much better NF (by almost 2 dB), although with less harmonic filtering.

III. Low-Noise Transconductor Amplifier

Fig. 4 presents a simplified SE version of the LNTA. The circuit is built around an input transformer with one primary and two identical secondary coils. The transformer splits the signal feeding it to the two inputs of a class-AB p-n common-gate

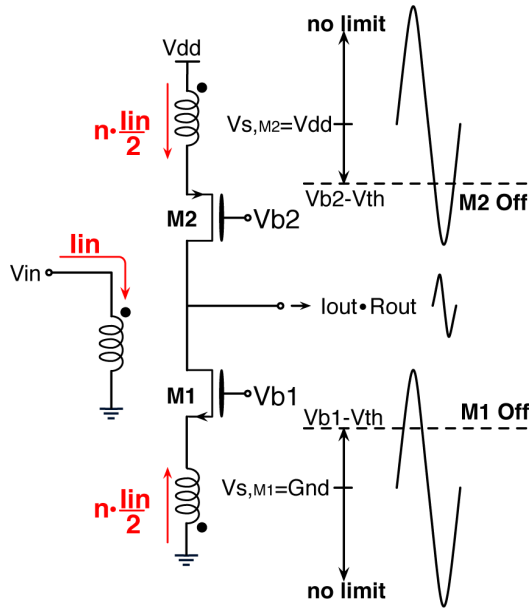

Fig. 4. Single-ended LNTA basic structure.

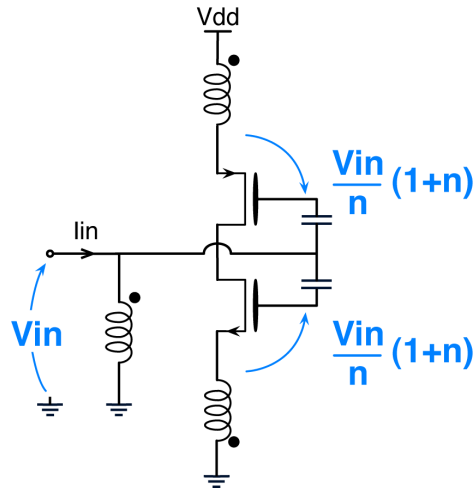

Fig. 5. Single-ended LNTA boosted structure.

amplifier. The use of a transformer allows the voltage to swing above the supply and below ground class-AB operation and low noise biasing. Moreover, the small turn ratio between secondary and primary (high n for a transformer n:1) reduces voltage swing and gives current gain at the secondary. Reducing the swing at the source of the input transistors improves linearity, while current gain is achieved at no linearity penalty. As shown in Fig. 4, the current is split almost equally between the two secondary coils that have the same inductance and drive almost the same impedance. While the input ideally cannot compress, the output can if the load impedance is too high. With an equivalent transconductance of 40 mS, the output compresses at 0 dBm if the differential output impedance is greater than 200 Ω. However, current-mode operation implies a low impedance load, giving a high linearity/compression point. A common-gate topology is used for better linearity but at the cost of a high NF in matching condition [18]. To reduce noise, a passive gate boost is used, as shown in Fig. 5. Applying a replica of the input voltage to the gates of the MOS transistors, the excess noise becomes $1+n$ times smaller than the noise of the classical common gate amplifier as reported in

$$\mathrm{NF}_{\mathrm{CG}} = 1+\gamma \tag{1a}$$

$$\mathrm{NF}_{\mathrm{boost}} = 1+\frac{\gamma}{1+n} \tag{1b}$$

where $\mathrm{NF}_{\mathrm{boost}}$ and $\mathrm{NF}_{\mathrm{CG}}$ are the NF with and without boost, γ is MOS excess noise factor, and n is the transformer ratio. On the other hand, a larger gate–source voltage swing degrades linearity, thus a tradeoff between linearity and NF exists. Both implemented circuits (shown in Fig. 6) use an FD signal path to reject common-mode noise and a cascode stage to improve output impedance for current-mode operation of the mixer. The FDD LNTA [shown in Fig. 6(a)] is FD, making it compatible with an external differential duplexer. Boosting is done through a couple of capacitors connected to the input pins. The TDD LNTA [shown in Fig. 6(b)] is SE and can be directly connected to the antenna switch in SAW-less applications. In this case, the transformer acts like a balun to drive the FD on chip signal path. With a single-ended input, it is not possible to use a capacitive boost, so a fourth coil is required [19].

A. Boosting Tradeoff

The amount of boosting depends on the transformer ratio n and sets the performance of the LNTA. On the other hand, under matching conditions, the gm of each input MOS transistor is constrained to be

$$gm = \frac{n^2}{Rs(1+n)}. \tag{2}$$

Fig. 7 shows the gm required to achieve matching and the corresponding NF versus the transformer ratio. For $n<1$, the NF is close to that of a classical CG, while for $n>4$ the required gm, and therefore power consumption, is not compatible with the targets. The range $1<n<4$ has been divided into two zones, one more suitable for TDD $(n<2.5)$ and one for FDD applications $(n>2.5)$. For the TDD case, high linearity/compression has been favored with respect to NF since a SAW-less receiver can have an NF 2–3 dB higher but should handle large out-of-band interferers. On the other hand, for the FDD case, the duplexer requires lower NF but reduces the linearity requirement.

B. Transformer Design Issues

In both the SE and the FD LNTA, the transformer has a key role; however, being connected to the input pins, its noise is directly added to the noise of the source degrading the NF. To reduce losses, the transformer should have a coupling coefficient as close as possible to one and the highest Q to reduce its intrinsic noise. The achievable performances are strictly correlated to the technology adopted. Nowadays, a low-cost RF process (as the one used) has typically no more than six copper layers, of which just one thick, plus a thick aluminum one for bond pads (AP). To maximize the coupling coefficient, the primary and secondary coils should be overlapped [20], however, with only one thick metal layer, this compromises the quality factor of one coil.

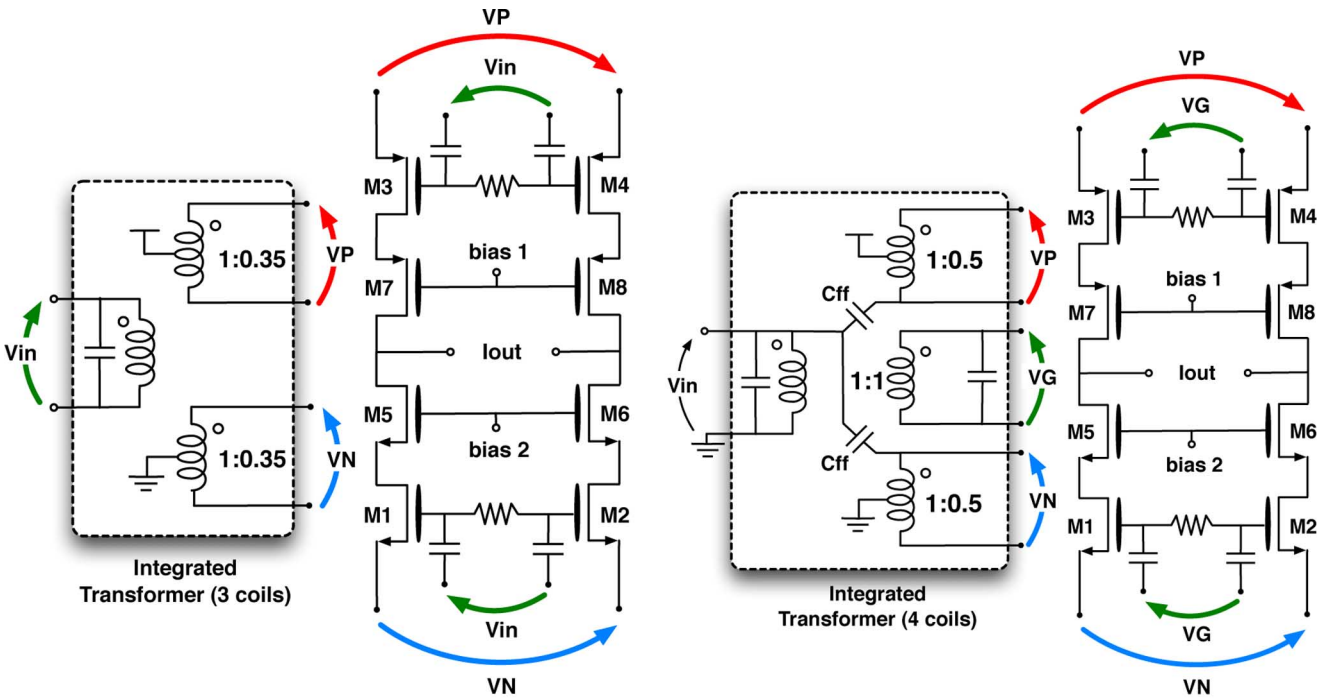

Fig. 6. (a) Fully differential LNTA for FDD applications. (b) Single-ended input LNTA for TDD applications.

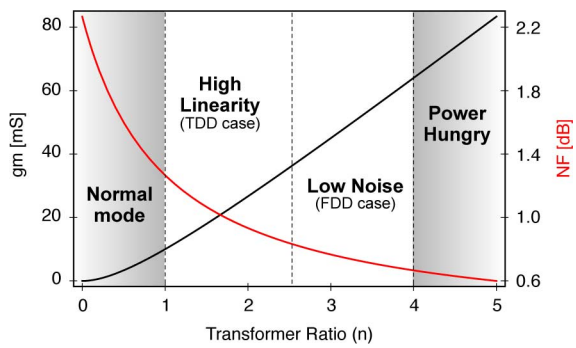

Fig. 7. Input MOS transconductance and NF versus transformer ratio.

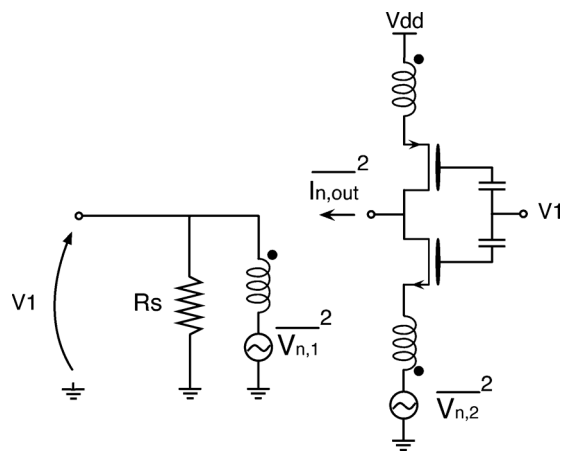

Fig. 8. LNTA simplified scheme for transformer noise analysis.

In the case of a simple transformer, it is possible to demonstrate that, independently of the current gain n, the two coils contribute equally to the overall noise and, thus, a stacked design inevitably penalizes one of the two windings. However, in the case of the LNTA proposed (Fig. 8), it is possible to demonstrate that, when the impedances of the windings are much greater than the driving and loading impedances, the noise transfer function associated with the primary coil is

$$i_{n,\text{out}}^2 = \left|\frac{n}{2Rs}\right|^2 \cdot V_{n,1}^2 \tag{3}$$

while for a single secondary coil it is

$$i_{n,\text{out}}^2 = \left|\frac{n^2}{4Rs(1+n)}\right|^2 \cdot V_{n,2}^2. \tag{4}$$

Therefore, the noise contribution of the secondary with respect to the primary is

$$V_{n,2}^2 = \left|\frac{n}{2(1+n)}\right|^2 \cdot V_{n,1}^2. \tag{5}$$

From (5), for $n > 1$ (as used in this design), the noise of the secondary is lower than that of the primary for the same Q. Therefore, the primary coil should use the thick copper metal while the secondary should use the AP metal due to its minor impact on the overall noise of the transformer.

When an additional coil is needed, as in the case of the LNA topology of Fig. 6, it is not possible to use a three-layer stacking to have both symmetric secondary and maximum quality factor since the bottom metal would give too much series resistance. The two secondary coils are thus realized on the same plane using the AP metal while the boosting coil is implemented with the thick copper layer as the primary coil. In general, the transformer use no more than two or three turns coils to avoid a large number of crosses that would degrade the overall quality factor.

Considering all the above constraints (NF versus power tradeoff and technology limits), the transformer ratios for the

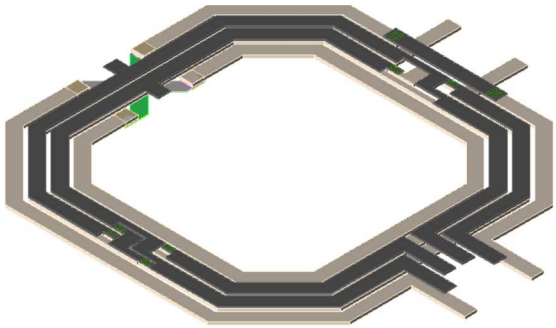

Fig. 9. Layout of three secondary transformer topology for SE LNTA.

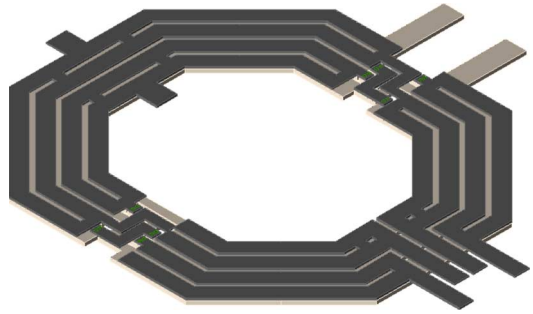

Fig. 10. Layout of two secondaries transformer topology for FD LNTA.

SAW-less receiver is $2:1$ (high linearity zone) while for the FDD receiver is $3:1$ (low noise zone). For the $2:1$ transformer, a primary with two turns is used. This is because the two secondary can be obtained using the exact same shape as the primary changing only the metal layer and the position of the cross. Unfortunately, since in this case the secondary coils need a center tap to provide VDD and ground connections, a symmetrical structure demands two crosses instead of one. To maximize coupling and to minimize the number of crosses the position of the crosses should be the same for both primary and secondary coils. This can be obtained in a simple way rotating the input (primary) by 90 degrees with respect to the outputs (secondary) (Fig. 9). Notice that, through this layout, an exact 2:1 ratio is obtained taking advantage of the constructive mutual inductance between the two coils. For the third secondary, a concentric spiral winding is used. Placing one turn of the secondary inside and one outside of the primary winding, as shown in Fig. 9, the desired 1:1 ratio is obtained. The light gray lines are the ultrathick copper used for the primary and the boosting coil while the dark gray lines are the AP used for the two secondary. To maximize the coupling, the primary and the two main secondary are perfectly overlapped.

According to [20], a transformer can have a notch in the transfer function due to the coupling capacitor that always exists between primary and secondary coil. This notch occurs at the particular frequency for which the capacitor current and the induced current cancel out as they are equal in module and opposite in phase. The frequency of the notch can be adjusted adding an explicit capacitance between the primary and the secondary coil, as shown in Fig. 6(b). Tuning the position of the notch such that it corresponds to the frequency of the third harmonic at least 30 dB of extra harmonic rejection can be obtained over the entire band of interest.

Using the same criteria outlined above, it is possible to realize the two secondary of the $3:1$ transformer, as shown in Fig. 10. The two dark gray lines (the two secondary) occupy the same space as the three-turns light gray lines (the primary) in order again to maximize coupling.

IV. Resonant Mixer and 25% Duty-Cycle Clock

The I and Q down-converters are realized by using a current-mode passive mixer in series with an LC tank resonating at the fourth harmonic of the local oscillator (LO) (Fig. 11). The impedance of the LC tank Z_{bb} is reflected at the input of the

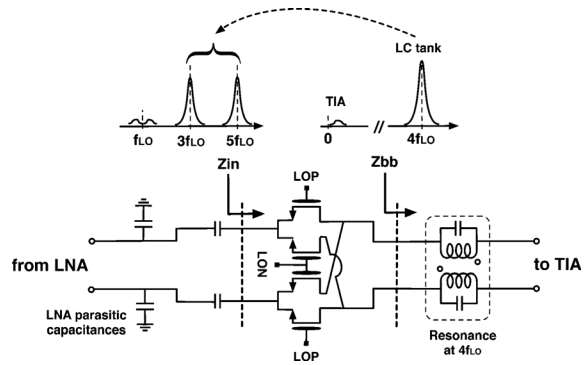

Fig. 11. Resonant mixer.

mixer shifted up and down in frequency by $f_{\rm LO}$ (and scaled in value). This increases the impedance seen looking into the mixer around the third and fifth harmonics of the LO. Due to such an impedance translation mechanism, the current partition between the output impedance of the LNA ($Zout_{\rm LNA}$) and the mixer input impedance reduces the current entering the mixer at the third and fifth harmonics of the LO without significantly affecting the one at the fundamental frequency. The end result is an improvement in the overall harmonic rejection of the RF front-end.

A. Third and Fifth Harmonic Rejection

Assuming a perfectly differential structure (i.e., neglecting even harmonics), the input impedance of the 25% duty-cycle quadrature mixer $Zin(\omega)$ can be approximately found using the theory of Mirzaei *et al.* [7] as

$$\begin{aligned} Z_{\rm in}(\omega) =& R_{\rm SW} + \frac{2}{\pi^2} \\ &\times [Z_{\rm LC}(\omega-\omega_{\rm LO}) + Z_{\rm LC}(\omega+\omega_{\rm LO})] + \\ &+ \frac{2}{9\pi^2}[Z_{\rm LC}(\omega-3\omega_{\rm LO}) + Z_{\rm LC}(\omega+3\omega_{\rm LO})] + \cdots \end{aligned} \tag{6}$$

where $Z_{\rm LC}(\omega)$ is the impedance at the mixer output (assumed to be narrowband). Assuming for simplicity that the down-converted signal is sensed by an ideal TIA, $Z_{\rm LC}$ becomes the LC tank resonating at $4\omega_{\rm LO}$. $Z_{\rm LC}$ appears at the input of the mixer scaled by a factor $2/\pi^2$ around the third and fifth harmonics and by a factor $2/(9\pi^2)$ at $\omega_{\rm LO}$ (higher harmonics have been neglected for simplicity). Since the LC tank is reflected also around

$\omega_{\rm LO}$, $Z_{\rm LC}$ should satisfy the following condition to minimize current attenuation at $\omega_{\rm LO}$:

$$\left|\frac{\pi^2}{2}Z_{\rm LNA}(3\omega_{\rm LO})\right| \ll |Z_{\rm LC}(4\omega_{\rm LO})| < \left|\frac{9\pi^2}{2}Z_{\rm LNA}(\omega_{\rm LO})\right|. \quad (7)$$

The right-hand side of this inequality assumes $|Z_{\rm LNA}(3\omega_{LO})| > |Z_{\rm LNA}(5\omega{\rm LO})|$, as it is usually the case. The tradeoff set by (7) indicates a limit in the maximum rejection achievable with this technique. Assuming $Z_{\rm LNA}$ is dominated by the capacitance at the output of the LNA ($C_{\rm LNA}$), (7) can be rewritten as

$$\frac{1}{6}\frac{\pi^2}{\omega_{\rm LO}C_{\rm LNA}} \ll |Z_{\rm LC}(4\omega_{\rm LO})| < \frac{9}{2}\frac{\pi^2}{\omega_{LO}C_{\rm LNA}}. \quad (8)$$

From (8) and allowing less than 0.5 dB attenuation at the fundamental frequency, the maximum attenuations at the third and fifth harmonic are 18 and 23 dB, respectively, giving a potential additional harmonic rejection of 17.5 and 22.5 dB, respectively.

The harmonic rejection of the resonant mixer is also limited by both the Q and the self-resonance of the integrated inductor in the tank. In this design, a rejection just above 10 dB was obtained around $3\omega_{\rm LO}$ and 15 dB around $5\omega_{\rm LO}$. Considering that the mixer itself intrinsically provides 10 dB of rejection at the third harmonic and 15 dB at the fifth harmonic (for a perfect square-wave LO), the total achieved rejection obtained was about 20 and 30 dB, respectively. Notice that these harmonics are also filtered by the input transformer (by about 30 dB) before they reach the mixer leading to a total rejection around 50–60 dB.

Since the $Zout_{\rm LNA}$ is relatively low at these frequencies due to the the parasitic capacitance (estimated at 250 fF), the voltage swing at the third and fifth harmonics is not sufficient to degrade the linearity performances. Considering for example a third harmonic at 6 GHz, $Zout_{\rm LNA}$ is approximately 100 Ω. For a 0-dBm blocker with an equivalent transconductance of 40 mS and 30 dB of filtering provided by the transformer, the voltage swing at the output of the LNA is approximately 40 mV.

B. Transformer-Based Differential Resonant Tank

The use of a resonant tank in series with each output of both I and Q mixers requires four inductors that, even considering their high resonance frequency, could increase area. Exploiting the differential signal currents provided by the mixer, a transformer-based resonant tank was realized which maximizes the quality factor and minimizes the area (Fig. 12) thanks to the constructive mutual coupling present between the two branches. Referring to Fig. 12, the inductance of each *LC* tank is given by

$$L_{\rm tank} = L(1+k) \quad (9)$$

where L is the inductance of each transform coil and k is the coupling between them. With this strategy, the area of the coils is significantly reduced, and the Q increased since the inductance is effectively doubled. Furthermore, such a resonator has a high impedance only for differential signals, thereby preventing

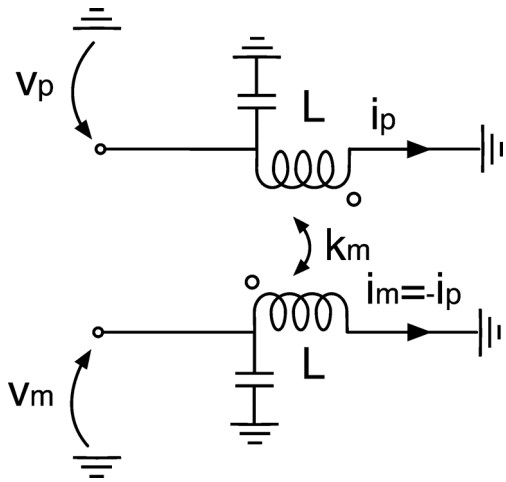

Fig. 12. Transformer-based resonant load.

amplification of the even harmonic that could be present due to mixer mismatches. The tank was designed to have a 1.5 nH of differential inductance and 538 fF of capacitance (250 fF fixed and 36 fF per eight elements switchable).

C. 25% Duty-Cycle Divider

Without any SAW before the LNA, reciprocal mixing can cause a significant NF degradation [21] since any interferer at the mixer input convolving with the phase noise of the local oscillator increases the in-band noise proportionally to the blocker magnitude (see Fig. 1). Since the receiver must handle blockers up to 0 dBm starting from 20-MHz offset, the phase noise of the LO should be lower than -172 dBc/Hz to minimize the SNR degradation [2]. Because of this, when multiple-phase mixers are used to satisfy the harmonic rejection required from the absence of a SAW, the generation and distribution of the clock could become the most power-hungry section of the entire receiver [2].

The use of the LNTA and the resonant mixer just described limits to four the number of phases required to drive I and Q mixers. However, to maximize conversion gain and to reduce IQ interaction, a 25% duty-cycle must be used [8]. The four clock phases are generated directly by the divider avoiding the use of a dedicated stage and saving power. The divider is derived from one proposed by Razavi *et al.* [22] that generates the 25% duty-cycle outputs thanks to a particular latch [Fig. 13(b)]. When the latch senses the input signal (M1-M2 are OFF), the NMOS pull-down devices are OFF and both outputs are high (one pulled up by the input and the other maintaining the high state from the previous cycle) [22]. This asymmetry in the latch response gives the 25% duty-cycle output.

In the original design [Fig. 13(b)], with M1-M2 ON and either one of the two inputs low, a static current flows between the rails during the entire clock phase leading to an excessive power consumption. To solve this problem, the original divider is modified adding M5-M6 in series to M1-M2 to eliminate the direct path between Vdd and ground Fig. 13(c). Starting from a very clean external clock the divider gives a quadrature clock

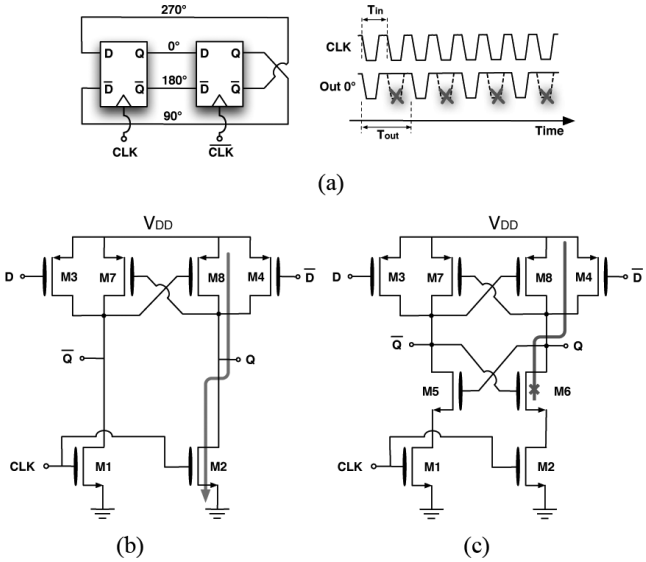

Fig. 13. (a) Divider block diagram and waveform. (b) Old latch structure. (c) Proposed latch structure.

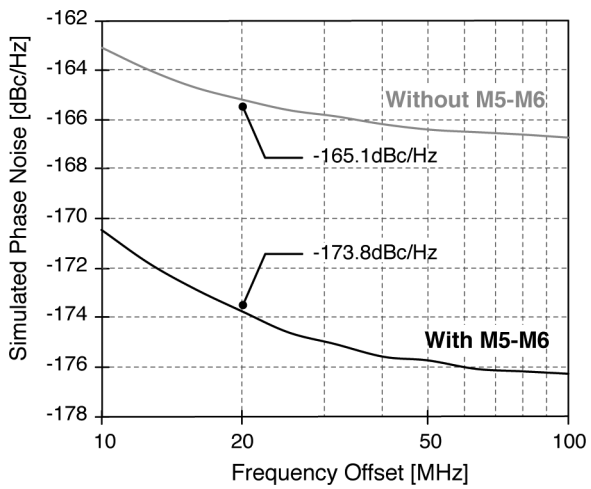

Fig. 14. Simulated PN from extracted layout for old and proposed design.

with −173.8 dBc/Hz phase noise at 20 MHz burning 6.4 mA (simulated from extracted layout) (Fig. 14).

The presence of M5-M6 introduces an additional degree of freedom in the sizing of M1-M2. In fact, in this case, no static current is present and M1-M2 are buffered by the M5-M6 reducing their load to the output. For the same power consumption, a size increment of M1-M2 led to a phase-noise reduction of 8.7 dB compared with the solution proposed in [22] (Fig. 14).

V. Baseband

The absence of RF selectivity for both the in-band blockers (e.g., from 200-kHz to 3-MHz offset in GSM, adjacent channels in UMTS) and the out-of-band ones (e.g., 20-MHz offset in GSM, TX leakage in UMTS) creates a challenging dynamic range requirement for the BB. In fact, the BB section has to handle these large interferers without increasing the noise floor

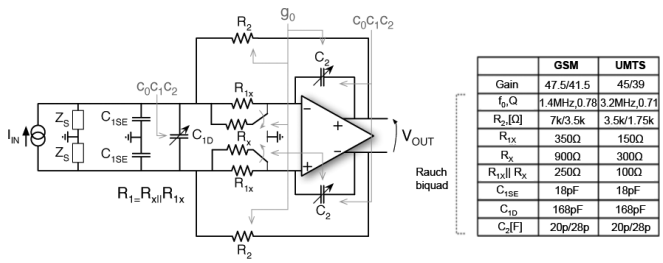

Fig. 15. Rauch biquad-based BB.

of the receiver due to both intermodulation terms and extra noise. The frequency profile of the BB input impedance represents another design constraint, since it affects the operation of the current mode RX chain. Therefore, a BB with low noise, high linearity, and low input impedance over a broad band is targeted. Furthermore, the BB should accomplish these goals with the smallest possible power budget, i.e., consuming less than 30% of the RF section.

Few representative examples are given below. For GSM, a −23 dBm (antenna referred) blocker 3-MHz away has to be handled with less than 5 dB NF. This corresponds to −116-dBm input-referred noise for the entire chain or −126 dBm for the BB (assuming 10% BB noise contribution) i.e., more than 100-dB BB dynamic range at 3 MHz. Also, in the presence of two −40-dBm tones at 0.8–1.6 MHz, an IM3 more than 85 dB below the interferer power is required to give an intermodulation term comparable to the level of the BB noise.

The detailed BB schematic (I or Q section) is shown in Fig. 15. A current-driven Rauch filter is used to directly interface the RF and BB sections, thus avoiding the need of cascaded I–V and V–I stages and compared with [2] has a second-order filter as opposed to a first-order. The input signal I_{IN} is the mixer down-converted current (Fig. 11) while the output is the voltage $V_{\rm OUT}$. Therefore, a transimpedance stage is obtained with Z_S representing the BB driving impedance, i.e., the equivalent mixer output impedance [8]. One control bit switches from TDD to FDD mode, acting on the resistors.

The baseband design goals are met exploiting the following features of the current driven Rauch filter. First, the passive current filter (first-order) implemented by C_1 that limits the amount of interferer current that reaches the OTA high-pass shapes the major noise contributors and keeps the high-frequency BB input impedance low. Second, the low in-band input impedance, provided by the feedback loop built around the high-dc gain OTA. Third, the possibility of implementing gain reconfigurability as explained in [23] to extend the handling capability of high-power blockers (more robustness to fading and input signals PAR). Notice that, although [23] describes a filtering ADC and not an analog filter, its architecture originated from a Rauch biquad. Furthermore, the approach proposed in [23] to handle both GSM and UMTS scenarios has been followed in the present design.

In the following subsections, the key elements of the BB are explained in detail, focusing on how they affect the entire chain.

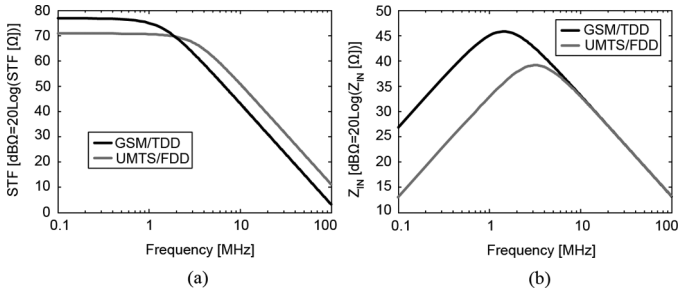

Fig. 16. Baseband. (a) Signal-transfer function. (b) Input impedance.

A. STF, Input Impedance, and Gain Selection

As expected, the signal transfer function $H(s) = V_{\rm OUT}/I_{\rm IN}$ of the Rauch filter Fig. 15 is a biquad

$$H(s) = \frac{G}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \tag{10}$$

in which

$$\begin{aligned} G &= R_2 \\ \omega_0 &= \sqrt{\frac{1}{R_1 C_1 R_2 C_2}} \\ Q &= \frac{1}{\omega_0 C_0 \left(R_1 + R_2 + \frac{R_1 R_2}{Z_s}\right)}. \end{aligned}$$

The feedback resistance R_2 sets the in-band transimpedance gain, while the time constants R_1C_1 and R_2C_2 set the selectivity. Gain, cutoff frequency, and Q will experience PVT variations, since no automatic calibration has been implemented. However, the possibility to tune the capacitances by 30% has been implemented (using bits $c_0c_1c_2$ in Fig. 15) which could be used to compensate PVT effects and/or to allow cutoff reconfigurability. Notice that, since Z_S (whose value is not easily predictable [23]) affects only the Q, the transfer function displays good robustness with respect to parasitic effects. Assuming a purely resistive driving impedance, a Butterworth STF has been chosen to maximize in-band flatness. The simulated STF (for nominal capacitance and high gain mode) for TDD and FDD is depicted in Fig. 16(a).

As already mentioned, a low-BB input impedance is required to insure current operation. This is because a high-BB impedance deteriorates the down-converter linearity, (which limits the receiver linearity) and, in an *I–Q* architecture, increases the asymmetry of the signal transfer function between positive and negative frequencies (complex STF) [7]. The Rauch filter input impedance is equivalent to an *RLC* resonant network where the inductance is synthesized by the gyrator made up of R_2 and the integrator $1/(sC_2R_1)$. In-band, the inductance creates a virtual ground while beyond the cutoff frequency the impedance is set by C_1. At cutoff, the inductance and the capacitance resonate, and the impedance reaches its maximum equal to R_1. The simulated input impedance profile for both TDD and FDD is reported in Fig. 16(b).

The gain control does not affect the BB cutoff frequency and the BB input impedance level [23]. First, the gain is modified reducing R_2 (Fig. 15). Then, R_x is switched from virtual ground (high-gain) to ground (low-gain), introducing a current partition in the filter forward gain. This reduces the integrator bandwidth limiting the increase of C_2 and keeping the resistance seen at the BB input. Finally, C_2 variation compensates for the previous changes to maintain the BB selectivity

B. Noise and Linearity Analysis

The dominant noise contributors are the input resistance R_1 and the operational amplifier. They both benefit from the high-pass noise-shaping mechanism of current filters explained in [24]. Notice that the noise analysis given in [23] can be applied with very little modifications to the Rauch filter, substituting the continuous-time feedback DAC with R_2. The noise of R_2 is not high-pass-shaped but follows the STF profile; however, it can be neglected with a small error. There is a tradeoff between in-band noise and selectivity [24] and between in-band noise and input impedance [25]. Widening the filter bandwidth increases the amount of noise filtering but reduces the interferer attenuation. Furthermore, noise can be reduced by lowering C_1 and increasing R_1 at the price of a higher input impedance.

BB linearity can be improved increasing the OTA open-loop gain at the signal frequency. In fact, the higher the OTA gain is, the smaller the swing at the virtual ground node is which reduces the amount of nonlinear terms for a given output swing. This has been accomplished with a feed-forward-compensated OTA [25].

C. Operational Amplifier

The operational amplifier is the core of the BB. It determines its power consumption, decides its nonlinearity, and contributes in a non-negligible way to its noise.

Considering nonlinearity, the key goal is to increase the OTA bandwidth. Using a traditional single-pole architecture, a very high open-loop unity-gain frequency f_T would be required to get sufficient gain at the frequency of the blockers (e.g., at 2 MHz). On the other hand, the use of feed-forward compensation can overcome this limitation [26]. A fast low-gain feed-forward path (Fig. 17) ensures the stability of the structure by determining the OTA f_T and ensuring -20-dB/decade slope when crossing the 0-dB axes. At the same time, a lower bandwidth higher order main path creates a -40-dB/decade gain slope below f_T, thus increasing the gain at the frequency of interest.

Considering noise, the input differential pair represents the main OTA noise source. To save power, a complementary p-n MOS architecture with current reuse has been chosen for the first stage. Its main benefit is that it gives the same equivalent gm with half of the current of a simple p-MOS or n-MOS only differential pair. Since the current folding branches of the p-n input stage consumes 25% of the total input stage current, 40% power saving is obtained (15% of the total OTA budget).

The OTA needs to drive a very large capacitive load due to the following reasons. First, the need to satisfy the demanding $1/f$ noise target of a direct conversion GSM receiver (100 Hz lower noise integration edge) mandates big input transistors. Combining this with the relatively large feedback capacitance C_2 makes the large $C_{\rm GS}$ of the input transistor to load the output at high frequency. Second, capacitance C_2 (reconfigurable) has about 5% parasitic to ground at both the top and the bottom

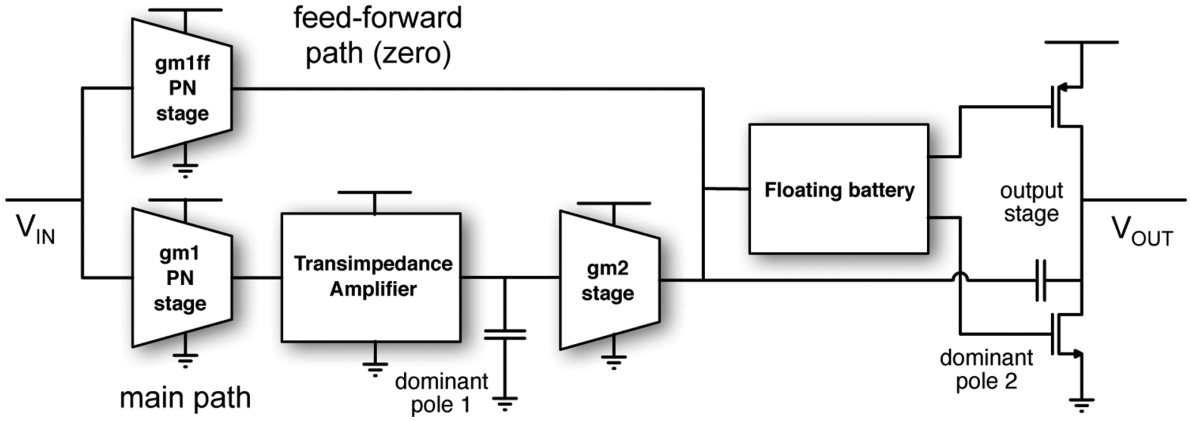

Fig. 17. BB op-amp diagram block scheme.

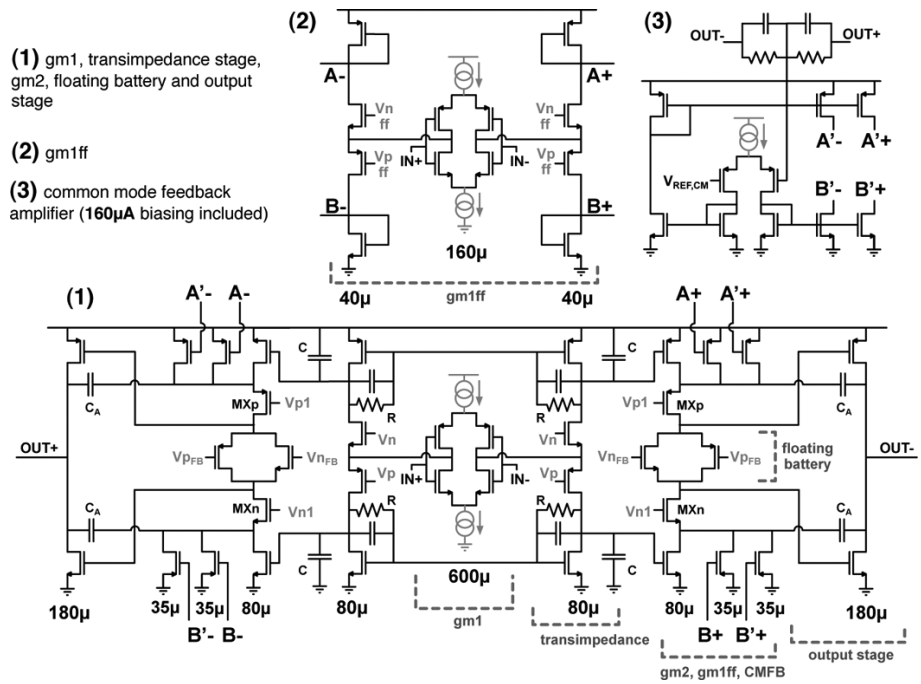

Fig. 18. BB op-amp MOS transistors simplified scheme.

plate. Finally some margin should be allowed to cover PAD and off-chip parasitic together with the differential probe input capacitance. It follows that a high OTA power consumption would be required to ensure system stability, since the nondominant pole is directly linked to the output capacitance. For a given OTA target bandwidth and a given capacitive load, to reduce the power consumption of the output stage, the Ahuja compensation technique can been exploited [27]. This gives, about 60% of current saving to push the nondominant pole at twice the OTA f_T (60 degrees phase margin), compared with a traditional Miller compensation. In addition, the right-hand-side zero is typical of a Miller amplifier is naturally avoided.

The operational amplifier detailed architecture is shown in Fig. 16. The main path is composed by the input complementary p-n stage (gm_1), a transimpedence amplifier based on the topology proposed by P. W. Li *et al.* [28] but driven in current from the source of the transistors, a second transconductance stage (gm_2), which feeds the output push pull stage (through a floating battery) [29], [30]. The feed-forward path is made by a simple transconductance stage (gm_{1ff}), which sums its current with the one of the main path in front of the class-AB common source output stage. This latter section embeds the Ahuja compensation loop.

The Rauch loop is designed to have more than 90-MHz bandwidth under all working conditions (GSM/UMTS, high/low gain) with $>$ 65 degrees phase margin and $>$ 14-dB gain margin. The $-40/-20$ dB per decade dual-slope approach gives the possibility to achieve 40–dB open-loop gain at 2 MHz (i.e., the edge of the UMTS band) and 75 dB at 200 kHz (i.e., the edge of the GSM low-IF band). Notice that, considering only the operational amplifier gain, these values are significantly higher (62 and 90 dB, respectively). The OTA equivalent input-referred noise resistance is 50 Ω with another 50Ω required to represent the flicker noise contribution (GSM).

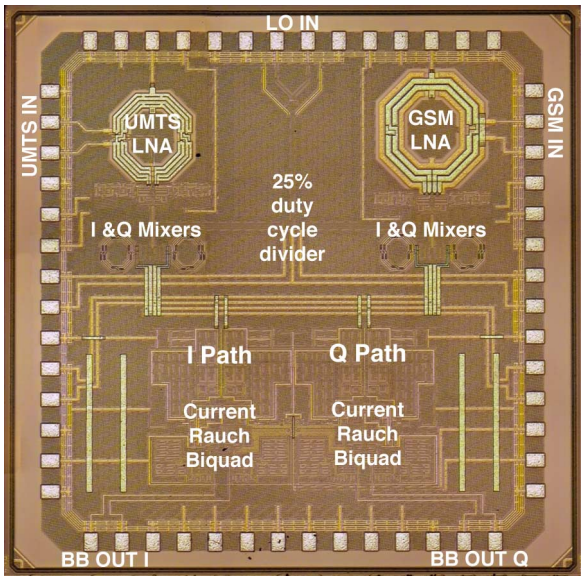

Fig. 19. Chip die photograph.

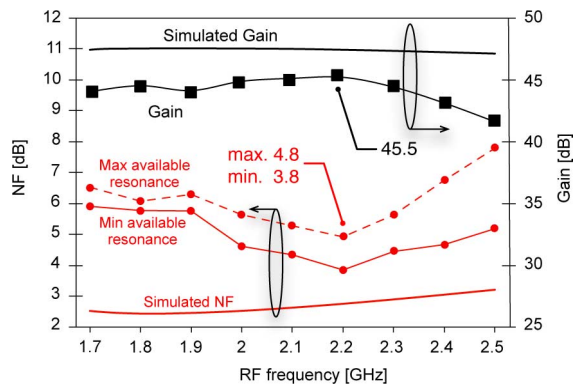

Fig. 20. Gain and NF from measurements and simulations of TDD receiver path.

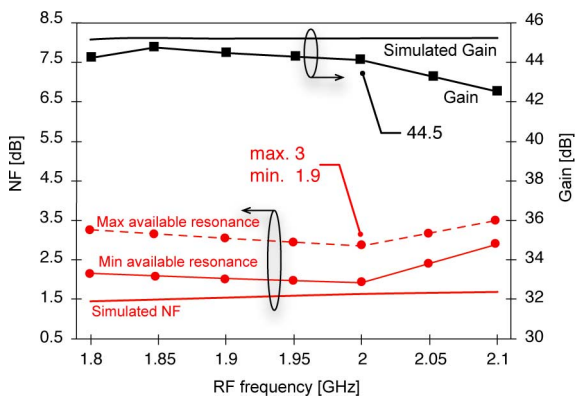

Fig. 21. Gain and NF from measurements and simulations of FDD receiver path.

VI. Prototype and Measurements

A chip prototype that includes two receivers was fabricated in 40-nm CMOS technology (Fig. 19). The two RF paths (SE and differential) share a common BB (I and Q) and a supply voltage of 1.8 V. The mixers are also used as switches to select the receiver path. The SE path implements the GSM standard, while the differential path implements the UMTS standard. As shown in Fig. 19, the GSM input transformer is bigger than the UMTS one due to the boosting coil. Thanks to its high resonance frequency, the resonator at the mixer output requires a small area (less than 5% of the entire receiver). The 25% duty-cycle divider, under a 1.2-V supply voltage, is also shared by two RX chains and is placed in the center of the die to optimize the LO distribution. The BB input capacitance is made of a differential part C_{1D} and a single-ended part C_{1SE} (Fig. 15).

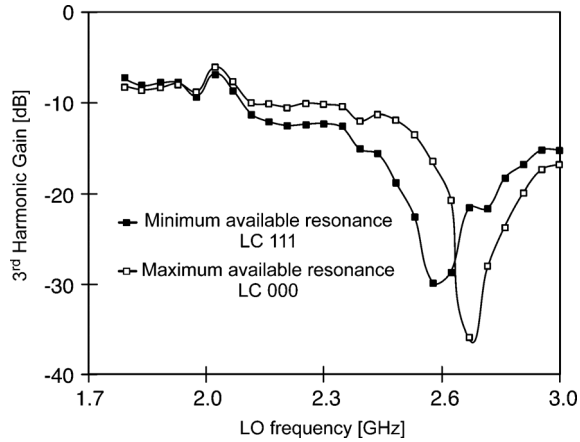

Fig. 22. TDD third-harmonic gain and resonant mixer tuning.

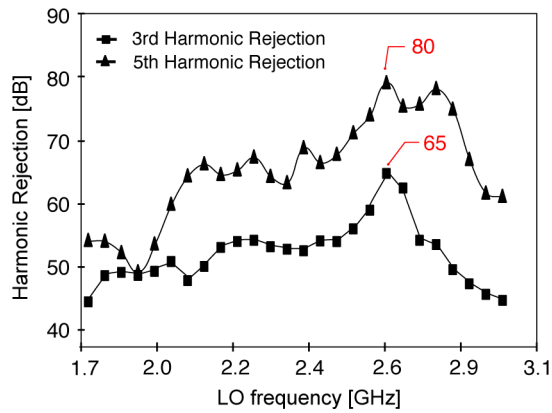

Fig. 23. TDD third and fifth harmonic rejection.

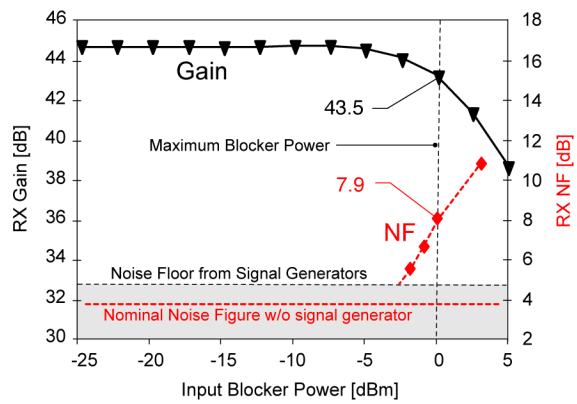

Fig. 24. TDD Gain and NF versus input blocker power.

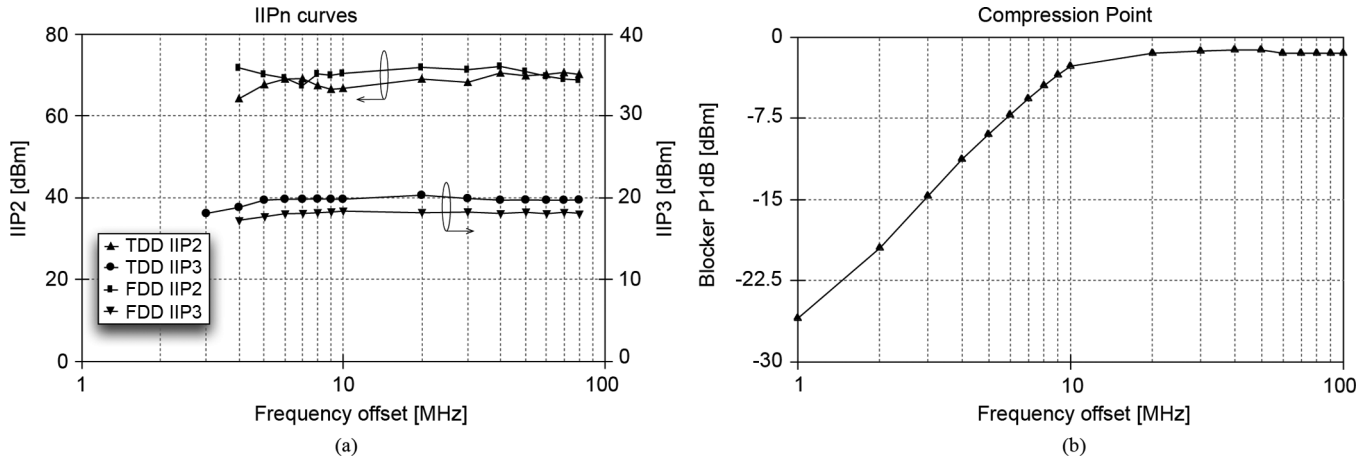

Fig. 25. Measured receiver linearity at $f_{\rm LO} = 2$ GHz. (a) Measured IIP2 using two-tones test ($f_1 = f_{\rm LO} + \Delta f$, $f_2 = f_{\rm LO} + \Delta f +$ 500 kHz) and measured IIP3 using two-tones test ($f_1 = f_{\rm LO} + \Delta f$, $f_2 = f_{LO} + 2\Delta f -$ 500 kHz). (b) Measured blocker $P_{1\ \rm dB}$ with blocker located at $f = f_{\rm LO} + \Delta f$.

TABLE I
COMPARISON WITH RECENTLY PUBLISHED SAW-LESS, BLOCKER TOLERANT RECEIVERS

	[15] Mizarei JSSC 2011	[21] I.S-C Lu ISSCC 2011	[11] Borremans JSSC 2011	[2] Murphy ISSCC 2012	This work (TDD)	This work (FDD)
RF Frequency [MHz]	850-950/1800-1900	850-950/1800-1900	400-6000	80-2700	1800-2400	1800-2100
RF input	Single Ended	Differential	Differential	Single Ended	Single Ended	Differential
Gain [dB]	77.8	60.7	70	70	45.5	44.5
Min in-band NF [dB]	3.1	2.9[1]	3.2[1]	1.9	3.8	1.9[1]
0dBm Blocker NF [dB]	11.4[2]	7[2]	15[3]	4.1[2]	7.9[3]	-
3rd/5th Harmonic Rejection HB	>40/N.A.	44/ N.A.	-	42/45	54/65	-
IIP3 [dBm]	>-12.4 (IB)	0 (IB)	10 (OB)	13.5 (OB)	>18 (OB)	>16 (OB)
IIP2 [dBm]	>45 (IB)	>44.3 (IB)	70 (OB)	54 (OB)	>64 (OB)[4]	>66 (OB)[4]
Active Area [mm^2]	2.4[5]	1.4	2	1.2	0.84	0.74
Supply Voltages [V]	1.3/2.7	2.8	1.1/2.5	1.3	1.2/1.8	1.2/1.8
Power Cons. [mW]	55[mA][5]	58.9 [mA][6]	38.9[7]	65[7]	32[7]	32[7]
LO divider current [mA]	N.A.	N.A.	N.A.	26 (2GHz)	6.4 (2GHz)	6.4 (2GHz)
CMOS technology	65nm	65nm	40nm	40nm	40nm	40nm

[1] An off-chip balun can results in an additional 1.2dB of NF degradation [2] 80MHz Blocker Offset
[3] 20MHz Blocker Offset [4] Measured from 3 samples [5] Including VCO and synthesizer
[6] Including ADC [7] Estimated at 2GHz given reported numbers

This capacitor is not tuned when changing the gain or the bandwidth simplifying the layout and increasing the capacitor density. Ninety-five percent of the equivalent BB input capacitance is contributed by C_{1D} (equal to 350 pF) while the remaining 5% by C_{1SE}. In this way the actual area is only 30% of that required by an entire single-ended solution. Using a M1–M5 MOM implementation, the area required by the input capacitance for the I (Q) path is about 500 $\times$ 300 μm^2 (50% of the I (Q) BB). The C_2 feedback capacitance value is modified from 20 pF to 28 pF passing from high-gain to low-gain mode. The resistance R_1 has nominal values of 250 and 100 Ω (GSM and UMTS, high-gain), while the resistance R_2 has nominal values of 7 and 3.5 kΩ (GSM and UMTS, high-gain).

Fig. 20 shows both measured and simulated gain and NF of the SAW-less receiver versus frequency. The minimum NF is 3.8 dB and is located at 2.2 GHz instead of the design value of 1.8 GHz (GSM standard) due to an error in the transformer design. From 2.1 to 2.3 GHz, the NF stays below 4.5 dB. Simulation shows that the mismatch between the resonance frequency of the primary and boosting coils (due to inaccurate EM simulations) causes an extra 1 dB of NF and approximately 1.4 dB of gain reduction. This conclusion is confirmed by the fact that, for the FD receiver, where resonance mismatch cannot exist thanks to the use of capacitive boosting, the measured 1.9-dB NF and 44.5-dB gain (with the resonant mixer tuned at the minimum possible frequency) are much closer to

simulations, as shown in Fig. 21. Fig. 21 shows both measured and simulated gain and NF of the FDD receiver versus frequency. The minimum NF is 1.9 dB and is located at 2 GHz; from below 1.8 to 2.05 GHz, the NF stays below 2.5 dB. All of the NF measurements were performed at 100-kHz IF.

Fig. 22 shows the third-harmonic gain versus LO frequency while tuning the resonance frequency of the mixer load at the maximum and at the minimum possible values. Since the mixer load resonance frequency, even at its minimum, is too high due to the inaccurate EM simulations the full potential of the technique cannot be exploited. However, at the wanted frequencies, a sizeable improvement in the harmonic rejection is still visible. Furthermore the same technique reduces LNA noise folding by the mixer improving NF as shown in Fig. 20. The 1 dB improvement is due to the fact that the spectrum of the LNA noise at the mixer output is not white but increases moving away from the RF band. In a similar way the resonant mixer improves the NF for the FDD receiver as shown in Fig. 21.

Fig. 23 shows third and fifth harmonic rejection versus $f_{\rm LO}$; 54 and 65 dB are measured at 2.2 GHz for TDD. The maximum achievable rejection is 65 and 80 dB, respectively, around 2.7 GHz, i.e., at the mixer load resonant frequency.

Fig. 24 shows NF and gain of the SE receiver as a function of the power level of an input blocker located at 20-MHz offset. Below -2 dBm, the noise floor of the signal generator used to supply the blocker dominates NF. At 0 dBm, which is the maximum blocker power defined by the standard, the NF reaches 7.9 dB. Notice, however, that this value is affected by the measurement setup. In this case, the dominant factor is the phase noise of the LO generator at 20-MHz offset which folds the in-band part of the blocker energy through reciprocal mixing. Gain compression at 0 dBm is only 1.4 dB, demonstrating the excellent dynamic range of the entire front thanks to the class-A/B LNA (no current slewing), the current-mode mixer, and the high-selectivity Rauch filter (no voltage clipping).

Fig. 25(a) shows the uncalibrated out-of-band IIP2 versus the position of the interferers for a typical sample. IIP2 is always above 64 dBm for both receivers and for all three measured samples from 3 MHz on. Fig. 25(a) also shows the IIP3 versus the position of the interferes. IIP3 is $>$ 18 and $>$ 16 dBm for the TDD and FDD receivers, respectively, for an offset frequency above 3 MHz. Fig. 25(b) shows the 1-dB compression point as a function of the blocker position for the TDD case. P1 dB is approaching -1.5 dBm above 20 MHz. All linearity measurements are taken setting the gain at its maximum and the resonance of the mixer load at the minimum available frequency as it is done for the minimum NF measurements. In both cases, the LNA consumes 9 mA, the BB consumes 4 mA, and the LO generation/distribution block consumes 6.5 mA at 2 GHz.

In Table I, we report the comparison with the other recently published SAW-less/blocker tolerant/noise-cancelling receivers.

VII. Conclusion

A wideband SE blocker-tolerant receiver suitable for use without a SAW filter in very demanding applications was described. The use of such a transceiver in high-end smart phones should give big savings in board size and overall BOM. Its key feature is the ability to meet very demanding specifications without requiring large power consumption and area while providing a very solid design thanks to the use of a differential signal path throughout the chip. The main limitation of the implemented prototype is a NF 1 dB higher than expected due to a combination of effects, which limits its use in high-end terminals. A redesign of the balun and of the LNA ground connection should produce an antenna sensitivity better than that of existing high-end transceivers. A fully differential transceiver suitable for FDD applications achieves almost 2 dB better NF with the same power consumption and 15% less area due to the simpler transformer.

References

[1] "Digital Cellular Telecommunications System (Phase 2+); Radio Transmission and Reception Eur. Telecommun. Standards Inst., (3GPP TS 45.005 Version 11.2.0 Release 11),, 2013.

[2] D. Murphy, H. Darabi, A. Abidi, A. Hafez, A. Mirzaei, M. Mikhemar, and M.-C. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2943–2963, Dec. 2012.

[3] W. Redman-White and D. M. W. Leenaerts, "$1/f$ noise in passive CMOS mixers for low and zero if integrated receivers," in *Proc. Solid-State Circuits Conf.*, 27, 2001, pp. 41–44.

[4] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Proc. IEEE Custom Integr. Circuits Conf.* , 2003, pp. 459–462.

[5] Z. Ru, E. A. M. Klumperink, G. Wienk, and B. Nauta, "A software-defined radio receiver architecture robust to out-of-band interference," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2009, pp. 230–231,231a.

[6] H. Khatri, L. Liu, T. Chang, P. Gudem, and L. Larson, "A saw-less CDMA receiver front-end with single-ended LNA and single-balanced mixer with 25 duty-cycle LO in 65 nm CMOS," in *Proc. IEEE Radio Frequency Integr. Circuits Symp.*, 2009, pp. 13–16.

[7] A. Mirzaei, H. Darabi, J. Leete, and Y. Chang, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. .

[8] M. Sosio, A. Liscidini, and R. Castello, "An intuitive current-driven passive mixer model based on switched-capacitor theory," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 60, no. 2, pp. 66–70, Feb. 2013.

[9] L. Franks and I. Sandberg, "An alternative approach to the realization of network transfer functions: The N-path filter," *Bell Syst. Tech. J.*, vol. 39, pp. 1321–1350, 1960.

[10] A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q n-path band-pass filters: Modeling and verification," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, May 2011.

[11] J. Borremans, G. Mandal, V. Giannini, B. Debaillie, M. Ingels, T. Sano, B. Verbruggen, and J. Craninckx, "A 40 nm CMOS 0.4-to-6 GHz receiver resilient to out-of-Band blockers," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1659–1671, Jul. 2011.

[12] Z. Ru, N. Moseley, E. A. M. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-Band interference," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3359–3375, Dec. 2009.

[13] M. Soer, E. A. M. Klumperink, Z. R. F. V. Vliet, and B. Nauta, "A 0.2-to-2.0 GHz 65 nm CMOS receiver without LNA achieving $>$ 11 dBm IIP3 and $<$ 6.5 dB NF," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2009, pp. 222–223,223a.

[14] C. Andrews and A. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.

[15] A. Mirzaei, H. Darabi, A. Yazdi, Z. Zhou, E. Chang, and P. Suri, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *Solid-State Circuits, IEEE J. of*, vol. 46, no. 4, pp. 950–964, 2011.

[16] I. Lu, C.-Y. Yu, Y.-H. Chen, L.-C. Cho, C. Sun, C.-C. Tang, and G. Chien, "A SAW-less GSM/GPRS/EDGE receiver embedded in a 65 nm CMOS SoC," in *Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 364–366.

[17] J. Borremans, G. Mandal, V. Giannini, T. Sano, M. Ingels, B. Verbruggen, and J. Craninckx, "A 40 nm CMOS highly linear 0.4-to-6 GHz receiver resilient to 0 dBm out-of-band blockers," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 62–64.
[18] B. Razavi, *RF Microelectronics*. Upper Saddle River, NJ, USA: Prentice-Hall PTR, 1998.
[19] X. Li, S. Shekhar, and D. Allstot, "GM-boosted common-gate LNA and differential colpitts VCO/QVCO in $0.18-\mu\mathrm{m}$ CMOS," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2609–2619, Dec. 2005.
[20] J. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, Sep. 2000.
[21] C.-Y. Yu, I. Lu, Y.-H. Chen, L.-C. Cho, C. Sun, C.-C. Tang, H.-H. Chang, W.-C. Lee, S.-J. Huang, T.-H. Wu, C.-S. Chiu, and G. Chien, "A SAW-less GSM/GPRS/EDGE receiver embedded in 65-nm SoC," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 3047–3060, Dec. 2011.
[22] B. Razavi, K. Lee, and R. Yan, "Design of high-speed, low-power frequency dividers and phase-locked loops in deep submicron CMOS," *IEEE J. Solid-State Circuits*, vol. 30, no. 2, pp. 101–109, Feb. 1995.
[23] M. Sosio, A. Liscidini, and R. Castello, "A 2G/3G cellular analog baseband based on a filtering ADC," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 4, pp. 214–218, Apr. .
[24] A. Pirola, A. Liscidini, and R. Castello, "Current-mode, WCDMA channel filter with in-band noise shaping," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1770–1780, Sep. 2010.
[25] J. G. F. D. Bernardinis, C. Tinella, A. Milani, J. Pan, P. Uggetti, M. Sosio, S. Dai, S. Tang, G. Cesura, G. Gandolfi, V. Colonna, and R. Castello, "A 40 MHz-to-1 GHz fully integrated multistandard silicon tuner in 80 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. , pp. 162–164.
[26] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue, and E. Romani, "A 20-mW 640-MHz CMOS continuous-time ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641–2649, Dec. 2006.
[27] B. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-18, no. 6, pp. 629–633, Dec. 1983.
[28] P. Li, M. Chin, P. Gray, and R. Castello, "A ratio-independent algorithmic analog-to-digital conversion technique," *IEEE J. Solid-State Circuits*, vol. SSC-19, no. 6, pp. 828–836, Dec. 1984.
[29] K. D. Langen and J. Huijsing, "Compact low-voltage power-efficient operational amplifier cells for VLSI," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1482–1496, Oct. 1998.
[30] R. Hogervorst, J. P. Tero, R. G. H. Eschauzier, and J. Huijsing, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.

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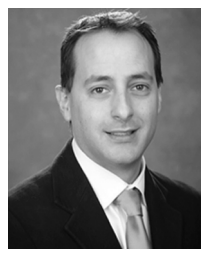

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