A 2-D GRO Vernier Time-to-Digital Converter with Large Input Range and Small Latency

Ping Lu[1], Pietro Andreani[1], and Antonio Liscidini[2]

[1] EIT Department, Lund University, Sweden; [2] University of Toronto, Canada

Abstract **— The proposed time-to-digital converter (TDC) arranges two Vernier gated-ring-oscillator (GRO) branches in a 2-dimension (2-D) fashion. All delay differences between X phases and Y phases can be used, rather than only the diagonal line. The large latency time inherited from Vernier structure is therefore dramatically reduced. The TDC is implemented in a 90nm CMOS process and consumes 1.8mA from 1.2V. The measured input range can safely cover a full period of a 50MHz sampling signal. With the same delay elements, the latency time is less than 1/6 of that needed in a standard Vernier TDC.**

Index Terms **— GRO, Vernier, Time to digital converter, 2-D.**

I. Introduction

Time-to-digital converters have been a hot research topic over a few years. However, the time resolution provided by self-loaded inverters does not always satisfy all TDC requirements, and thus different kinds of solution based on Vernier algorithm and noise-shaping were investigated.

A classic Vernier TDC improves the time resolution by using two delay lines with different inverter delays [1]. The effective time resolution is given by the difference of two delays, which can be designed much smaller than a single inverter delay. However, in traditional Vernier architecture, the number of stages grows exponentially with the number of bits and results in an increased sensitivity to device mismatch and a large latency.

Noise shaping is another method of increasing the effective TDC resolution [3]. In a GRO TDC, each new measurement starts from the TDC state at the end of the previous measurement, rather than discarding it. Thus, both the delay mismatch and the quantization error experience a first-order noise shaping, leading to an improvement in effective resolution and linearity. However, the raw (i.e., unshaped) resolution in GRO TDC is still limited by an inverter delay.

A GRO-based Vernier TDC (GVTDC) combining the Vernier approach with a GRO manner has therefore been proposed in [4]. As shown in Fig.1 (a), two delay lines in linear Vernier architecture are replaced by two GROs, which can achieve both a high raw resolution and a first-order frequency shaping of the quantization noise.

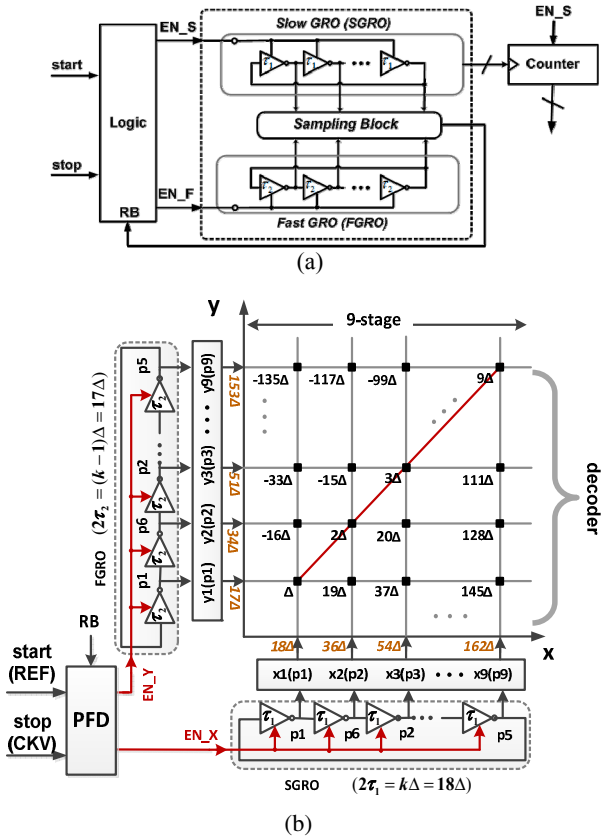
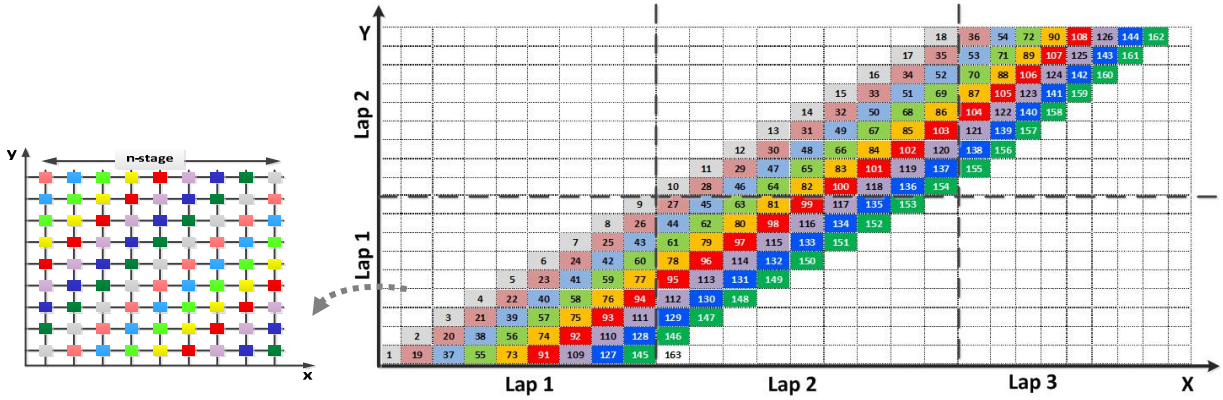


Fig. 1 (a) 1-D GVTDC; (b) 2-D GVTDC.

However, as in other Vernier TDCs, the long latency limits the detection range and highest sampling frequency.

The TDC proposed in this paper introduces a 2-D approach [2] to GVTDC, i.e., the two delay lines in a 2-D TDC [2] are replaced by two GROs (Fig.1 (b)). Unlike the GVTDC in [4], the 2-D Vernier TDC not only achieves a very low time quantization beyond the inverter delay, but also reduces dramatically the output latency time; equivalently, this TDC can greatly extend the detection range for a given sampling frequency.

An overview of the paper is as follows. Section II describes the proposed the 2-D GVTDC. Section III details the circuit implementation. Section IV gives the analytical and measurement results. Conclusions are drawn in Section V.



(a) (b)

Fig. 2 The 2-D Vernier plane: (a) GRO; (b) phase spread in time.

II. GRO-BASED 2-D VERNIER TDC

A. Principle of 2-D Vernier

To explain the concept of the proposed 2-D GVTDC, Fig. 1(b) illustrates a Vernier-plane that is composed of a 9-stage slow-delay GRO (*SGRO*) and a 9-stage fast-delay GRO (*FGRO*), with the inverter delay time τ_1 and τ_2, respectively. It should be noted that only the rising edge of the GRO phases is used for sampling, in order to avoid the mismatch between rise and fall time.

The plane XY is arranged into a vector to obtain an ordered set of time references with a constant quantization step Δ. As shown in Fig. 1(b), the operation in the Vernier plane is performed by a function $i = i(x, y) \in \mathbb{N}$, which associates the position i in the vector with the coordinates (*x, y*). It is noted that the values of *x* and *y* are limited between 1 and 9, due to the ring operation of the GROs. For convenience, let us first consider *x* and *y* with an infinite range (e.g. in Fig. 2(b)). According to [2], we obtain

$$\begin{cases} X_{inf}(i) = i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot (k-1) \\ Y_{inf}(i) = i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot k \end{cases} \quad (1)$$

where X_{inf} and Y_{inf} represent the absolute taps of *SGRO* and *FGRO* delay, respectively, and $\lfloor a \rfloor$ is the integer number smaller or equal to *a*. Then, considering the ring operation of the 9-stage GRO (Fig.2 (a)), (1) can be rewritten with modulo-9 operations, yielding

$$\begin{cases} X(i) = \mathrm{mod}\{X_{inf}(i), 9\} = \mathrm{mod}\{i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot (k-1), 9\} \\ Y(i) = \mathrm{mod}\{Y_{inf}(i), 9\} = \mathrm{mod}\{i - \left\lfloor \dfrac{i-1}{k} \right\rfloor \cdot k, 9\} \end{cases} \quad (2)$$

As mentioned in [2], $Y_{inf}(i)$ is periodic and limited between *0* and *k*. In our case, *k* is twice as large as the modulo operator, i.e. k=18. It indicates, for the Y axis, that the needed maximal lap number is 2, as shown in Fig.2 (b). The number of laps, combined with the coordinates *(x,y,)* determines the TDC output (in the same way as in the 3-D Vernier Ring TDC presented in [5]).

In Fig. 2, all the positions in the 9×9 delay matrix are used, resulting in an unbroken series of consecutive integer numbers (TDC outputs). For 3 *SGRO* (X-axis) laps (~2.34ns latency), the proposed TDC covers more than $\pm$ 800ps without any gap in the detection code. In [2] and [5], only partial matrix positions are utilized, which actually wastes some detection range. As shown in Fig. 2, to cover a normalized range of 162, [2] needs 162 sampling units (the whole colored area) in the plane. An input that is larger than 162 (e.g. 163) cannot be detected in such a 2-D Vernier TDCs, but is easily obtained in our 9×9 matrix within the given latency.

B. Principle of GRO operation

Two GROs are implemented as the delay lines in Vernier plane. During the TDC operation, when *FGRO* catches up with *SGRO*, the state of both GROs is frozen by falling *EN_X/EN_Y*. The capacitor at each *SGRO*/*FGRO* mode holds the voltage value at the freezing instant, and during the next measurement cycle, each GRO starts from this state. In this way, the quantization error is accumulated across all measurement, resulting the first-order quantization noise shaping.

III. CIRCUIT IMPLEMENTATION

The complete TDC includes the 2-D GRO core, a phase frequency detector (PFD), and a decoder [6]. The PFD senses the time difference between two inputs *start* and *stop* and generates two enable pluses *EN_X* and *EN_Y*

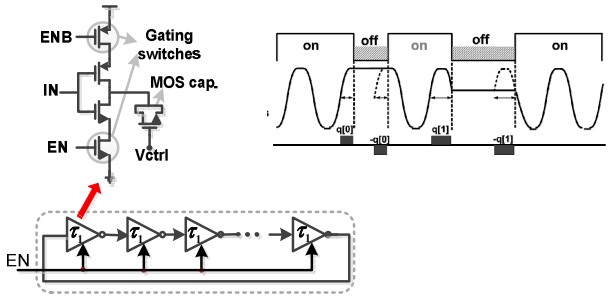


Fig. 3 GRO cell and gating behavior.

controlling the gating switches in *SGRO* and *FGRO*, respectively. The quantized delay generated by the two GROs is then read out by the decoder.

A. GRO Core

The GRO core is composed of two GROs and a matrix of comparators. As illustrated in Fig.3, the delay cells include also 2 gating switches that turn the ring oscillator into a GRO [3]. When both gating switches are on, *SGRO* and *FGRO* are running like regular ring oscillators; when they are off, *SGRO* and *FGRO* hold the state, as illustrated in the right of Fig.3.

The sampling block (9×9 D flip-flop matrix in the Vernier plane) determines when FGRO catches up with SGRO. For a high-resolution TDC, a narrow metastability region is necessary, and for this reason a modified sense-amplifier-based flip-flop is adopted [7]. The flip-flop eliminates the big mismatch between D-to-Q and CLK-to-Q delays, which appears as a large time offset in the comparator (flip-flop). By using the new comparators, the TDC detection range is greatly improved compared to [4] and not limited by the sampling units.

B. Phase frequency detector

GVTDC works properly only if EN_X always leads EN_Y. In order to guarantee the condition, the adaptive PFD of Fig. 4 is used. It generates an EN_X always leading EN_Y, regardless of the phase relation between start and stop. The PFD makes use of two true-single-phase-clock flip-flops having an always-high internal "D" input, and of an SR latch used as an arbiter. When start is leading, EN_X corresponds to start, while when stop is leading, EN_X corresponds to stop. A sign signal can be sent out indicating a positive or negative phase error.

The device propagation time (gating delay) in the feedback path allows both GROs to continue running even when one FGRO phase has already caught up with one SGRO phase, as illustrated in the upper-left of Fig.4. If the delay amount is large, a faulty sampling may occur in the next measurement. A simple modification, inserting

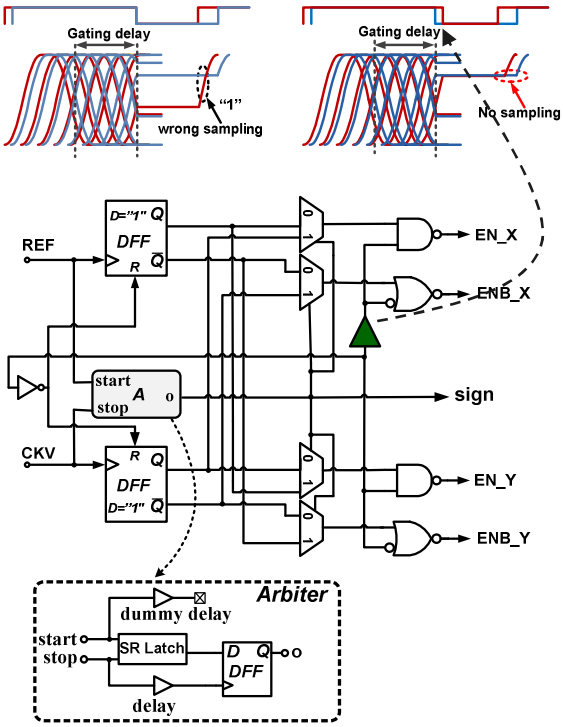


Fig. 4 Adaptive phase frequency detector.

a delay in the EN_X falling-edge path, mitigates this issue (upper-right of Fig.4).

C. Decoder

As previously stated, the decoder uses the lap number and the relative address to calculate the TDC output. However, in most DPLL applications the TDC input range is just one or a few DCO periods, which are usually safely contained in the colored parallelogram of Fig.2 (b). For this special case, a simple multi-phase counter (refer to [4]) combined with a column selector can realize the decoding.

IV. Implementation Results

A. Non-ideal factors

It is well-known that the variable starting phases in a GRO TDCs can scramble the spurious tones due to nonlinearity and convert them to noise. However, if the absolute delays of SGRO/FGRO are very large (e.g. τ_1, $\tau_2 >> \Delta$), the absolute mismatch is also bound to be large, compared to the Vernier resolution Δ.

Fig.5 gives the spectrum of the simulated TDC output in presence of different amounts of delay mismatches. When the delay difference between SGRO and FGRO cells is close to the raw Vernier resolution, the in-band noise floor is highly degraded. This may be a severe issue in GVTDC design.

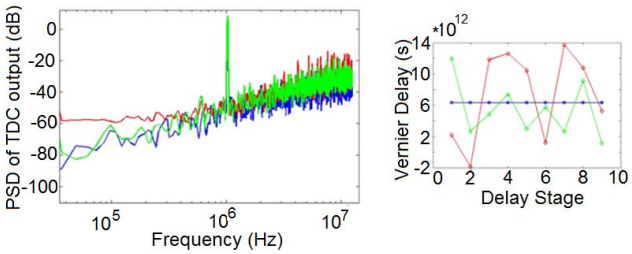


Fig.5 PSD of TDC output in presence of delay mismatches

A straightforward solution to this issue is to adopt small absolute delays for both GROs; in this case, however, a second non-ideal effect, i.e. charge redistribution, will have an increasingly adverse impact resulting in additional white noise at lower frequencies.

B. Measurements

The 2-D GVTDC has been implemented in a 90nm standard CMOS process. Fig.6 shows the chip photograph, where the active area is 0.22mm·0.20mm. A 50MHz reference (sampling) clock is used.

The SGRO has a unit delay of ~90ps (18Δ), and the FGRO has a unity delay of ~85ps (17Δ). The raw resolution is therefore ~5ps. Assuming an oversampling ratio (OSR) of 16, the in-band quantization noise obtained from transistor-level simulations is equivalent to what would be obtained from a noise-shaping-less Vernier TDC with a 1.9ps raw resolution [6].

The measured prototype does show a very good shaping at higher frequencies, as clear from Fig. 7. However, the in-band noise suffers from a high white noise floor, which deteriorates the equivalent TDC resolution to ~15ps. Considering that charge redistribution alone cannot deteriorate the equivalent resolution beyond the value of the raw resolution (assuming all memory of the GRO state is lost), device mismatch is the likely major culprit of such a performance deterioration (Fig.5), although the high bond-wire inductances may also play a role (which, however, is impossible to simulate with good accuracy). The 2-D GVTDC can work with a very large input range, only limited by the reference period. The needed latency time for ±800ps detection range is only 2.34ns, which is far lower than in a regular Vernier TDC (14.4ns).

Working with a 50MHz sampling frequency, the TDC consumes a current of 1.8mA from 1.2V.

V. CONCLUSIONS

We have presented a GRO-based Vernier TDC working in a 2-D fashion. The TDC displays a first-order shaping of the quantization noise, with a latency time that is only 1/6 of that of a standard Vernier TDC.

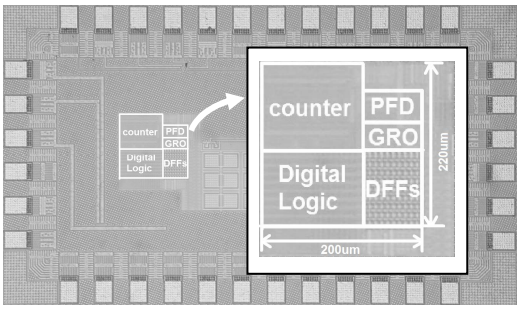


Fig.6 Die photo of proposed 2-D GVTDC

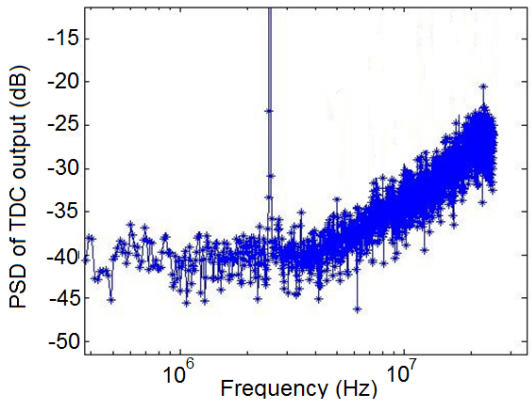


Fig. 7 Measured PSD of TDC output.

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