

An Intuitive Analysis of Phase Noise Fundamental Limits Suitable for Benchmarking LC Oscillators

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Abstract—An intuitive yet sufficiently accurate formulation of the phase noise of various commonly used oscillators, including most types of class-B (standard, AC-coupled and with tail filter) and class-C, is derived and used to compare their fundamental limitations. A noise factor that represents the difference between the maximum achievable Figure of Merit and the actual one is derived for all topologies considered. Measurements on a dedicated chip prototype that integrates two high performance topologies allow to verify, in an unbiased way, the accuracy of the predictions. A very good agreement between the model and both simulation and measurement is obtained.

Index Terms—Class-B, class-C, class-F, CMOS integrated circuits, excess noise factor (ENF), figure of merit (FoM), GSM, impulse sensitivity function, low-noise, phase noise, radio frequency integrated circuits, voltage controlled oscillators, wide tuning range oscillators.

I. INTRODUCTION

MODERN communication systems need clocks with very low phase noise and/or jitter. To minimize phase noise for a given power consumption, integrated oscillators often use as load a high-Q LC-tank. Through the years, integrated LC oscillators have improved as a result of technology and/or topologies evolution, however, it is not always easy to ascertain the dominant reason of such improvements. In the past, following the pioneering work of Leeson [1], authors have analyzed oscillators either in a rigorous mathematical way or using a simpler yet accurate linear time variant (LTV) approach [2]–[7] but generally preferring rigor to intuitiveness. The goal of this paper is to determine the ultimate performance limit for some of the most used LC oscillator topologies, combining reasonable accuracy with intuitiveness. In addition, the theory is experimentally verified in a rigorous and objective way comparing two high performance topologies in exactly the same operating conditions, i.e., technology, Q of the tank, dividers, etc.

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In the following, LC oscillators are classified as it is done for power amplifiers, considering negative resistance implemented with NMOS, PMOS or complementary PMOS-NMOS transistors, assuming an arbitrary gain between the tank and the active devices and that the bias current is supplied from the positive rail. No voltage-biased oscillators are considered. To compare different architectures we rely on a well-accepted figure of merit (FoM) [8]. Furthermore, we normalize the phase noise to the ultimate limit through a very useful parameter called excess noise factor (ENF) [9]–[11]. In the derivation of the FoM for the different topologies, $1/f$ noise is neglected and only differential topologies are considered (for their many advantages, e.g., exact 50% duty cycle, reduced cross talk, etc.). Notice that a differential Colpitts oscillator is a special case of a negative resistance one and therefore is included in this analysis [12]. Finally, we are not considering the impact of tuning the oscillator center-frequency (which is key for voltage-controlled oscillators, VCOs) due to space limitations, but in the experimental verification, wide tuning range oscillators are considered. The paper is organized as follows. Section II lists the oscillators considered in this work, i.e., those for which the tank is not loaded by the active devices, derives their phase noise and FoM, using some simplifying assumptions, and introduces the concept of ENF. Section III compares the different topologies in term of ENF and defines the two most promising ones from fundamental arguments. Section IV experimentally compares these topologies using a specially designed test bench. Finally, Section V draws some conclusions and indicates possible future works.

II. PHASE NOISE IN LC-TANK OSCILLATORS

The conceptual schematic of an LC-oscillator is shown in Fig. 1, where the LC-tank losses are represented by $R_T = Q/(\omega_0 C)$ and the active components by an energy-restoring block. According to the LTV theory of Hajimiri and Lee [3], the conversion of noise into phase noise is described by the impulse sensitivity function (ISF) Γ . The ISF defines the effect of noise on the oscillation phase and is a function of the phase of the tank voltage. The general expression for the phase noise is:

$$L_T(\Delta\omega) = 10 \text{Log} \left[\frac{4kT}{P_{\text{RF}}} (\Gamma_{T,\text{rms}}^2 + \Gamma_{M,\text{rms}}^2 \alpha) \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \quad (1)$$

where $P_{\text{RF}} = A_0^2/(2R_T)$ is the power dissipated in the tank, α is a noise factor that includes γ_{MOS} and attenuation between tank and MOS gates, $\Gamma_{T,\text{rms}}$ and $\Gamma_{M,\text{rms}}$ are the rms ISF for R_T

and the MOS transistors and no other noise source is considered. The ratio between RF power in the tank P_{RF} and the DC power P_{DC} , called power efficiency η_P , is expressed in terms of voltage and current efficiencies [13] η_I and η_V as:

$$\eta_P = \frac{P_{\text{RF}}}{P_{\text{DC}}} = \frac{I_{\text{RF}} V_{\text{RF}}}{I_{\text{DC}} V_{\text{DC}}} = \eta_I \eta_V \quad (2)$$

where I_{RF} and V_{RF} are the rms values of the fundamental components of current and voltage across R_T , V_{DC} , and I_{DC} are the supply voltage and current. Using (2) into (1), the oscillator's phase noise becomes:

$$L(\Delta\omega) = 10 \text{Log} \left[\frac{4kT}{P_{\text{DC}}} \frac{\Gamma_{T,\text{rms}}^2 + \Gamma_{M,\text{rms}}^2 \alpha}{\eta_P} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right]. \quad (3)$$

Different oscillators are compared in terms of a FoM [8] that normalizes the phase noise to the oscillation frequency ω_0 , the offset frequency $\Delta\omega$ and the power dissipation (expressed in mW or dBm):

$$FoM = -10 \log \left[L(\Delta\omega) P_{\text{DC},\text{mW}} \left(\frac{\Delta\omega}{\omega_0} \right)^2 \right]. \quad (4)$$

Using (3) into (4) leads to the following handy expression:

$$\begin{aligned} FoM &= -10 \log \left[\frac{kT (\Gamma_{T,\text{rms}}^2 + \Gamma_{M,\text{rms}}^2 \alpha)}{10^{-3} Q^2 \eta_P} \right] \\ &= 173.8 \text{ dBc/Hz} + 10 \log \left[\frac{\eta_P Q}{\Gamma_{T,\text{rms}}^2 + \Gamma_{M,\text{rms}}^2 \alpha} \right]. \end{aligned} \quad (5)$$

Assuming that the oscillation voltage is nearly sinusoidal and that the energy restoring element drives the tank from a high impedance, the ISF for R_T is a sinusoid in quadrature with the tank voltage giving $\Gamma_{T,\text{rms}}^2 = 1/2$ [3]. To improve the FoM we can act on three fronts. First the tank Q, getting 6 dB for every doubling of it. Second, on the power efficiency, getting only 3 dB for every doubling of it. Third, on the ISF and excess noise factor of the transistors. Assuming 100% power efficiency, noiseless transistors and no other noise contribution, the FoM, called FoM_{MAX} , becomes:

$$\begin{aligned} FoM_{\text{MAX}} &= -10 \log \left[\frac{kT}{2 \cdot 10^{-3} Q^2} \right] \\ &= 173.8 \text{ dBc/Hz} + 10 \log (2Q^2). \end{aligned} \quad (6)$$

FoM_{MAX} is a thermodynamic limit associated with the noise and power dissipation of the unloaded tank. Expressing the actual FoM in terms of FoM_{MAX} gives the excess noise factor (ENF) [10]:

$$\text{ENF} = FoM_{\text{MAX}} - FoM = 10 \log \left[\frac{2 (\Gamma_{T,\text{rms}}^2 + \Gamma_{M,\text{rms}}^2 \alpha)}{\eta_P} \right]. \quad (7)$$

The ENF defines the distance from the ultimate limit. The same concept was proposed by van der Tang and Kasperkovitz

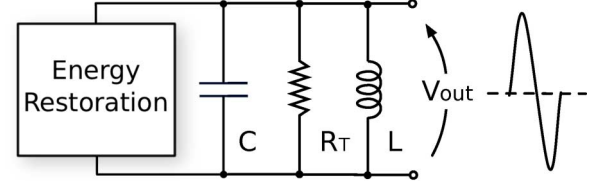


Fig. 1. Generic LC oscillator.

[10] putting $F = 1$ into the Leeson expression and assuming 100% efficiency, rigorously derived by Bank [9] using an ISF approach and by Murphy *et al.* using a phasor approach [7].

If the transistor current noise power spectral density is proportional to the derivative of the drain current with respect to the gate voltage $\Gamma_{M,\text{rms}}^2 = 1/2$ [9], [12] and for a direct coupling between tank and transistors, the excess noise factor α is just γ_{MOS} . Using this result into (5) and (7) gives:

$$\begin{aligned} FoM &= -10 \log \left[\frac{2kT}{10^3 Q^2 \eta_P (1 + \gamma_{\text{MOS}})} \right] \\ &= 173.8 + 10 \log \left[\frac{2\eta_P Q^2}{1 + \gamma_{\text{MOS}}} \right], \end{aligned} \quad (8)$$

$$\text{ENF} = 10 \log \left[\frac{1 + \gamma_{\text{MOS}}}{\eta_P} \right]. \quad (9)$$

More generally, α is proportional to the inverse of the voltage gain between tank and active devices. In Colpitts oscillators, this factor is larger than one due to capacitance partition from drain to gate, while using transformer coupling the factor can be either larger or smaller than one.

VCO topologies mimic those of RF power amplifiers (PAs). We analyze VCOs for which the load is naturally represented by a parallel resonator and the active devices by a Norton equivalent [14]. This includes class B, C, and F. These topologies are the most commonly used, although some recently proposed ones cannot be included in the model, e.g., ‘‘Clip and Restore’’ and class-D [15], [16].

The ENF of published oscillators [17]–[32], grouped by topology, is plotted in Fig. 2 versus tank Q. These data indicate no clear winner and a very large spread within the same architecture, although class-B with tail filter and class-C are the closest to the limit (also Colpitts, which can be however assimilated to a class-C [12]). Second order effects often dominate and the reported tank Q can be inaccurate (e.g., in [17] FoM and Q are inconsistent as pointed out in [10] and this data is not considered in Fig. 2). The difficulty with extracting the tank Q, together with the high sensitivity of phase noise to Q, limits the ability to assess the potential of a new topology. Because of this, we have built a test chip to compare different topologies in the exact same operating conditions. In the following we determine the minimum achievable ENF for the oscillators satisfying (8), showing that the only differentiator is efficiency, which is maximized maximizing η_I and voltage swing. However, the following three aspects should be considered. First, the voltage drop across the bias current source, V_B , degrades efficiency by $1 - V_B/V_{\text{DD}}$. Second, the bias transistors contribute to phase noise in a topology dependent way. Third, in some cases there

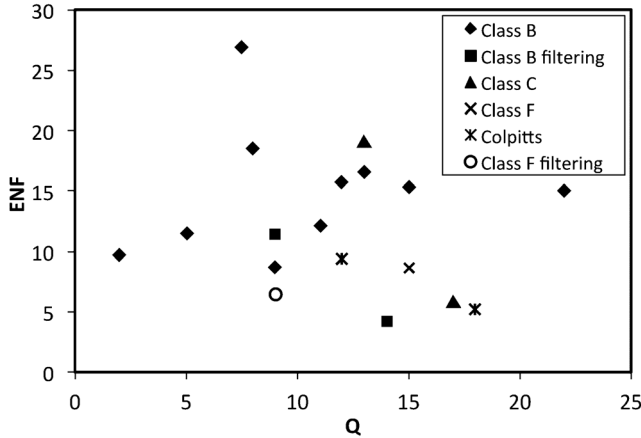


Fig. 2. Benchmarking of different oscillator topologies using ENF.

is a maximum voltage swing beyond which the active devices load the tank causing $\Gamma_{M,rms}^2$ to increase.

III. DIFFERENT OSCILLATOR TOPOLOGIES

A. Class-B Oscillators

For the class-B oscillator, the shape of the tank current can be approximated as in Fig. 3(a) assuming negligible parasitic capacitance at the tail current generator. The rms fundamental component of the RF current is $\sqrt{2/\pi} I_{DC}$ and η_I is $\sqrt{2/\pi}$. Due to the tail current source, the active devices do not load the tank even when they enter the triode region. Therefore, the maximum η_V occurs at the maximum achievable swing and is equal to $\sqrt{2(1 - V_B/V_{DD})}$. This gives an η_P of $2/\pi(1 - V_B/V_{DD})$. For the complementary class-B oscillator of Fig. 3(b) the shape of the tank current is shown in the figure. In this case the fundamental component of the RF current is $2\sqrt{2/\pi} I_{DC}$, and η_I is $2\sqrt{2/\pi}$. On the other hand, since the voltage cannot exceed the supply, the maximum η_V is equal to $(1 - V_B/V_{DD})/\sqrt{2}$. This gives an η_P of $2/\pi(1 - V_B/V_{DD})$, a result valid for both N-only and P-N implementations since η_V is twice for the former and η_I is twice for the latter, giving the same η_P . Andreani and Fard [33] and Murphy *et al.* [7] have shown that for a p-n oscillator (8) and (9) are valid only if the tank is floating otherwise the phase noise is degraded.

The ENF of an ideal class-B oscillator, calculated using (9), is uniquely defined by η_V and its minimum is $10 \log[(\pi V_{DD})/(2(V_{DD} - V_B)(1 + \gamma_{MOS})]$, where $(V_{DD} - V_B)$ is the maximum possible swing. Two important non-idealities however exist. First, the current source contributes phase noise proportionally to its gm , suggesting to increase V_B . This sets a trade-off between minimum additional noise and maximum η_V . Second, due to the tail parasitic capacitance, when the switching transistors are in the triode region they load the tank, contributing extra noise. Therefore, as the swing increases, there is an additional trade-off between efficiency and noise that limits the achievable FoM, making the minimum ENF much larger than 3 dB. Consider as an example the circuit of Fig. 3(a) with a tank Q of 15 and $V_{DD} = 1.5$ V. Simulations give a minimum ENF above 10 dB. This is due to an η_P of 29% (giving $10 \log(1/0.29) = 5.4$ dB loss), mainly due to the voltage drop

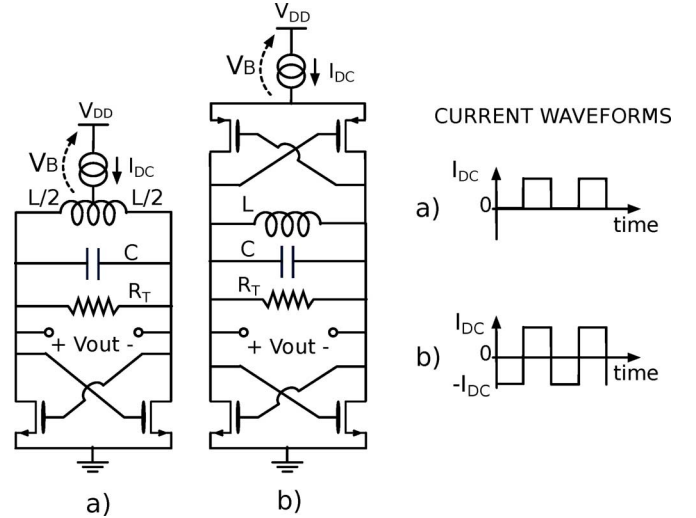


Fig. 3. NMOS (a) and complementary MOS (b) “class-B” LC oscillators.

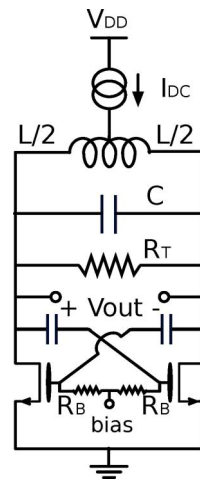


Fig. 4. AC-biased class-B oscillator (NMOS only).

on current source, a tail transistor noise 5% of the total and a switching MOS noise, enhanced by the tail parasitic capacitance, 61% of the total (giving $10 \log(1/(1 - 0.66)) = 4.7$ dB loss).

One way to improve efficiency is to use AC coupling to control V_B by forcing a DC voltage drop on the capacitor connected between the drain and gate of the switching transistors as shown in Fig. 4 (for simplicity Fig. 4 and the followings with AC coupling represent only conceptual schematics where the circuit that set the DC bias is not shown). While η_I is not improved, the extra degree of freedom allows to improve η_V and therefore ENF (e.g., for the previous example by about 1.5 dB).

B. Class-B Oscillators With Tail Filter

Most of the above limitations can be overcome placing an additional LC-tank, resonating at $2\omega_0$, at the tail of a class-B oscillator [34]. Three advantages are obtained. First, the common source node can swing below ground, increasing the maximum η_V . Second, the switching transistors can enter the triode region without loading the tank since they see a high impedance in series with them. Third, the noise of the current source around

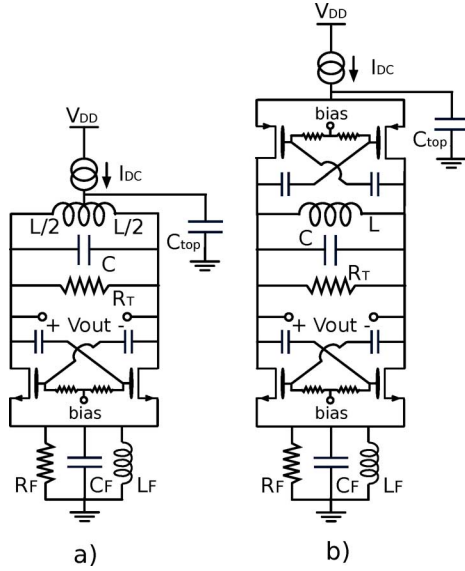


Fig. 5. Oscillators with second-harmonic LC tail filter.

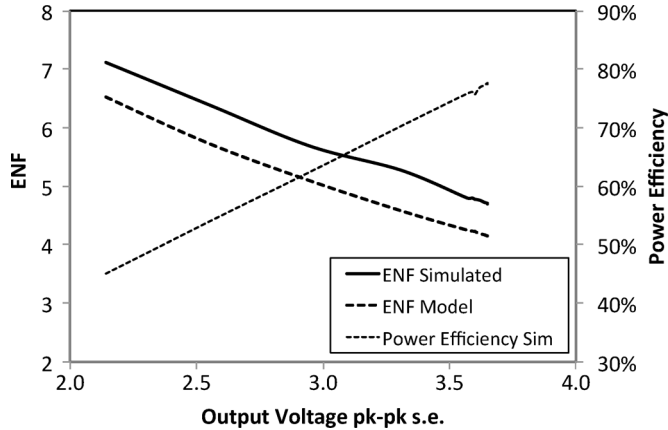


Fig. 6. Class-B oscillator with tail filter: calculated and simulated ENF and simulated power efficiency.

$2\omega_0$ can be filtered with a large capacitance C_{top} . The presence of an extra tank within the circuit creates an additional state variable and the ISF needs to be computed with a more complex approach [2]. In actuality, simulation shows that if the impedance of the tank is sufficiently high, (8) still describes the new topology in a sufficiently accurate way.

The best ENF is reached using the tail tank with an AC-coupled class-B oscillator as shown in Fig. 5(a). In this case, although the shape of the tank current is no longer a square wave (due to the presence of C_{top} that allows large spikes of current from the supply), η_I is still remarkably close to $\sqrt{2}/\pi$ up to the maximum achievable voltage swing. Ideally η_P would reach 100% for a differential swing of πV_{DD} peak ($V_B = 0$), giving a minimum ENF of 3 dB (if $\gamma_{MOS} = 1$). In reality, simulation results (Fig. 6) give a maximum η_P close to 80%. Extrapolating the efficiency curve of Fig. 6 for even higher swings (assuming not to break the transistors) it may seem that more than 100% η_P could be reached. In reality at some point a decrease of η_I would nullify the slight increase of η_V , making η_P to saturate to a value close but still below 100%.

We compare ENF from the model (assuming a $\Gamma_{T,rms}^2 = 1/2$, $\Gamma_{M,rms}^2 = 1/2$, and $\gamma_{MOS} = 1$) and from simulations as a function of the output voltage swing. As shown in Fig. 6 simulations confirm the model within an error of 0.8 dB over a large range of swings. This error is due to excess transistors noise and is probably explained by an increase in γ_{MOS} for high swing.

A practical limit of the class-B oscillator with tail filter is the large voltage that the active device must endure. For a 1.5 V supply simulation shows that the maximum V_{GS} is close to 4 V. The problem is greatly reduced using the p-n topology shown in Fig. 5(b). In this case, 100% η_P is reached with half the voltage swing of the n-only topology, i.e., $\pi/4 V_{DD}$ peak. Simulation for the same operating condition as above (using a fully-differential tank capacitance) shows that the best ENF is close to that of the n-only case with a maximum V_{GS} of 1.9 V, i.e., compatible with thick oxide device almost always available in any deep scaled CMOS technology.

C. Class-C Oscillators

Another way to improve ENF is by improving η_I . This leads to the class-C oscillator whose schematic is the same as the AC coupled class B (Fig. 4) with the addition of a large capacitance in parallel to the current source. Despite their apparent similarity, the two topologies behave very differently. First, since the DC drop on the coupling capacitors is much larger for the former, the switching transistors are off when balanced. Second, the large capacitor shunting the current source allows to deliver sharp current spikes at the peak of the voltage swing. Combining these two effects drastically reduces the conduction angle for the tank current, as shown in Fig. 7. In the limit the tank current becomes a series of pulses giving an η_I of $1/\sqrt{2}$ and an η_P of $(V_{sw}/V_{DD})(1 - V_B/V_{DD})$, where V_{sw} is the peak voltage swing. For the same bias current this could give 3.9 dB increase in the ENF compared with a class-B oscillator (1.95 dB due to better η_I , 1.95 dB due to better η_V), as indicated in the literature [12]. However, to get such an improvement the class-B oscillator should have been operated at small oscillation amplitudes, very far from the optimum ENF (i.e., in current limited mode). For the same oscillation amplitude only η_I increases, giving a 1.95 dB ENF improvement. If the noise of the current source is negligible, the ENF of a class-C oscillator is given by $10 \log(V_{DD}/V_{sw})(1 + \gamma_{MOS})$ where V_{sw} is the peak swing. This shows that also a class-C oscillator has an ENF uniquely defined by its voltage swing and, for the same V_{DD} , it has the same ENF of a class-B with a voltage swing $2/\pi$ times smaller. Ideally, with $V_B = 0$, 100% η_P can be reached with a differential voltage swing of $2V_{DD}$ peak (compared with πV_{DD} in the class-B oscillator with tail filter). The large shunt capacitance of the class-C oscillator filters out the noise of the bias allowing a smaller V_B further improving η_P .

The class-C oscillator has a drawback that severely limits its phase noise at large oscillation amplitudes efficiency. Due to the shunt capacitor, when the switching transistors are in the triode region they load the tank, increasing noise. The maximum swing that ensures saturation is $V_{DD} - V_B$ (assuming that the switching transistors are biased just one threshold above ground). In this condition, even assuming $V_B = 0$, η_P is 50% with a loss of 3 dB in the ENF. In practice the optimum FoM

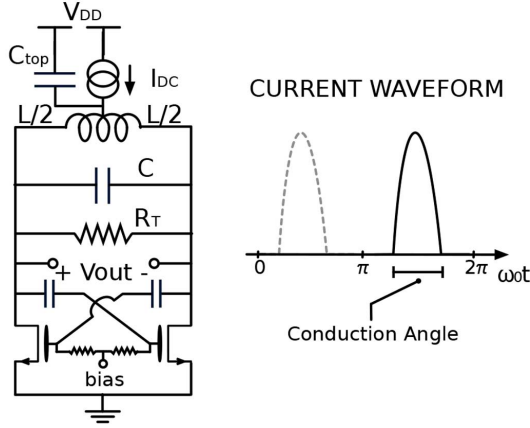


Fig. 7. Class-C oscillator (NMOS only).

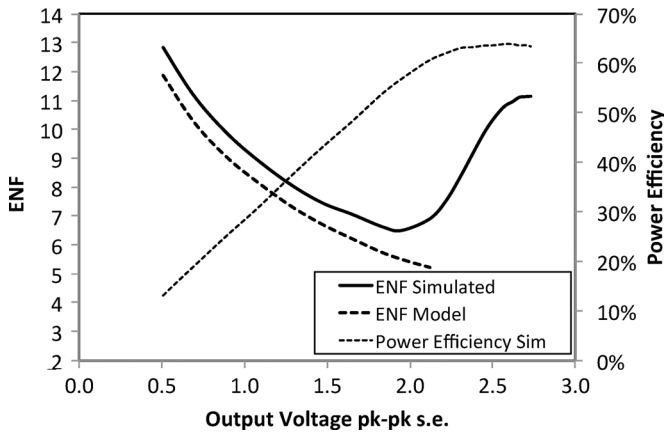


Fig. 8. Class-C oscillator: calculated and simulated ENF and simulated power efficiency.

is achieved when the device just enters the triode region at the oscillation peak with a slightly higher noise but a sufficiently higher η_P to give a better ENF [12].

We compare ENF from the model (assuming a $\Gamma_{T,rms}^2 = 1/2$, $\Gamma_{M,rms}^2 = 1/2$ and $\gamma_{MOS} = 1$) and from simulations as a function of the output voltage swing in the same operating conditions as above. Such a comparison is shown in Fig. 8, which also plots η_P . As expected, initially η_P increases and ENF decreases almost linearly with the swing. In this region the model error stays below 1 dB and is caused by the transistors noise (γ_{MOS} is larger than 1).

At large voltage swings, where the switching transistors enter into the linear region, the model cannot be used since the circuit loads the tank. The difference between model and simulation increases due to two effects. First, noise from the tank, switching pair, and current source increases. Second, η_I decreases, cancelling the corresponding increase in η_V as shown in the η_P plot. Simulation predicts a minimum of the ENF of 6.5 dB for a differential peak swing of 1.3 V_{dd} , which is close to the ENF of the model at the edge of its range of validity.

D. Class-F Oscillator

Another way to improve efficiency in a PA is by acting on the resonator. The goal is to create an output waveform with

sharper transitions (ideally a square wave) so that the active devices dissipate power for a smaller percentage of time. The same concept should give a better FoM since efficiency and FoM are directly related. In addition the new resonator has a different ISF, with potentially an even larger effect on the ENF. A possible class-F oscillator (shown in Fig. 9(a)) uses two series-connected LC tanks, resonating respectively at the fundamental frequency (ω_0) and at the third harmonic. Assuming a square wave current and sufficiently high Q, the voltage across the first tank is a sinusoid at ω_0 and the voltage across the second tank a sinusoid at $3\omega_0$, with opposite phase. If the tank impedances at $3\omega_0$ and at ω_0 are comparable the voltage resembles the one of Fig. 9(b). At the switching instants the waveform has a higher slope than a sinusoid with the same peak amplitude, potentially improving phase noise. This oscillator is analyzed using the ISF approach in Appendix A. The phase noise can be expressed as:

$$L(\Delta\omega) = 10 \log \left\{ f_{RES} (1 + \gamma_{MOS}) \frac{kT}{2P_{RF}} \left(\frac{\omega_0}{Q_{\omega_0} \Delta\omega} \right)^2 \right\} \quad (14)$$

where P_{RF} is the signal power, Q_{ω_0} is the Q of the tank at ω_0 , and f_{RES} is the *resonator noise factor*, given in (A13), which is a function of the ratio between the resonator impedances and the quality factors of the two resonators. Assuming transistor current noise is γ_{MOS} times the derivative of the drain current with respect to the gate voltage, the transistors phase noise is γ_{MOS} times the tank phase noise, i.e., the result derived in [9], [12] for harmonic oscillators is true also for class-F. To minimize ENF we need to minimize f_{RES} and to maximize efficiency. Appendix A shows that f_{RES} decreases as $Q_3\omega_0$ is increased. Moreover, if $Q_3\omega_0$ is greater than $5/3 Q_{\omega_0}$, f_{RES} is smaller than 1 and is proportional to C_3 . The minimum C_3 is when the impedances at $3\omega_0$ and at ω_0 are equal (to prevent oscillation at $3\omega_0$). If $Q_3\omega_0$ is too small f_{RES} becomes larger than 1. To verify the analysis, two class-F and a class-B oscillators have been simulated for the same operating conditions. In one class-F $Q_3\omega_0$ is equal to Q_{ω_0} , while in the other $Q_3\omega_0$ is equal to $3Q_{\omega_0}$. In both cases the resonator impedance at ω_0 and at $3\omega_0$ is nearly equal. Fig. 10 reports the simulated and calculated phase noise as a function of the DC power dissipation. As expected, increasing $Q_3\omega_0$ gives a better phase noise. When Q_{ω_0} and $Q_3\omega_0$ are equal, class-F and the class-B oscillators show the same phase noise since conversion efficiency and resonator noise compensate each other.

E. Transformer-Coupled Oscillators

Transformer-based oscillators are often used to improve tuning range [32], [37]–[40] thanks to different resonant modes at different frequencies. In fact, as analyzed in [37], high order LC tanks have potential advantages in wideband or multiband applications. However, with the increase of resonator order, frequency stability becomes an issue and more design parameters have to be optimized simultaneously (including inductance ratio, capacitance ratio, and coupling factor). As an example Goel *et al.* [40] obtained a good peak FoM of 192 dBc/Hz, however, since the impedance and quality factor can change significantly from mode to mode, the FoM varies more than 5 dB over the tuning range [37]–[40].

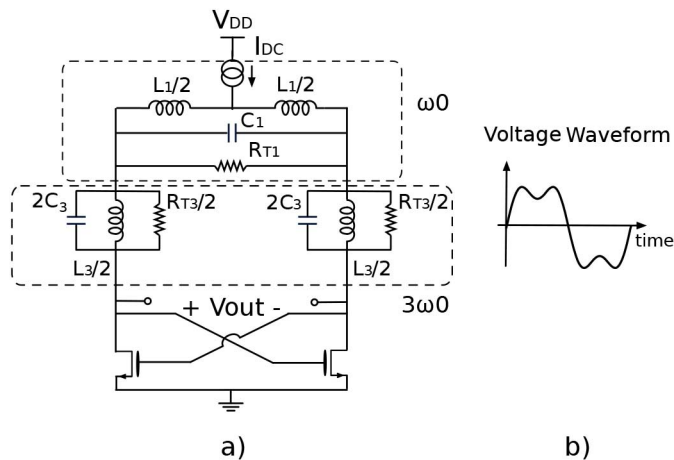


Fig. 9. Class-F oscillator: (a) circuit schematic and (b) typical voltage waveform.

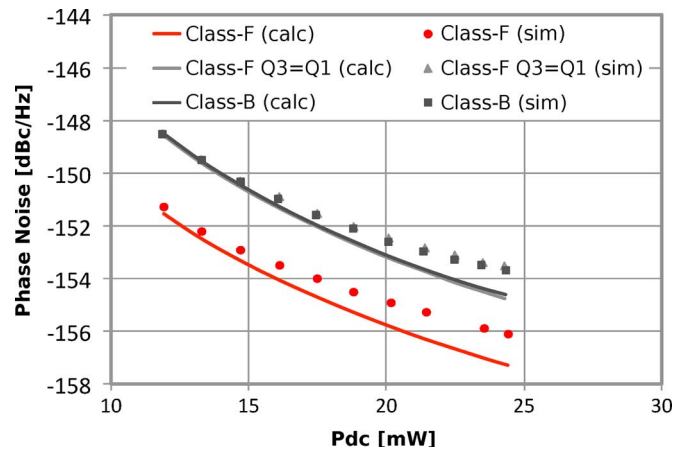


Fig. 10. Comparison between Class-F and Class-B oscillators phase noise. Dots represent simulated data, lines are calculated based on (11)–(14).

On the other hand, the transformer-coupled technique can be used also to reduce the noise of the active devices, i.e., to improve ENF. In fact, introducing a gain between the tank and the active devices, reduces α in (7). This was done via a step-up transformer by Mazzanti and Andreani [12] for a class-C oscillator, which obtained one of the highest FoM published. Experimental verification, however, shows nearly the same ENF as with direct coupling. This is because in a transformer coupled oscillator the active devices contribute less noise but enter earlier in the linear region due the larger swing. Since for class-C the optimum FoM is achieved with the active devices just reaching the edge of the linear region at maximum swing, transformer coupling reduces both noise and efficiency. Transformer coupling can be used in class B with LC tail filter topology with potential benefits since the active devices can enter the linear region without loading the tank. Even if simulation and theory indeed show a potential transistor noise reduction, the step-up transformer-coupled [12] oscillator suffers from several drawbacks. The quality factor of the secondary is usually less than the primary, which means its noise is no more negligible. Second, the absolute quality factor obtainable is less than the one of a single inductor. Finally,

a step-up transformer generally occupies more area than its equivalent inductor. Another key problem is device reliability due to high swing at the gate. A way to mitigate the latter problem is to use p-n topology and/or to reduce the voltage supply. The need of a very low voltage supply, which may help from a reliability point of view, poses a challenge in the design of the voltage regulator, always needed in industrial applications.

F. Comparison Between Topologies

Table I summarizes the maximum power efficiency and the minimum ENF for the oscillators considered. The most promising topologies are the class-B with tail filter and the class-C. Notice that further benefits could potentially be achieved using transformer coupling, but we have not inserted this possibility in the table due to its many practical limitations. Table I looks only at fundamental noise limits and does not reflect other important design considerations and practical aspects, such as tuning range, start-up issues, and area occupation.

From an industrial point of view, class-B with tail filter and class-C are the most feasible structures. Therefore, these are the two topologies we have chosen for the prototype circuit implementation. Class-B with tail filter is one of the most interesting architectures thanks its advantages, obtained with a relatively simple design and a small additional area. On the other hand, class-C oscillators suffer from a trade-off between oscillation amplitude and start-up conditions that could reduce its advantages with respect to a class-B. To improve efficiency, the gate bias voltage should be as low as possible, while meeting the Barkhausen criteria in a reliable way. To overcome this limitation, in recent years solutions like dynamic bias [13] and hybrid class C/B [35] were presented. As a consequence, we have decided to implement the hybrid class C/B oscillator for its greater robustness even if it has a higher ENF compared with a simple class-C.

IV. EXPERIMENTAL VERIFICATION

A key challenge to compare different oscillators is the strong noise sensitivity to tank Q. It is necessary to know Q with a few per cent accuracy to ascertained improvements of the order of 1 dB. This difficulty has resulted in reported numbers inconsistent or even unfeasible. To verify our model a test chip was implemented in TSMC 55 nm CMOS (shown in Fig. 11) that includes a class-B oscillator with tail filter, and an hybrid class-C/class-B oscillator (shown in Fig. 12) oscillating around 7.5 GHz two dividers by 2 and two peak detectors to sense the oscillation amplitude. In both cases, n-type transistors implement the negative resistance and a p-type transistor provide the bias current. The gate voltage bias for the core transistors in the hybrid oscillator is provided by an external voltage generator through a passive on-board low-pass RC filter with very low cut-off frequency. Great care was taken to eliminate spurious effects. First of all, the same tank (including tuning) was used for both topologies. To see the effect of the divider, the class-B oscillator was stepped twice followed by two different dividers. Almost identical phase noise is obtained after division up to about 20 MHz

TABLE I
EFFICIENCY COMPARISON OF NMOS VCOS

OSC. TYPE	$\eta_{I, \max}$	$\eta_{V, \max}$	$\eta_{P, \max}$	ENF _{min} ($\gamma_{\text{MOS}}=1$) Simulated
CLASS-B	$\sqrt{2}/\pi$	$\sqrt{2} \left(1 - \frac{V_B}{V_{DD}}\right)$	$\frac{2}{\pi} \left(1 - \frac{V_B}{V_{DD}}\right)$	~10dB
CLASS-B AC-BIAS	$\sqrt{2}/\pi$	$\sqrt{2} \left(1 - \frac{V_B}{V_{DD}}\right)$	$\frac{2}{\pi} \left(1 - \frac{V_B}{V_{DD}}\right)$	~8.5dB
CLASS-B AC-BIAS LC-FILTER	$\sqrt{2}/\pi$	$\frac{\pi}{\sqrt{2}} \left(1 - \frac{V_B}{V_{DD}}\right)$	$1 - \frac{V_B}{V_{DD}}$	~4.5dB
CLASS-C	$1/\sqrt{2}$	$1/\sqrt{2}$	$1/2$	~6dB
CLASS-F	$\sqrt{2}/\pi$	$\frac{4\sqrt{2}}{\pi} \left(1 - \frac{V_B}{V_{DD}}\right)$	$\frac{8}{\pi^2} \left(1 - \frac{V_B}{V_{DD}}\right)$	~8.5dB

offset demonstrating that the phase noise of the dividers is negligible in the frequency of interest. Both VCOS are tunable from about 6.1 GHz to 8.7 GHz through two MOM capacitor banks (a 7-bit coarse and a 4-bit fine) and a continuous tuning varactor. For the class B oscillator, a small tail inductor resonates the tail capacitance at $2\omega_0$. Due to its low Q (about 3) it is not tuned as ω_0 varies. Fig. 13 shows the simulated and measured phase noise for both oscillators with a 1.5 V supply. The bias currents at maximum FoM are 12.5 mA for the hybrid and 21.6 mA for class-B. Both oscillators exceed the GSM requirement of -150 dBc/Hz at 20 MHz offset with 3.6 GHz carrier over the entire tuning range. The hybrid oscillator shows an extra noise term below 10 MHz offset associated with the resistors at the gate of the switching transistors in the class-C portion which are relatively small. Fig. 14 shows oscillation amplitude vs. bias current for the two cases, the two different slopes show an η_I about 25% better for the hybrid. This is significantly less than what is expected for ideal class-B vs. class-C. Simulations partially explain the lower efficiency of the hybrid class-C/class-B structure [35]. The peak detector maximum voltage range limits the validity of the data at high swing. From the measured oscillation amplitude vs. bias current and simulated η_I a tank Q about 9.7 at 7.6 GHz is obtained. This relatively low value is due to the large tuning range and very low target phase noise that increases sensitivity to non idealities [32]. Peak FoM is 187.1 and 187.9 dB with an η_P of 36% and 42% for the hybrid and class-B, respectively (Fig. 15). These results agree well with simulations and are consistent with the model prediction that at the peak FoM should depend only on efficiency. Measured and simulated FoM and ENF versus output voltage for both topologies are plotted in Figs. 15 and 16, respectively. At low bias, the superior η_I of the hybrid gives better η_P (see Fig. 15), leading to a better FoM. For the hybrid, however, as the amplitude increases and the transistors enter triode region, ISF increases and the FoM reaches a peak around 1.4 V p-t-p swing. On the other hand, for the class-B the tail filter avoids loading the tank even if the tran-

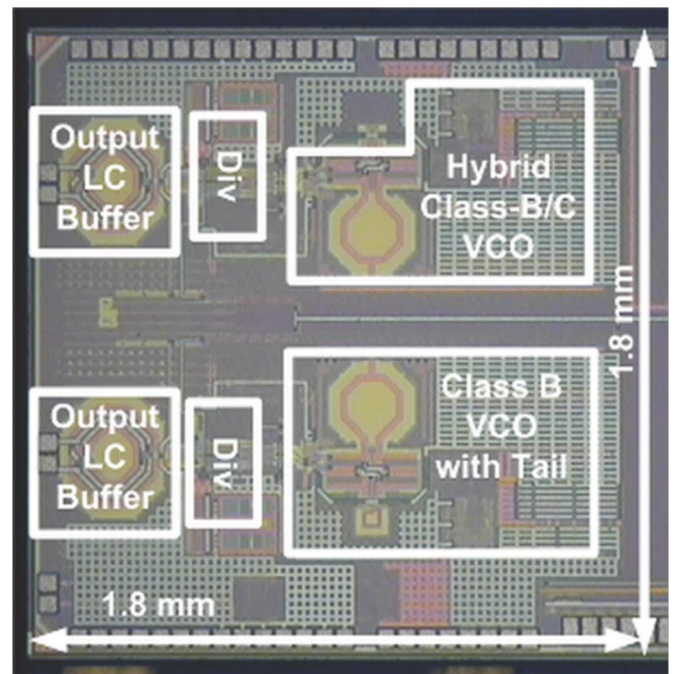


Fig. 11. Chip photo and block diagram of the prototype.

sistors enter the triode region. As a result, transistor ISF change only slightly up to 2.1 V p-t-p giving a higher peak FoM. Notice that the class-B oscillator could achieve an even higher FoM if pushed to higher oscillation amplitudes (ideally 4.7 V p-t-p gives 100% η_P). The oscillation amplitude was limited to 2.1 V p-t-p for reliability reason.

V. CONCLUSION

An intuitive model for the phase noise of oscillators whose load is driven from a current source is derived including an ENF that normalizes the FoM to the fundamental limit. It is found that class-B with tail tank and class-C oscillators more closely

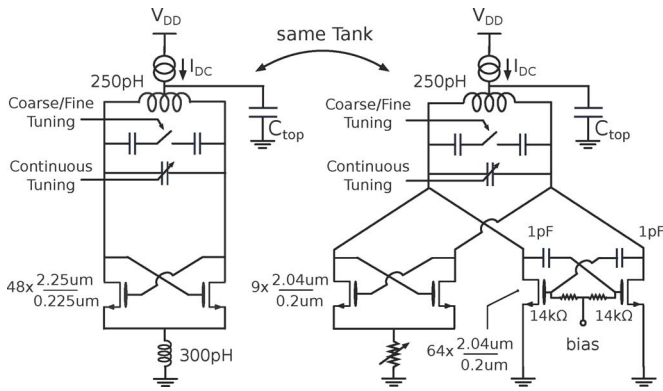


Fig. 12. Schematic of the class-B and Hybrid class-C/B oscillators.

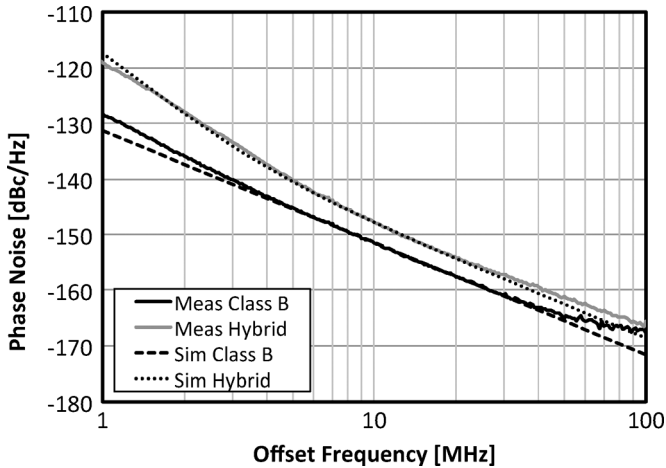


Fig. 13. Measured phase noise after frequency division by 2 of class-C and class-B oscillators at their respective maximum FoM bias point (12.5 mA for Hybrid class-C/B and 21.6 mA for class-B) when tuned at 7.6 GHz. For comparison the simulated phase noise is also reported.

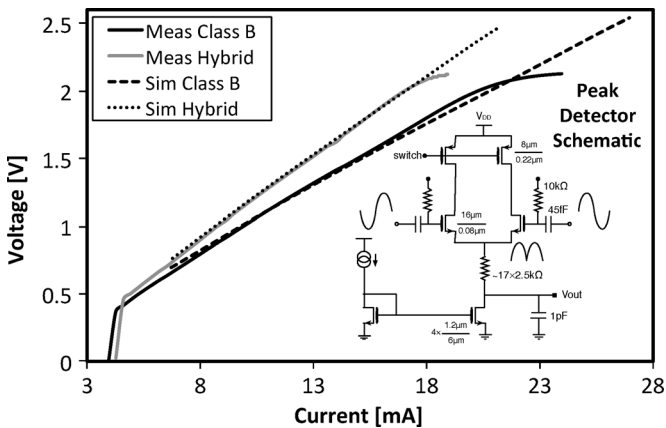


Fig. 14. Oscillation amplitude vs bias current: measurements and simulations. The schematic of the peak detector is also reported.

approach the limit while class-F become competitive when the $3\omega_0$ tank has a Q higher than the ω_0 one. These conclusions are consistent with experimental data although uncertainty in the Q gives a wide spread between the FoM of different implementation of the same topology. To verify the analysis a test chip was fabricated where Q uncertainty and other effects can only affect the absolute value of the measured data but not the relative one. Class-B with tail filter and class-C where compared,

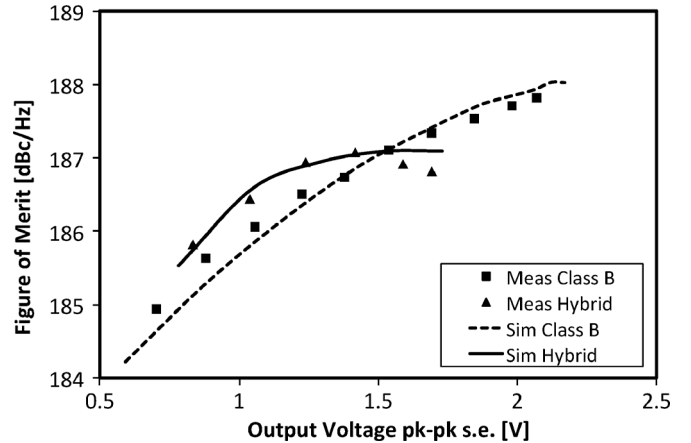


Fig. 15. FoM vs output voltage for the class-B and Hybrid class-C/B oscillators: Measurements and simulations.

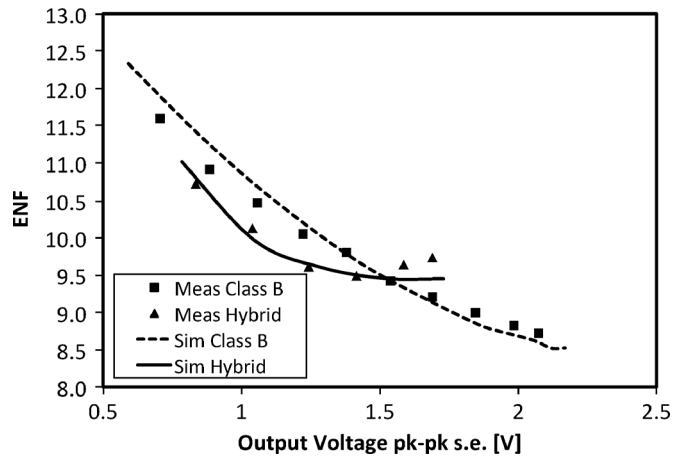


Fig. 16. ENF vs output voltage for the class-B and Hybrid class-C/B oscillators: Measurements and simulations.

giving results consistent with expectations. The possibility of using step-up transformer coupling between the tank and the MOS gates to potentially reduce transistor phase noise has been indicated as a potential way to further improve the ENF.

APPENDIX A

For the class-F oscillator of Fig. 9, the load is a fourth-order system made of two LC tanks, resonating at ω_0 and $3\omega_0$. The ISF for each noise source is calculated starting from the state vector X [2], [3], [36] defined as:

$$\vec{X} = \left[V_{C1} \sqrt{\frac{L_1}{C_1}} I_{L1} \sqrt{\frac{C_3}{C_1}} V_{C3} \sqrt{\frac{L_3}{C_1}} I_{L3} \right]. \quad (A1)$$

The four state variables are the voltage on the capacitors and the current in the inductors. The steady-state oscillation is approximated by a sinusoid at ω_0 across the main tank and a sinusoid at $3\omega_0$ across the second tank (opposite in phase). The steady-state vector is:

$$\vec{X}_0 = \left[A_1 \cos \omega_0 t \quad A_1 \sin \omega_0 t \quad -\sqrt{\frac{C_3}{C_1}} A_3 \cos 3\omega_0 t \quad -\sqrt{\frac{C_3}{C_1}} A_3 \sin 3\omega_0 t \right] \quad (A2)$$

The system can be represented as the steady-state vector X_0 , plus a random perturbation vector ΔX . Neglecting the component of ΔX orthogonal to the trajectory, the phase perturbation $\Delta\phi$ can be derived from the state variables derivatives \dot{X} [3], [36]. The ISF in terms of state-space vectors is:

$$\Gamma_i = \omega_0 \frac{q_{\text{MAX}}}{\Delta q} \frac{\Delta \vec{X}_i \cdot \dot{\vec{X}}}{|\dot{\vec{X}}|^2}. \quad (\text{A3})$$

The main noise sources are the tank losses and the transistors noise. ISFs of the two tanks are:

$$\Gamma_1 = \frac{q_{\text{MAX}}}{A_1 C_1} \frac{-\sin(\omega_0 t)}{\left(1 + \frac{9A_3^2 C_3}{A_1^2 C_1}\right)}, \quad (\text{A4})$$

$$\Gamma_3 = \frac{q_{\text{MAX}}}{A_1 C_1} \frac{3A_3}{A_1} \frac{\sin(3\omega_0 t)}{\left(1 + \frac{9A_3^2 C_3}{A_1^2 C_1}\right)}. \quad (\text{A5})$$

From the noise density in the two tanks, given by $I_{n,1}^2/\Delta f = 4kT\omega_0 C_1/Q\omega_0$ and $I_{n,3}^2/\Delta f = 4kT3\omega_0 C_3/Q_3\omega_0$ respectively, and (A4) and (A5) the phase noise can be computed adding up the two contributions [3] as:

$$L_{\text{RES}}(\Delta\omega) = 10 \log \left\{ f_{\text{RES}} \frac{kT}{2P_{\text{RF}}} \left(\frac{\omega_0}{Q\omega_0 \Delta\omega} \right)^2 \right\} \quad (\text{A6})$$

where P_{RF} is the power dissipated by the resonator and the *tank noise factor* f_{RES} is:

$$f_{\text{RES}} = \frac{\left(1 + \frac{3Q\omega_0 C_3}{Q_3\omega_0} \frac{9A_3^2}{A_1^2}\right) \left(1 + \frac{3Q\omega_0}{Q_3\omega_0} \frac{A_3^2 C_3}{A_1^2 C_1}\right)}{\left(1 + \frac{9A_3^2 C_3}{A_1^2 C_1}\right)}. \quad (\text{A7})$$

When f_{RES} is equal to 1 the resonator phase noise in a class-F oscillator is the same as that of tank1 in a class-B oscillator. To derive useful design insights (A7) is simplified as follows. The ratio between the amplitude at the third harmonic (A_3) and at the fundamental (A_1) can be expressed in terms of the ratio between the impedance at the two resonance frequencies (z_3) as $A_3/A_1 \sim \beta z_3/3$, where β depends on the current waveforms and is equal to 1 for a square-wave. Using this approximation in (A7) f_{RES} becomes:

$$f_{\text{RES}} \cong \frac{(1 + \beta^2 z_3) \left(1 + \frac{\beta^2}{9} z_3\right)}{\left(1 + \beta^2 z_3 \frac{Q_3\omega_0}{3Q\omega_0}\right)^2}. \quad (\text{A8})$$

To optimize phase noise f_{RES} must be minimized. When z_3 is increased the amplitude of the third harmonic increases and a waveform with a steeper slope is obtained but the noise added by the third harmonic tank increases. For $Q_3\omega_0$ larger than $5/3$, $Q\omega_0 f_{\text{RES}}$ is smaller than 1 and decreases as z_3 is increased. For $Q_3\omega_0$ lower than $5/3$, $Q\omega_0 f_{\text{RES}}$ increases with z_3 . The oscillator in Fig. 9 has been simulated under the same operating conditions used for the class-B oscillators and the results are reported in Fig. 17. The simulated phase noise of the tank as well as the percentage due to the third harmonic tank match well with calculations. As predicted by (A8), for C_3 and C_1 such that the impedance at the two resonance frequencies is the same, the percentage of noise of the third harmonic tank is nearly con-

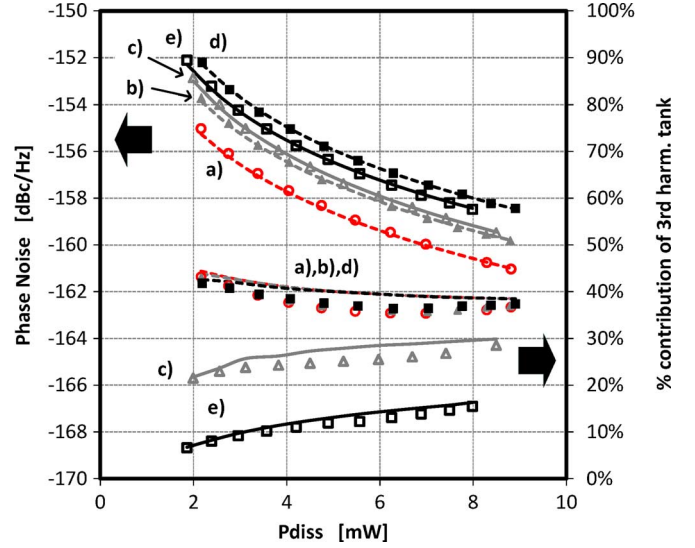


Fig. 17. Class-F oscillators total phase noise of the resonator (left scale) and percentage of the third harmonic tank (right scale). Dots are simulations, lines are calculations: (a) $Q_3 = 3Q_1$, $C_3 = C_1$; (b) $Q_3 = 2Q_1$, $C_3 = 2/3C_1$; (c) $Q_3 = 2Q_1$, $C_3 = C_1$; (d) $Q_3 = Q_1$, $C_3 = 1/3C_1$; (e) $Q_3 = Q_1$, $C_3 = C_1$.

stant, independent Q. When $Q_3\omega_0$ is equal to $2Q\omega_0$ increasing z_3 improves the phase noise, while when $Q_3\omega_0$ is equal to $Q\omega_0$ phase noise degrades for higher z_3 . The ISF of the active devices (Γ_{TR}) is calculated using (A3) but with a charge pulse applied across the whole tank. Γ_{TR} is equal to $\Gamma_1 + \Gamma_3$. The thermal noise of the transistors is a time-varying function equal to $4kt \gamma_{\text{MOS}} g_m(t)$. The transconductance can be approximated as:

$$g_m = \frac{\partial i}{\partial V} = \frac{\partial i}{\partial t} \frac{1}{\partial V / \partial t} = \frac{\sum_{k=0}^{\infty} k I_k \sin(k\omega_0 t + \phi_k)}{A_1 \sin(\omega_0 t) - 3A_3 \sin(3\omega_0 t)} \quad (\text{A9})$$

where I_k are the Fourier coefficients of the current waveform. Using (A9), (A4), and (A5) (to compute Γ_{TR}) yields the transistor phase noise:

$$L_{\text{TR}}(\Delta\omega) = 10 \log \left\{ f_{\text{RES}} \frac{\gamma_{\text{MOS}} kT}{2P_{\text{RF}}} \left(\frac{\omega_0}{Q\omega_0 \Delta\omega} \right)^2 \right\} \quad (\text{A10})$$

where f_{RES} is given by (A7) or (A8). This result is similar to the general result derived by Bank for sinusoidal oscillators i.e., the noise of the transistors is γ_{MOS} times the noise of the tank, irrespective of the device details. However, in a class-F oscillator, the device size and bias influence the amplitude ratio between the third and the fundamental harmonic through the coefficient β in (A8). Based on (A6) and (A10), the phase noise expression of the class-F oscillator is found, as reported in (14).

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REFERENCES

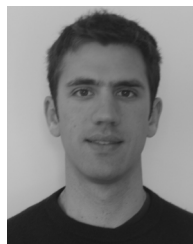
- [1] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proc. IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.

- [2] F. X. Kaertner, "Determination of the correlation spectrum of oscillators with low noise," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 1, pp. 90–101, Jan. 1989.
- [3] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.
- [4] A. Demir, A. Mehrotra, and J. Roychowdhury, "Phase noise in oscillators: A unifying theory and numerical methods for characterization," *IEEE Trans. Circuits Syst. I*, vol. 47, no. 5, pp. 655–674, May 2000.
- [5] J. J. Rael and A. A. Abidi, "Physical processes of phase noise in differential LC oscillators," in *Proc. 2000 IEEE Custom Integrated Circuits Conf. (CICC)*, May 2000, pp. 569–572.
- [6] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in Colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.
- [7] D. Murphy, J. J. Rael, and A. A. Abidi, "Phase noise in LC oscillators: A phasor-based analysis of a general result and of loaded Q," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 6, pp. 1187–1203, Jun. 2010.
- [8] P. Kinget, "Integrated GHz voltage controlled oscillators," in *Analog Circuit Design*. Boston, MA, USA: Kluwer Academic, 1999, pp. 353–381.
- [9] J. Bank, "A harmonic-oscillator design methodology based on describing functions," Ph.D. dissertation, Dept. Signals Syst., Sch. Elect. Eng., Chalmers Univ. Techn., Chalmers, Sweden, 2006.
- [10] J. van der Tang and D. Kasperkovitz, "Oscillator design efficiency: A new figure of merit for oscillator benchmarking," in *Proc. IEEE ISCAS*, 2000, vol. II, pp. 533–536.
- [11] A. Zanchi, A. Bonfanti, S. Levantino, C. Samori, and A. L. Lacaita, "Automatic amplitude control loop for a 2-V, 2.5-GHz LC-tank VCO," in *Proc. 2001 IEEE Custom Integrated Circuits Conf.*, May 9–9, 2001, pp. 209–212.
- [12] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.
- [13] L. Fanori and P. Andreani, "Highly efficient class-C CMOS VCOs, including a comparison with class-B VCOs," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, pp. 1730–1740, Jul. 2013.
- [14] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, MA, USA: Cambridge Univ. Press, 1998.
- [15] A. Visweswaran, R. Staszewski, and J. Long, "A clip-and-restore technique for phase desensitization in a 1.2 V 65 nm CMOS oscillator for cellular mobile and base stations," in *2012 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 350–352.
- [16] L. Fanori and P. Andreani, "A 2.5–3.3 GHz CMOS class-D VCO," in *2013 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2013, pp. 346–347.
- [17] H. Wang, "A 9.8 GHz back-gate tuned VCO in 0.35 μm CMOS," in *2013 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 1999, pp. 406–407.
- [18] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE J. Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.
- [19] B. De Muer, M. Borremans, M. Steyaert, and G. Li Puma, "A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise up-conversion minimization," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 1034–1038, Jul. 2000.
- [20] C. Samori, A. L. Lacaita, A. Zanchi, S. Levantino, and G. Cali, "Phase noise degradation at high oscillation amplitudes in LC-tuned VCO's," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 96–99, Jan. 2000.
- [21] F. Svelto, S. Deantoni, and R. Castello, "A 1 mA, -120.5 dBc/Hz at 600 kHz from 1.9 GHz fully tunable LC CMOS VCO," in *Proc. 2000 IEEE Custom Integrated Circuits Conf. (CICC)*, May 2000, pp. 577–580.
- [22] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, Jun. 2001.
- [23] P. Andreani and H. Sjolund, "Tail current noise suppression in RF CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 37, no. 3, pp. 342–348, Mar. 2002.
- [24] N. H. W. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. F. Wagner, C. Plett, and N. G. Tarr, "Design of wide-band CMOS VCO for multiband wireless LAN applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 8, pp. 1333–1342, Aug. 2003.
- [25] G. De Astis, D. Cordeau, J.-M. Paillot, and L. Dascalescu, "A 5 GHz fully integrated full PMOS low phase noise LC VCO," *IEEE J. Solid-State Circuits*, vol. 40, no. 10, pp. 2087–2091, Oct. 2005.
- [26] H. Kim, S. Ryu, Y. Chung, J. Choi, and B. Kim, "A low phase-noise CMOS VCO with harmonic tuned LC tank," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 7, pp. 2917–2924, Jul. 2006.
- [27] H.-H. Hsieh and L.-H. Lu, "A high-performance CMOS voltage-controlled oscillator for ultra-low-voltage operations," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 3, pp. 467–473, Mar. 2007.
- [28] S. Dal Toso, A. Bevilacqua, M. Tiebout, N. Da Dalt, A. Gerosa, and A. Neviani, "A 0.06 mm² 11 mW Local oscillator for the GSM standard in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 7, pp. 1295–1304, Jul. 2010.
- [29] P. Andreani, K. Kozmin, P. Sandrup, M. Nilsson, and T. Mattison, "A TX VCO for WCDMA/EDGE in 90 nm RF CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1618–1626, Jul. 2011.
- [30] T. W. Brown, F. Farhabakhshian, A. Guha Roy, T. S. Fiez, and K. Mayaram, "A 475 mV, 4.9 GHz enhanced swing differential colpitts VCO with phase noise of -136 dBc/Hz at a 3 MHz offset frequency," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1782–1795, Aug. 2011.
- [31] A. Liscidini, L. Fanori, P. Andreani, and R. Castello, "A 36 mW/9 mW power-scalable DCO in 55 nm CMOS for GSM/WCDMA frequency synthesizers," in *2012 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, 2012, pp. 348–350.
- [32] G. Li, L. Liu, Y. Tang, and E. Afshari, "A low-phase-noise wide-tuning-range oscillator based on resonant mode switching," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1295–1308, Jun. 2012.
- [33] P. Andreani and A. Fard, "More on the phase noise performance of CMOS differential-pair LC-tank oscillators," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2703–2712, Dec. 2006.
- [34] E. Hegazi, H. Sjolund, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.
- [35] L. Fanori, A. Liscidini, and P. Andreani, "A 6.7-to-9.2 GHz 55 nm CMOS hybrid class-B/class-C cellular TX VCO," in *2012 IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 19–23, 2012, pp. 354–356.
- [36] P. Andreani and X. Wang, "On the phase-noise and phase-error performances of multiphase LC CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1883–1893, Nov. 2004.
- [37] S. Rong and H. C. Luong, "Analysis and design of transformer-based dual-band VCO for software-defined radios," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 59, no. 3, pp. 449–462, Mar. 2012.
- [38] A. Bevilacqua, F. P. Pavan, C. Sandner, A. Gerosa, and A. Neviani, "A 3.4–7 GHz transformer-based dual-mode wideband VCO," in *Proc. 32nd European Solid-State Circuits Conf., ESSCIRC*, 2006, pp. 440–443.
- [39] J. Borremans, A. Bevilacqua, S. Bronckers, M. Dehan, M. Kuijk, P. Wambacq, and J. Craninckx, "A compact wideband front-end using a single-inductor dual-band VCO in 90 nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2693–2705, Dec. 2008.
- [40] A. Goel and H. Hashemi, "Frequency switching in dual-resonance oscillators," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 571–582, Mar. 2007.



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Prof. Castello has been a member of the TPC of the European Solid-State Circuits Conference (ESSCIRC) since 1987 and of the IEEE International Solid-State Circuits Conference (ISSCC) from 1992 to 2004. He was Technical Chairman of ESSCIRC 1991 and General Chairman of ESSCIRC 2002, Associate Editor for Europe of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1994 to 1996 and Guest Editor of the July 1992 special issue. From 2000 to 2007, he was a Distinguished Lecturer of the IEEE Solid-State Circuits Society. Prof. Castello was named one of the outstanding contributors for the first 50 and 60 years of ISSCC and a co-recipient of the Best Student Paper Award at the 2005 Symposium on VLSI of the Best Invited Paper Award at the 2011 CICC and of the Best Evening Panel Award at ISSCC 2012. He was one of the two European representatives at the Plenary Distinguished Panel of ISSCC 2013.