A Power-Scalable DCO for Multi-Standard GSM/WCDMA Frequency Synthesizers

Antonio Liscidini, *Senior Member, IEEE*, Luca Fanori, *Member, IEEE*, Pietro Andreani, *Senior Member, IEEE*, and Rinaldo Castello, *Fellow, IEEE*

***Abstract*—A Digitally Controlled Oscillator (DCO) whose power consumption can be reconfigured while maintaining an almost constant phase-noise figure-of-merit (FoM). This is achieved by using either a single-switch-pair or a complementary (i.e., double-switch-pair) oscillator topology, without disturbing the optimized LC tank of the DCO. The optimal power consumption in the complementary (P-N) configuration is reduced by 75% compared to the single-switch-pair (N-only) configuration, while the FoM is kept constant. Measurements on a 55 nm CMOS 4 GHz DCO prototype show a minimum phase noise of −129.3 dBc/Hz at 2 MHz offset from the carrier in the P-N configuration, and of −134.7 dBc/Hz in the N-only configuration, with a phase noise difference very close to the 6 dB expected from theory. The current consumption is 6 mA and 24 mA, respectively, resulting in approximately the same FoM of −185 dBc/Hz.**

***Index Terms*—DCO, GSM, oscillator, phase noise, power scalable, reconfigurable oscillator, reconfigurability, WCDMA.**

I. Introduction

THE compatibility with several standards sets major constraints in the design of voltage-controlled oscillators (VCOs) for cellular applications. In particular, beside a large tuning range (typically larger than 33%, and in some cases approaching 50%), a cellular transmitter (TX) VCO must provide an exacting phase noise performance, especially if SAW-less operation is demanded [1].

If the TX frequency synthesizer must be compliant with a multi-standard transceiver, an efficient power scalability of the VCO is crucial to save power in those cases where the phase noise requirements are relaxed, while still providing the lowest possible phase noise where needed. Nowadays, most multi-standard transceivers adopt different VCOs (up to 6 or even more if carrier aggregation is supported) to cover the different standards with good phase noise as well as good power efficiency, even if the available tuning range would suffice to cover all frequency bands with a smaller number of VCOs. The reason for this choice is that customizing the VCO to the specific requirements of a given standard is generally more efficient in terms of power consumption, especially when phase noise requirements vary significantly from case to case (e.g., between GSM and WCDMA) [2].

A very straightforward way of obtaining power scalability is by tuning the VCO bias current while keeping the same LC tank in all configurations, as in the wide-band multi-standard single-oscillator TX synthesizer described in [3]. Although this approach is simple and saves the area of an extra VCO, current tuning is relatively power inefficient and has a limited power-scalability range. This is primarily due to the fact that, for low current levels, it is difficult to sustain an oscillation having adequate amplitude to drive the buffers following the VCO, even though the associated phase noise may well be already acceptable. A more attractive way of scaling the VCO power consumption without sacrificing the oscillation amplitude is to adopt a transformer-based solution, as devised by Bevilacqua *et al.* [4]. This approach has been recently refined by Li *et al.* [5] to design a VCO with a truly remarkable tuning range and phase noise performance. Notwithstanding the merits of these works, it is obvious that transformer-based VCOs are more complex, and take up more area, than a much simpler inductor-based VCO.

In the design presented in this paper, power scalability is achieved by modifying the oscillator topology, while preserving the traditional LC tank built around a single coil[1] [6]. The idea is to be able to switch from a single cross-coupled switch-pair (either N- or P-type) oscillator topology, to one making use of a complementary cross-coupled pair (both N- and P-type). As shown in [8], these two topologies are ideally capable of the same peak FoM, but they attain it at different levels of current consumption. As a result, their lowest achievable phase noise is also different: the single-switch-pair topology is capable of a 6 dB lower phase noise, paid by a four times higher power consumption. Using this approach, the design of a power-scalable VCO having a constant FoM becomes possible.

The paper is organized as follows: in Section II, a brief analysis of the phase noise requirements for mobile TXs is reported; the power efficiency of traditional LC-tank oscillator is discussed in Section III, while the proposed solution is described in Section IV, and a detailed description of the circuit implementation is shown in Section V; finally, Section VI discloses the most important measurement results.

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A. Liscidini is with the Electrical and Computer Engineering Department, University of Toronto, Toronto, ON, M5S 3G4 Canada.

L. Fanori is with the Department of Electrical and Information Technology, Lund University, SE-22100 Lund, Sweden, and also with Marvell Italy, 27100 Pavia, Italy.

P. Andreani is with the Department of Electrical and Information Technology, Lund University, SE-22100 Lund, Sweden.

R. Castello is with the Dipartimento di Elettronica, Università di Pavia, 27100 Pavia, Italy.

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[1]It should be noted that a traditional single-coil LC tank can nevertheless be optimized in more or less advanced ways, e.g., by enhancing the trade-off between channel resistance and parasitic capacitance of the MOS switches used in discrete capacitive frequency tuning [7].

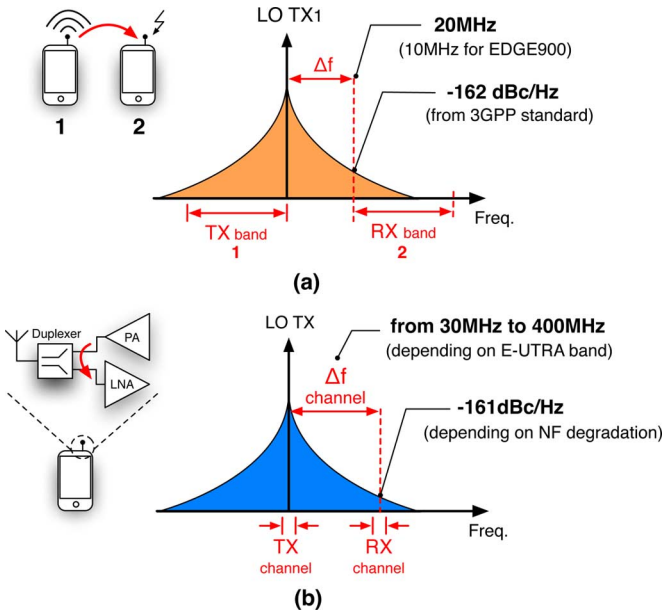

Fig. 1. Worst-case scenarios for phase-noise TX specifications: (a) GSM TDD standard; (b) WCDMA FDD standard.

II. Phase Noise Requirements for Multi-Standard Mobile Terminals

In a cellular TX, the most stringent phase noise requirements are typically derived from the degradation that the transmitted signal can produce on a receiver (RX). In particular, when the system uses time-division-duplex (TDD) like GSM (Fig. 1(a)), the scenario that must be considered is when the phase noise produced by the TX VCO spills over into the receiver band of another handset. The worst case occurs when the GSM transmitter uses the highest channel in the TX band, and the receiver occupies the lowest channel in the RX band. In this case, the phase noise specification $\mathcal{L}_{\mathrm{TDD,GSM}}$ and its frequency offset $\Delta\mathrm{f}$ from the carrier are respectively obtained from the maximum integrated noise $\mathrm{MaxNoise_{RX}}$ that can be tolerated in the channel, and from the distance between TX and RX bands. In particular, we can write

$$\mathcal{L}_{\mathrm{TDD,GSM}}(\Delta f) = \mathrm{MaxNoise}_{RX}|_{\mathrm{dBm}} - \mathrm{BW_{RX}}|_{\mathrm{dBHz}} - \mathrm{PW_{TX}}|_{\mathrm{dBm}} \quad (1)$$

where $\mathrm{BW_{RX}}$ is the RX channel bandwidth, and $\mathrm{PW_{TX}}$ is the highest allowed TX power. According to the 3 GPP standard [9], $\mathrm{MaxNoise_{RX}}$ is -79 dBm over the channel bandwidth of 100 kHz, while $\Delta\mathrm{f}$ is 20 MHz and $\mathrm{PW_{TX}}$ is $+33$ dBm. With these data, $\mathcal{L}_{\mathrm{TDD,GSM}}$ is calculated from (1) at -162 dBc/Hz at 20 MHz offset from the 900 MHz carrier.

In the case of an FDD architecture (e.g., WCDMA), the scenario that defines the TX phase noise requirements is when the TX signal leaks into the RX path of the same terminal (Fig. 1(b)). The distance between TX and RX channels sets $\Delta\mathrm{f}$, while the amount of phase noise is similarly defined as in (1). However, in this case the maximum noise tolerated by the RX is not defined by 3 GPP, but rather depends on the targeted RX noise figure (NF) and the duplexer adopted between antenna and transceiver [1]. An example considering a (maximum) TX power of 26 dBm and a TX-to-RX duplexer attenuation of 45 dB is reported in Fig. 1(b).

Considering all FDD and TDD cases and the operative band reported by E-UTRA, it is possible to compile the chart shown in Fig. 2, where all phase noise specifications have been normalized to an oscillation frequency of 2 GHz and a frequency offset of 20 MHz for ease of comparison. These specifications vary by more than 10 dB across the bands, from the most challenging of the 900 MHz GSM, to the most relaxed of the WCDMA band I. Even if an adequate tuning range could be achieved, it is impossible to cover all these bands in a power-optimized way without the availability of a dedicated power-scalable VCO. This is because the very severe phase noise constraints set by GSM would result in a large power waste in all other cases.

III. Power Efficiency Versus Phase Noise in Traditional LC Oscillators

For a given LC tank, optimized in terms of quality factor (Q) and tuning range, the phase noise and power consumption of traditional cross-coupled LC oscillators (either single-switch-pair or complementary) can be scaled only acting on the dc bias current. As shown in Fig. 3, a doubling of the bias current $\mathrm{I_{bias}}$ reduces the phase noise $\mathcal{L}$ by 6 dB, following the equation [10]

$$\mathcal{L}(\Delta\omega) = 10\log_{10}\left[\frac{kT}{Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{I_{\mathrm{bias}}^2 R}\frac{\pi^2}{8}(1+\gamma+F_{\mathrm{bias}})\right] \quad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, ω_0 is the angular oscillation frequency, $\Delta\omega$ is the angular frequency offset from the carrier, R is the equivalent parallel tank resistance, γ is the channel noise factor of the MOS device working in the active region, and $\mathrm{F_{bias}}$ is a factor accounting for the noise injected by the bias current generator into the tank. Equation (2) is valid until the oscillator amplitude reaches its maximum $\mathrm{V_{out,max}}$, where the phase noise reaches a minimum. Furthermore, (2) indicates that the phase noise contribution of the cross-coupled MOS pair is always in the same proportion γ:1 to the phase noise contributed by the parallel tank resistance, independently of the dc current drawn by the VCO. This result is in fact intrinsically guaranteed in any well-behaved current-biased class-B or class-C harmonic oscillator [11]–[13].[2]

Looking at the plot in Fig. 3, the introduction of power scalability in the oscillator may appear straightforward, and indeed it is, via a programmable $\mathrm{I_{bias}}$. However, as will be shown in the following, the simple tuning of $\mathrm{I_{bias}}$ results in a sub-optimal power efficiency and a limited range of power scalability.

A. Harmonic Oscillator Efficiency vs. DC-Bias Current

The oscillator efficiency can be studied using its FoM, which normalizes the oscillator phase noise to its power consumption $\mathrm{P_{diss}}$ [15]. The FoM is defined as

$$\mathrm{FoM} = -10\mathrm{Log}\left[\left(\frac{\Delta\omega}{\omega_0}\right)^2 \cdot \frac{\mathcal{L}(\Delta\omega)}{P_{\mathrm{diss}}} \cdot 1\ \mathrm{mW}\right] \quad (3)$$

[2]We notice that different results are obtained in voltage-biased class-D oscillators [14].

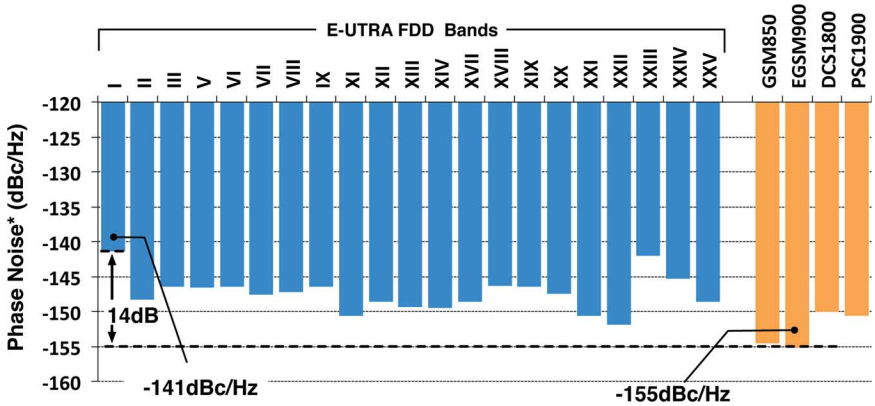

Fig. 2. Summary of phase noise specifications for all GSM/EDGE and E-UTRA bands (normalized to a 2 GHz carrier frequency and a frequency offset of 20 MHz).

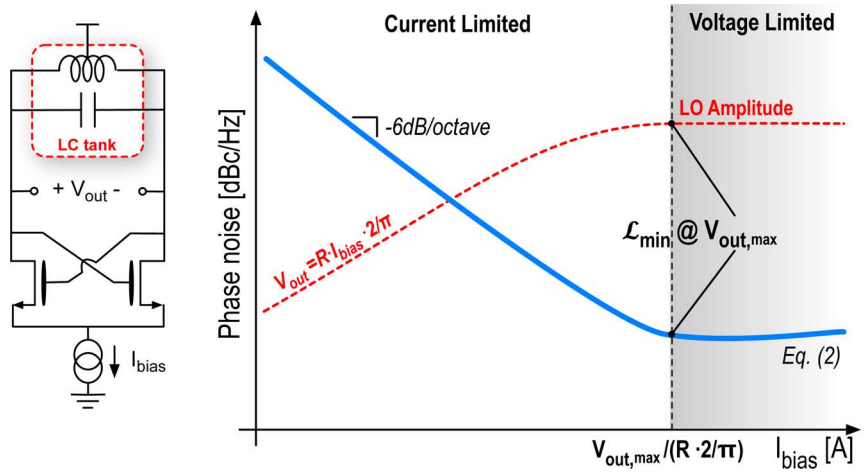

Fig. 3. Phase noise vs. bias current for a standard LC oscillator.

and a qualitative plot of FoM vs. I_{bias} for typical LC oscillators is reported in Fig. 4. When I_{bias} is doubled, the phase noise decreases by 6 dB following (2), while P_{diss} (i.e., $V_{dd} \times I_{bias}$) increases only by 3 dB, leading to a FoM improvement of 3 dB/octave with respect to I_{bias}. The peak FoM, which corresponds to the minimum phase noise, is reached when the oscillation amplitude cannot increase any longer. The fact that FoM is dependent on I_{bias} shows that a simple current tuning is not an efficient way of trading P_{diss} for phase noise. Furthermore, since the best power efficiency (i.e., the best FoM) occurs for the lowest achievable phase noise, which is required only in the aforementioned worst-case scenario, the oscillator would work in a power-wasting regime for most of the time.

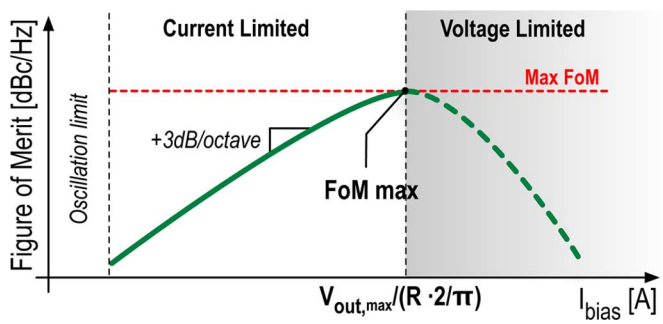

Fig. 4. Figure-of-merit (FoM) vs. bias current for a standard LC oscillator.

B. Power Scalability Plot

The efficiency of an oscillator in terms of power scalability can be appreciated in the log-log plot of Fig. 5, where P_{diss} is a function of the demanded phase noise The solid curve, with a slope of 1/2, represents the case of a classic LC-tank oscillator, where the phase noise scales by 6 dB when P_{diss} is halved. The dashed line with a unity slope, on the other hand, describes the best possible case, where the efficiency is kept constant while P_{diss} is varied. Both curves start from the same point, where the phase noise is lowest and both P_{diss} and FoM are highest. The same plot highlights also the power scalability range, defined as the ratio between the maximum usable power (P_{max}, when the oscillator enters the voltage-limited region) and the minimum usable power (P_{min}, when the oscillation dies out).

As it is clear from Fig. 5, the capability of an LC-tank oscillator to be reconfigured in terms of power without changing the tank configuration is quite limited, and far from the optimal line of maximum power efficiency. Changing the tank impedance while scaling P_{diss}, on the other hand, would ideally allow a close-to-optimal operation; this, however, would entail the use of at least two inductors, if different impedance levels

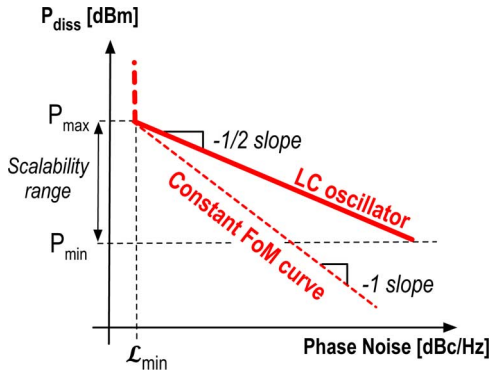

Fig. 5. Power scalability plot for a standard LC oscillator.

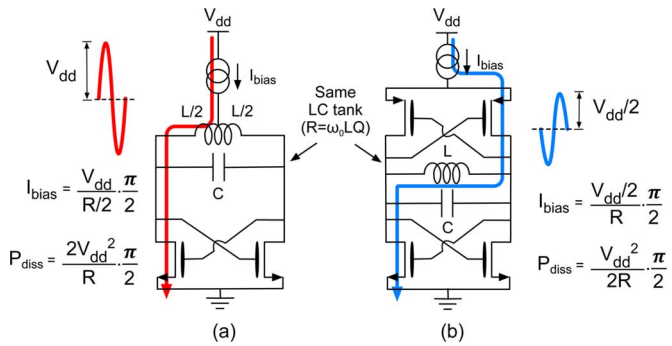

Fig. 6. (a) Single cross-coupled-pair and (b) complementary cross-couple-pair LC oscillators.

are wished at the same oscillation frequency, with the unavoidable Q degradation due to the additional MOS devices needed to switch on and off an extra inductor.

In the next section, we show that the path leading to an optimal power scalability is not via the tank, but indeed via the oscillator topology itself.

IV. A Power-Scalable LC Oscillator

The idea of an efficient power-scalable oscillator starts from the comparison between the single cross-coupled-pair and the complementary cross-couple-pair LC oscillators reported in Fig. 6. If built around the same tank, these two topologies have two main differences: maximum oscillation amplitude (which corresponds to both minimum phase noise and maximum FoM), and DC current I_{bias} needed to achieve it.

Neglecting the voltage drop across the current generators, the single-pair topology allows a maximum oscillation amplitude that is double that of the complementary topology, since in the latter the oscillation is confined between ground and V_{dd}, while in the former the oscillation can climb up to $2V_{dd}$. Thus, the complementary topology reaches a minimum phase noise that is 6 dB higher than in the single-pair topology. This penalty in terms of minimum phase noise is traded off with a higher current efficiency. In fact, in the complementary oscillator I_{bias} flows through the entire tank (reversing direction each semi-period of oscillation), instead of only half of it, as in the single-pair oscillator. As a consequence, to achieve its maximum oscillation amplitude (and minimum phase noise), the complementary oscillator requires only one quarter of the current needed by the

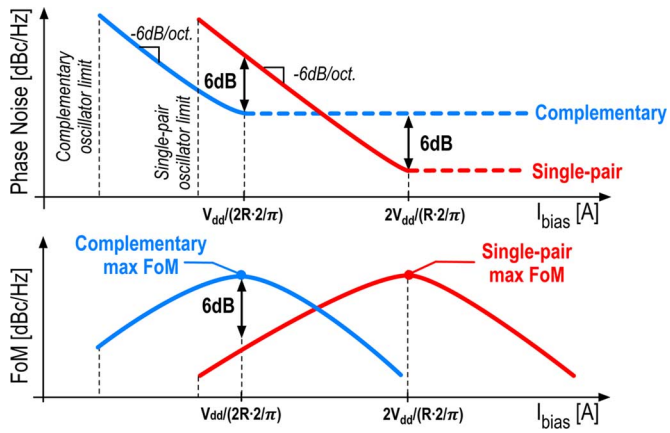

Fig. 7. Phase noise and FoM plots for both single-pair and complementary-pair LC oscillators.

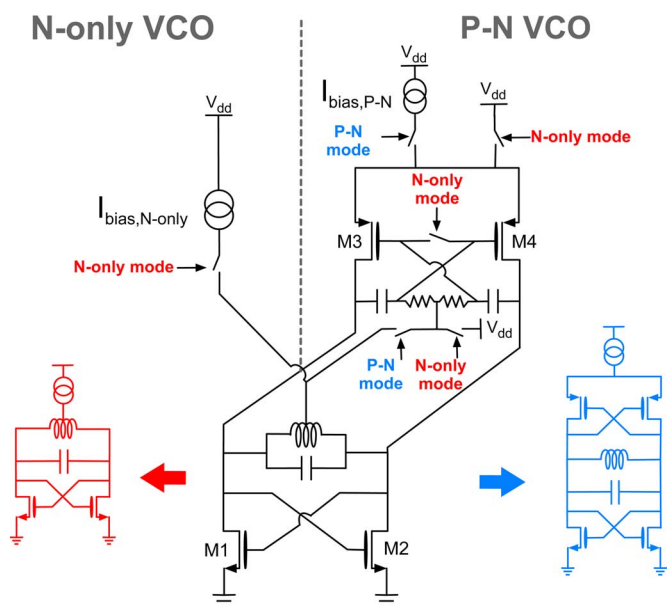

Fig. 8. Simplified schematic view of the power-scalable oscillator.

single-pair oscillator, assuming that V_{dd} is the same. The notable result is that the two configurations display the same FoM, since the complementary topology has a 6 dB higher phase noise with a 6 dB lower P_{diss} [8]. Fig. 7 shows the qualitative plots of phase noise and FoM vs. I_{bias} for both oscillators, summarizing the above analysis. These plots suggest a straightforward way of building an efficient power-scalable oscillator: switch from single-pair to complementary topology, while keeping the same LC tank, when a relaxed phase noise specification (by at least 6 dB) is allowed, saving 75% of the P_{diss} required by the single-pair oscillator, and maintaining a basically invariant FoM.

Fig. 8 shows the simplified schematic view of the power-scalable VCO, where the complementary P-N topology (on the right) is merged with the N-only topology (on the left) sharing the same tank. The P-N topology is obtained by turning on the P-N mode control bit, which activates $I_{bias,P-N}$ and biases the gate of M3/M4 at a voltage equal to that of the central tap of the inductor. In a similar way, the N-only topology is activated by turning on the N-only mode control bit, which switches

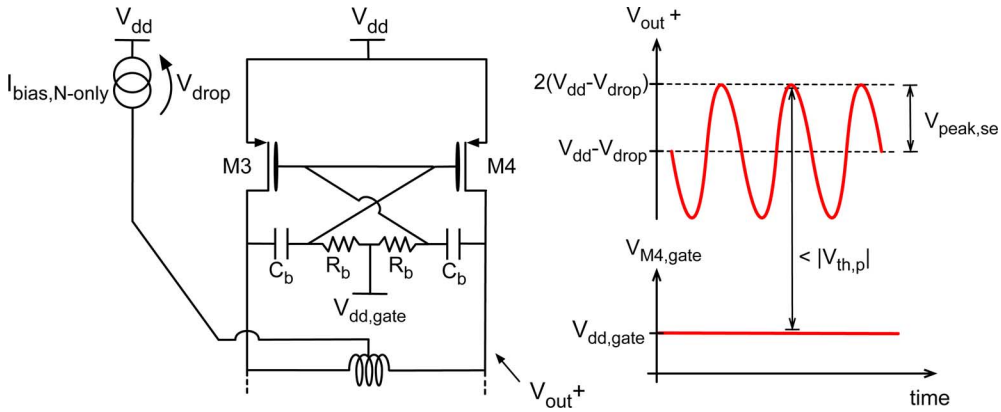

Fig. 9. Ideal voltage waveforms for single-ended output $V_{out}+$ and gate of M4 (or M3) in N-only mode.

off M3/M4 and turns on the current source $I_{bias,N-only}$, which feeds the VCO from the central tap of the inductor.

While the above reconfiguration from N-only to P-N topologies is straightforward in principle, its implementation is not. The main issue is to ensure that M3/M4 are safely turned off across the whole oscillation period when the oscillator operates in N-only mode, to avoid a serious degradation of the tank Q. Adding an AC coupling between drain and gate of M3/M4 and biasing the gate of M3/M4 to V_{dd} is not sufficient, because the oscillation goes well above V_{dd}, and pushes M3/M4 into conduction when the voltage difference between drain and gate is higher than a PMOS threshold voltage $|V_{th,p}|$ (in which case P-MOS drain and source swap place, compared to what indicated in Fig. 8). This creates a trade-off between oscillation amplitude and average tank Q, deteriorating the lowest achievable phase noise level.

Such a trade-off may be avoided by connecting the M3/M4 gates to a voltage higher than V_{dd} when M3/M4 are in the off state. This, however, requires an extra DC voltage $V_{dd,gate}$ that must be well above the oscillation peak (and equal to $2V_{dd} - |V_{th,p}|$ for a maximum peak single-ended oscillation amplitude $V_{peak,se}$ equal to V_{dd}), which may not be available on the transceiver chip.

To solve this problem without resorting to an extra dc voltage, the proposed VCO combines two different techniques (Fig. 8). The first is to place the bias current generators between power supply and oscillator, instead of between the sources of the N-MOS switching pair and ground. This reduces the DC voltage at the output nodes of the oscillator, allowing a larger oscillation amplitude before M3/M4 are turned on. As shown in Fig. 9, the maximum $V_{peak,se}$ in N-only mode becomes $V_{dd}-V_{drop}$, where V_{drop} is the voltage drop across the current generator. To ensure that M3/M4 are not turned on in N-only mode, V_{drop} should be higher than $(2V_{dd}-V_{dd,gate}-|V_{th,p}|)/2$, which corresponds to $V_{peak,se} = (V_{dd,gate}+|V_{th,p}|)/2$. As an example, assuming $V_{th,p} = -0.5$ V and $V_{dd} = V_{dd,gate} = 1.5$ V, V_{drop} has to be greater than 0.5 V, and the maximum $V_{peak,se}$ is equal to 1 V. In practice, a slightly lower V_{drop} than the above can be used, while still keeping the phase noise contribution of M3/M4 negligible. This allows a larger $V_{peak,se}$, yielding a lower phase noise and a higher FoM.

The second technique adopted is the introduction of an RC network, tunable by the P-MOS switch M5 (Fig. 10), to control the oscillation swing at the gate of M3/M4, reducing it when the oscillator works in N-only mode [6]. When operating in P-N mode (Fig. 11), the common source of M3/M4 is connected to $I_{bias,P-N}$, while the DC voltage at the gate is forced to be equal to the voltage at the center tap of the tank inductor, i.e., to the common-mode voltage at the VCO output. At the same time, switch M5 is turned off, and the cut-off frequency of the AC-coupling circuit between drain and gate is equal to $1/(C_bR_b)$. Choosing R_b large enough to set the cut-off frequency well below ω_{LO}, the oscillation at the gate of M3/M4 exhibits the same swing as the oscillation at the tank output, ensuring that the phase noise contribution of M3/M4 is as low as in a standard complementary oscillator [12].

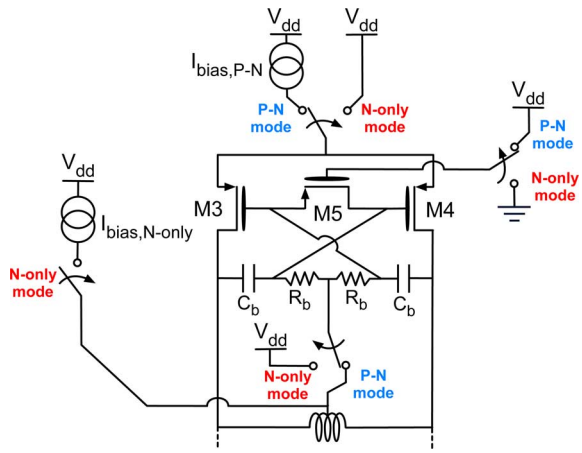

Fig. 10. Bias circuitry for the reconfigurable power-scalable oscillator.

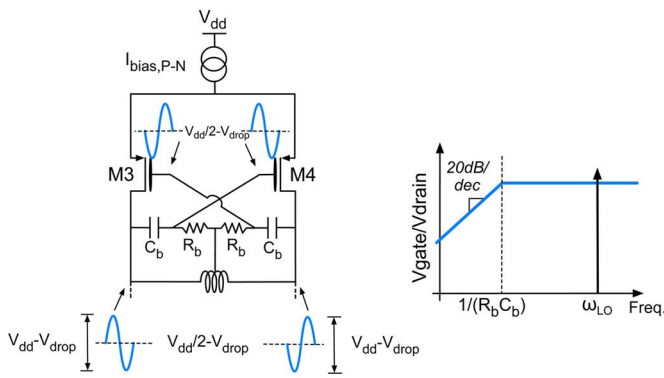

Fig. 11. Bias circuit in P-N mode.

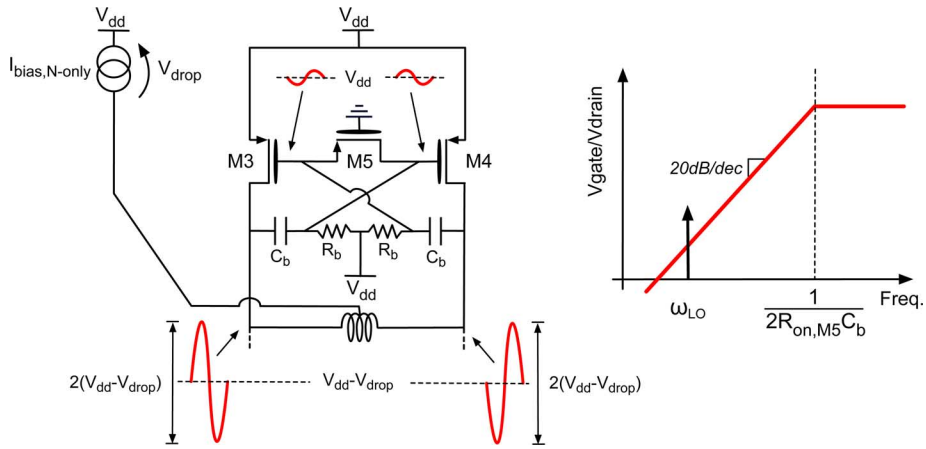

Fig. 12. Bias circuit in N-only mode.

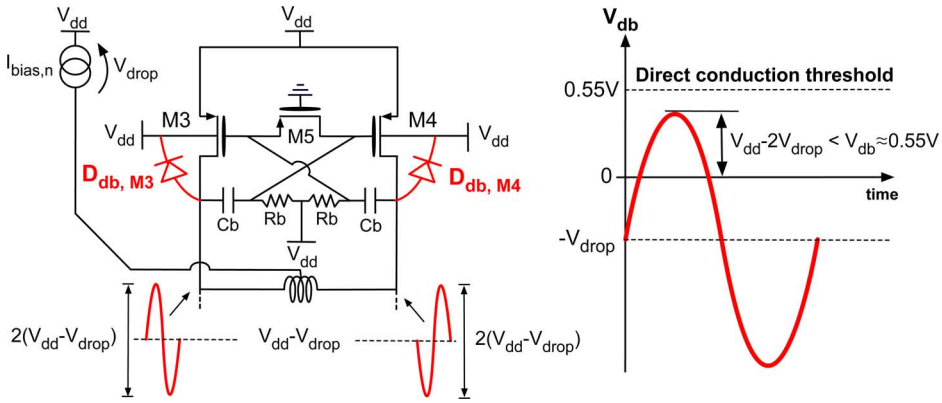

Fig. 13. P-MOS drain-to-bulk diodes in N-only mode.

In the N-only mode of operation, both source and gate of M3/M4 are biased to V_{dd}, and M5 is turned on (Fig. 12). In this case, the cut-off frequency of the ac-coupling network becomes $2/(C_b R_{on,M5})$, where $R_{on,M5}$ is the on-resistance of M5. $R_{on,M5}$ is chosen small enough to guarantee a sufficient attenuation between tank output and the gate of M3/M4, thereby keeping M3/M4 in the off-state. Notice that minimizing $R_{on,M5}$ also maximizes the Q of the circuit made of the series of C_b and $R_{on,M5}$, making its impact on the overall tank-Q negligible. Since the series of the two AC-coupling capacitances C_b is in parallel to the tank, the maximum oscillation frequency in N-only mode is a slightly lower than in P-N mode.

When operating in N-only mode, an additional issue is to keep reverse-biased the drain-to-bulk diodes of the turned-off P-MOS transistors M3/M4 over the entire oscillation period, again to avoid degradation of the tank-Q. This requires that the voltage across these diodes should never exceed their activation voltage $V_{db} \approx 0.55$ V (Fig. 13), imposing a second limit to the minimum value of V_{drop}, which has to be greater than $(V_{dd} - V_{db})/2$ as well. However, since typically $V_{th,p}$ is lower than V_{db}, this new requirement on V_{drop} is automatically satisfied, once the previous one is.[3]

In the proposed VCO, power re-configurability has been combined with the flexibility of a digitally controlled oscillator (DCO). The approach adopted here is the dither-less one proposed in [16], which makes use of a capacitively degenerated N-MOS pair, as shown in Fig. 14. In this way, the capacitance C_{fine} is reflected in parallel to the LC tank shrunk by a factor proportional to $gm_N/(\omega_{LO} C_{cal})$, where gm_N is the N-MOS transistor transconductance averaged over one oscillation period, while C_{cal} is the total capacitance between the N-MOS sources. The circuit of Fig. 14 differs from the one reported in [16] with respect to the way the trimming of the shrinking factor is implemented. In Fig. 14, this is achieved acting on C_{cal}, as opposed to using the N-MOS bias current (i.e., gm_N). In this way, DCO frequency resolution and current consumption can be scaled independently of each other. Furthermore, the extra phase noise contribution from the additional current source in [16] is eliminated.

V. DCO Prototype

A prototype of the proposed DCO, based on the circuit in Fig. 15, has been realized in a 55 nm CMOS process. The DCO has been tailored to GSM/WCDMA applications, assuming a frequency divider by either 2 or 4 at its output, to avoid TX pulling. The resulting oscillation frequency is tunable between 6.5 and 9.0 GHz. The total area occupation is 0.7 mm × 0.7 mm, including the oscillator core, the current sources, and a frequency divider-by-2. The chip micrograph is shown in Fig. 16.

The tank employs a differential inductor of 250 pH, with a simulated Q of 15 at 7 GHz. The coarse frequency tuning is

[3]We notice that the loading effect of M3/M4 in N-only mode was neglected in [6], where only the associated drain-to-bulk diodes were discussed.

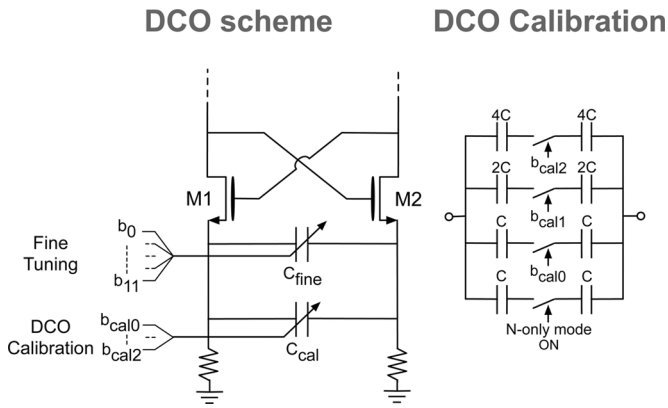

Fig. 14. Fine-tuning circuitry in the DCO.

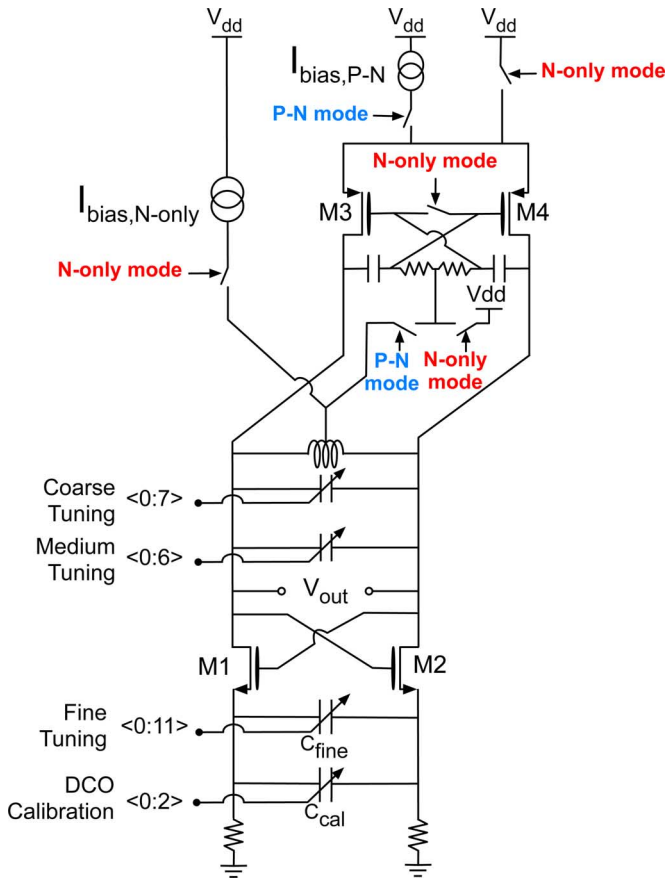

Fig. 15. Final schematic view of the DCO.

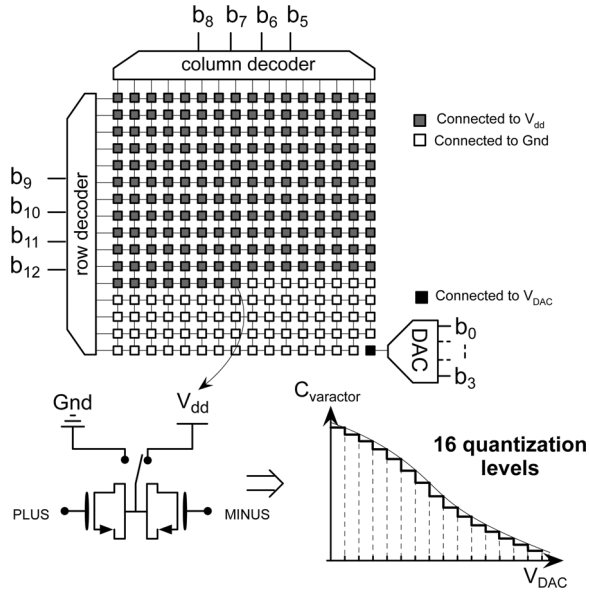

Fig. 16. Chip micrograph.

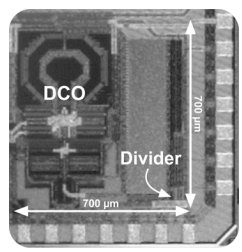

Fig. 17. Fine-tuning varactor array.

common to both n-only and p-n VCOs, and is performed with one coarse-tuning and one medium-tuning capacitor bank, controlled by 7 and 6 bits and achieving a frequency resolution of 20 MHz and 1.4 MHz respectively, with a large overlap between the two banks.

The third, fine-tuning capacitor bank, placed between the two sources of M1 and M2, is controlled by 12 bits, and refines the frequency resolution step down to less than 1.5 kHz, ensuring at the same time a fine tuning range large enough to cover at least 2 medium-tuning steps. As shown in Fig. 17, the 8 MSBs of the 12 fine-tuning bits implement a thermometric control of a 16×16 varactor array, where each varactor is biased either to V_{dd} or to ground; the 4 LSBs, on the other hand, feed a resistive-ladder DAC, which provides 16 equally-spaced voltage levels between V_{dd} and ground: the output of this DAC is used to control the bias voltage of an additional varactor. Since the varactor size in the array is large enough to ensure a good matching, the DAC acts always on the same varactor, without the need of dynamic element matching.

To allow calibration of the fine frequency resolution, the capacitance placed between the sources of M1 and M2 (controlling the shrinking factor of the DCO) can be varied under the control of a 3-bit word. The calibration capacitance C_{cal} can be tuned between 0.4 pF and 2.4 pF in N-only mode, and between 0.1 pF and 2.1 pF in P-N mode. To ensure proper operation of the capacitance shrinking circuit, two degeneration resistances are inserted between the source of M1/M2 and ground (Fig. 15), with value tunable between 10 Ω and 30 Ω.

The high output swing in N-only mode imposes the use of 1.8 V thick-oxide devices for the N-MOS switching pair M1/M2, with a (minimum) length of 220 nm. On the other hand, the lower output swing in P-N mode allows the use of faster standard 1.2 V P-MOS devices for M3/M4, with the minimum channel length of 55 nm; moreover, it is sufficient that the width of M3/M4 sustains the maximum current drained in P-N mode, which, being only 1/4 of that in N-only mode, allows M3/M4 to be quite small.

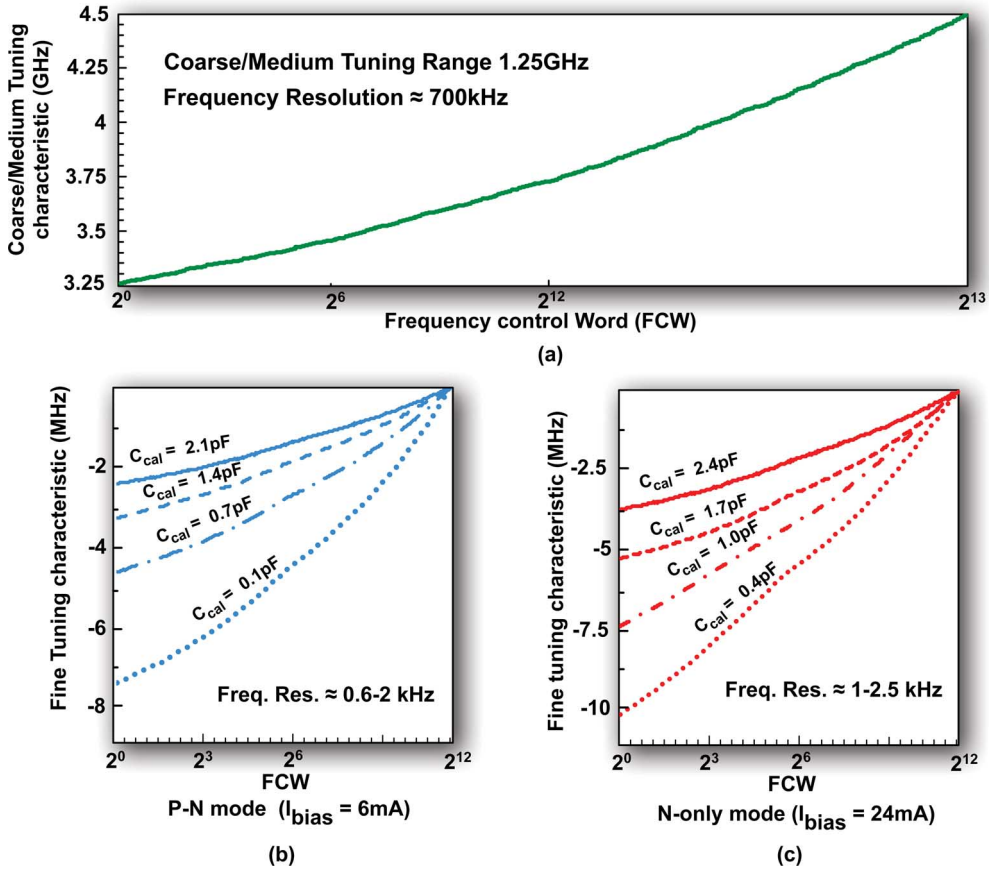

Fig. 18. Tuning characteristics at the output of the on-chip divider-by-2: (a) Coarse/medium tuning; (b) fine tuning in P-N mode; (c) fine tuning in N-only mode.

The two current sources $I_{bias,N-only}$ and $I_{bias,P-N}$ are implemented as current DACs, both controlled by a 6-bit word. They consist of P-MOS current mirrors with a highly tunable ratio, which is required to match the amplitude and phase noise performance in the two modes of operation across all supported bands. With a reference current of 0.8 mA, provided off-chip and filtered on-chip, $I_{bias,N-only}$ has a tunable output current between 4.4 mA and 30 mA in steps of 0.4 mA, while the current provided by $I_{bias,P-N}$ is tunable between 1.1 mA to 7.5 mA in steps of 0.2 mA.

The voltage drop across $I_{bias,N-only}$ is around 0.5 V at the nominal current consumption of 24 mA in N-only mode. This is large enough to keep M3/M4 in the off-state across the oscillation period in N-only mode. Finally, the DCO is buffered with a frequency divider-by-2 (using the topology proposed in [17]) to simplify the measurement setup.

VI. Measurement Results

The DCO oscillates between 6.5 GHz and 9.0 GHz, for a 33% tuning range. Fig. 18(a) shows the measured coarse/medium tuning characteristic at the output of the on-chip divider-by-2. The fine-tuning range is programmable from 2.5 MHz to 7.5 MHz in P-N mode (Fig. 18(b)), with a corresponding frequency resolution from 0.6 kHz to 2 kHz, and between 4 MHz and 10 MHz in N-only mode, with a corresponding frequency resolution of 1 kHz to 2.5 kHz (Fig. 18(c)).

TABLE I
Summary of DCO Performance

Parameter	P-N Mode	N-only Mode
DCO Frequency	6.5-9 GHz	
Coarse Tuning Range	2.5 GHz (33%)	
Coarse Frequency Resolution	1.4 MHz	
Fine Tuning Range[(a)]	5 to 15 MHz	8 to 20 MHz
Fine Frequency Resolution[(a)]	1.2 to 4 KHz	2 to 5 KHz
Power Supply	1.5 V	1.5 V
Current Consumption	6 mA	24 mA
Phase Noise 3.92GHz @ 2MHz[(b)]	-129.3dBc/Hz	-134.7dBc/Hz
FoM[(b)]	185.6dBc/Hz	185dBc/Hz
Power scalability range	from 6.75mW to 36mW	
Technology	55 nm CMOS	

(a) Programmable by the capacitance C_{cal}
(b) After an on-chip divider by 2

Fig. 19 plots the phase noise measurements, performed with a supply voltage of 1.5 V. In N-only mode, the DCO displays a phase noise of −134.7 dBc/Hz at 2 MHz offset from the 3.92 GHz carrier, which extrapolates to −166.7 dBc/Hz at 20 MHz offset after a further frequency division by 4 and

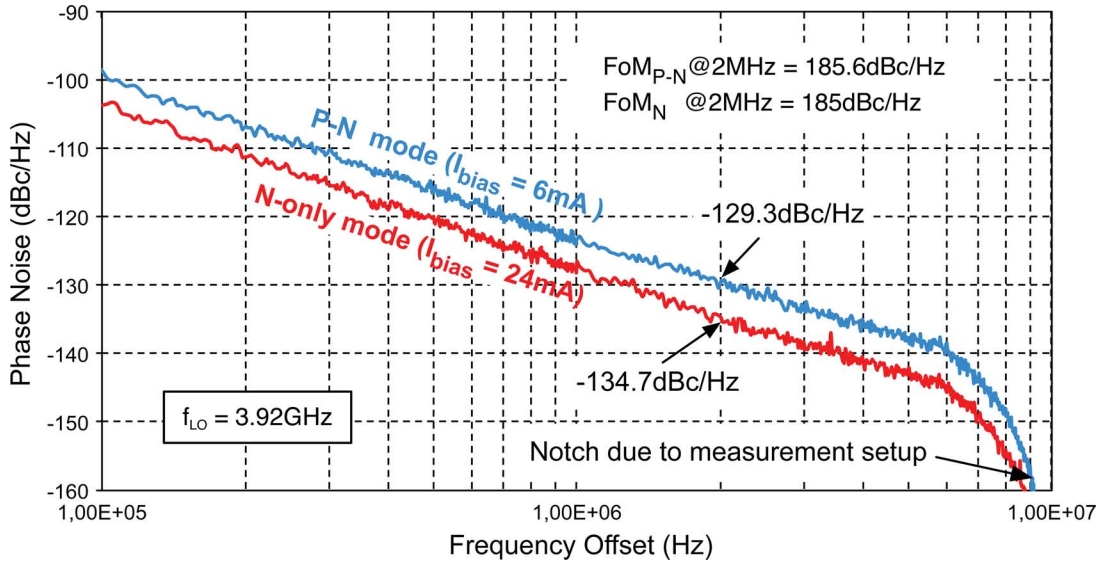

Fig. 19. Phase noise measurements in P-N mode and N-only mode at the output of the on-chip divider-by-2.

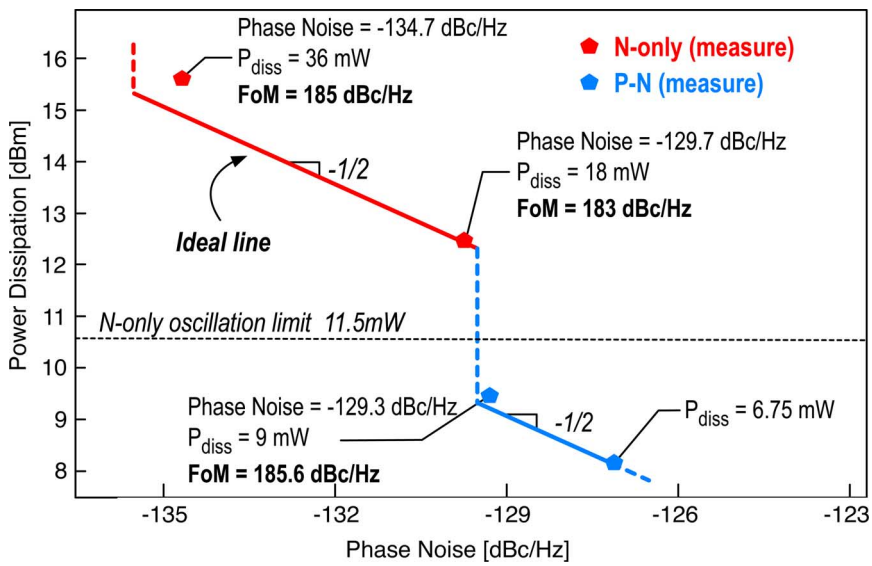

Fig. 20. Power-scalability plot for the reconfigurable DCO.

assuming a 20 dB/dec slope. The most exacting phase noise specification for the GSM transmitter (i.e., the already mentioned -162 dBc/Hz at 20 MHz offset from 900 MHz) is expected to be met with a margin of 4.7 dB. The $1/f^3$ noise corner is close to 400 kHz. The optimal current consumption is 24 mA, which results in a FoM of 185.0 dBc/Hz. In P-N mode, the DCO achieves a phase noise of -129.3 dBc/Hz at 2 MHz offset from the 3.92 GHz carrier. With an optimal current consumption of 6 mA, the FoM in P-N mode is 185.6 dBc/Hz. The phase noise difference between the two DCOs is 5.4 dB, very close to the theoretical value of 6 dB associated to the fourfold difference in bias currents.

Fig. 20 shows the power scalability plot of the DCO. The power consumed by the DCO ranges from 36 mW to 6.75 mW, with a phase noise variation between -134.7 dBc/Hz and -127.0 dBc/Hz. From 36 mW to 18 mW, the oscillator works in N-only mode: the power consumption is reduced acting on the bias current, resulting in a FoM loss of 2 dB in the worst case. After that, the DCO topology is changed from N-only to P-N, greatly reducing the power consumption but leaving the phase noise almost unchanged. In this way, a much higher efficiency is restored. The current consumption in P-N mode can be scaled down farther, reaching a minimum power dissipation of 6.75 mW before the oscillation dies out. The plot reports also the minimum power of 11.5 mW at which the N-only topology can oscillate, which is approximately twice as high as that needed by the P-N topology, as predicted by theory. Finally, Table I summarizes the DCO performance in both modes of operation, while Table II compares the DCO with several published oscillators with a tuning range of at least 15% and meeting the GSM TX noise specification at 20 MHz offset from the carrier.

TABLE II
COMPARISON WITH STATE-OF-THE-ART CELLULAR TRANSMITTER VCOS HAVING A TUNING RANGE OF AT LEAST 15%

	Vdd (V)	Tech. (nm)	Frequency (GHz)	PN (dBc/Hz)	Estimated PN @20MHz from 915MHz (dBc/Hz)	Pdc (mW)	FoM (dBc/Hz)
This work (power scalable)	**1.5**	**55**	**6.5-9.0 (33%)**	**-134.7 @2MHz[(a)] from 3.9GHz**	**-168**	**36**	**185**
				-129.3 @2MHz[(a)] from 3.9GHz	**-162**	**9**	**185.6**
Fanori, *ISSCC'12* [18]	1.5	55	6.7-9.2 (32%)	-137 @2MHz from 4GHz[(a)]	-170	27	188/189
Dal Toso, *JSSC'10* [19]	1.2	65	13-15 (15%)	-133 @3MHz from 3.6GHz[(b)]	-162	8.4	185
Li, *JSSC'12* [5]	0.6	65	2.5-5.6 (76%)	-157 @20MHz from 3.6GHz	-169	13.5	188/192
Fanori, *JSSC'13* [20]	0.4	65	3.0-4.8 (46%)	-150 @10MHz from 3.0GHz	-166	6.8	191
Babaie, *ISSCC'13* [21]	1.25	65	2.9-3.8 (25%)	-142 @3MHz from 3.7GHz	-169	15	192
Staszewski, *JSSC'05* [22]	1.4	90	3.2-4.1 (25%)	-165 @20MHZ from 915MHz[(b)]	-165	25.2	183
Fanori, *JSSC'13* [23]	1.2	90	3.4-4.5 (28%)	-147 @10MHz from 3.9GHz	-166	6.6	191
Andreani, *JSSC'11* [1]	1.2	90 RF	2.6-4.1 (46%)	-156 @20MHz from 3.7GHz	-168	22.8	188
Ruippo, *MWCL'10* [24]	1.2	130	2.9-5.4 (60%)	-126 @1MHz from 3.6GHz	-164	9.8	185/190

(a) after division by 2

(b) After division by 4

VII. CONCLUSION

In this paper, a power-scalable oscillator tailored to GSM and WCDMA applications has been presented. The design combines single (N-only) and complementary (P-N) cross-coupled switch-pair topologies in order to scale simultaneously phase noise and power consumption, preserving a constant power efficiency and an optimal FoM. Measurements on a 55 nm CMOS oscillator prototype confirm the theoretical analysis and demonstrate an optimal power scalability.

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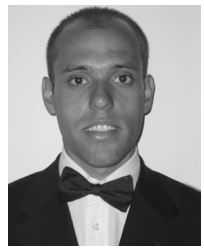
Antonio Liscidini (S1999–M2006–SM'13) was born in Tirano, Italy, in 1977. He received the Laurea degree (*summa cum laude*) and the Ph.D. in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was a summer intern at National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS LNAs. From 2008 to 2012, he was an Assistant Professor at the University of Pavia and consultant for Marvell Semiconductors in the area of integrated circuit design. Since December 2012, he has been an Assistant Professor in the Edward S. Rogers Sr. Department of Electrical and Computer Engineering of the University of Toronto, Ontario, Canada. His research interests are in the implementations of transceivers and frequency synthesizers for cellular and ultra low power applications.

Dr. Liscidini received the Best Student Paper Award at IEEE 2005 Symposium on VLSI Circuits and the Best Invited Paper Award at 2011 IEEE Custom Integrated Circuit Conference. From 2008 to 2011, he served as Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS and he served as Guest Editor of IEEE JOURNAL OF SOLID STATE CIRCUITS for the special issue on ESSCIRC conference July 2013. Currently, he is member of the TPC of the European Solid-State Circuit Conference (ESSCIRC) and of the IEEE International Solid-State Circuit Conference (ISSCC).



Luca Fanori was born in Pavia, Italy, in 1984. He received the M.Sc. degree in electronic engineering and the Ph.D. in electrical engineering from the University of Pavia, Pavia, Italy.

He was in an internship at Marvell Italy and Ericsson AB in Sweden to design All-Digital-PLL and studying LTE transceiver architectures. After two years of post doc at Lund University, he currently works for Marvell Italy, where his research activities are focused on the implementations of frequency synthesizers.

Dr. Fanori was a co-recipient of the Best Invited Paper Award at the IEEE 2011 Custom Integrated Circuits Conference (CICC).

Pietro Andreani (M2003–SM2007) received the M.S.E.E. degree from the University of Pisa, Italy, in 1988, and the Ph.D. degree from the Department of Electrical and Information Technology (EIT), Lund University, Sweden, in 1999.

Between 2001 and 2007, he was Chair Professor with the Center for Physical Electronics, Technical University of Denmark. Since 2007, he has been an Associate Professor at EIT, where he is involved with analog/mixed-mode/RF IC design. He is also a part-time IC designer at Ericsson Modems in Lund.

Dr. Andreani has been a TPC member of ISSCC (2007–2012), guest editor of JSSC (Dec. 2012), and is a TPC member of ESSCIRC.

Rinaldo Castello (M'78–SM1992–F1999) graduated from the University of Genova, Italy (*summa cum laude*) in 1977 and received the M.S. and Ph.D. degrees from the University of California, Berkeley, CA, USA, in 1981 and 1984. From 1983 to 1985 he was Visiting Assistant Professor at the University of California, Berkeley. In 1987 he joined the University of Pavia, Italy, where he is now a Full Professor. He consulted for ST-Microelectronics, Milan, Italy, until 2005. In 1998 he started a joint research centre between the University of Pavia and ST and was its Scientific Director up to 2005. He promoted the establishing of several design centre from multinational IC companies in the Pavia area among them Marvell for which he has been consulting from 2005.

Prof. Castello has been a member of the TPC of the European Solid State Circuit Conference (ESSCIRC) since 1987 and of the IEEE International Solid-State Circuits Conference (ISSCC) from 1992 to 2004. He was Technical Chairman of ESSCIRC 1991 and General Chairman of ESSCIRC 2002, Associate Editor for Europe of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1994 to 1996 and Guest Editor of the July 1992 special issue. From 2000 to 2007, he was a Distinguished Lecturer of the IEEE Solid-State Circuits Society. Prof. Castello was named one of the outstanding contributors for the first 50 and 60 years of ISSCC and a co-recipient of the Best Student Paper Award at the 2005 Symposium on VLSI of the Best Invited Paper Award at the 2011 CICC and of the Best Evening Panel Award at ISSCC 2012. He was one of the two European representatives at the Plenary Distinguished Panel of ISSCC 2013.