

A Current-Mode, Low Out-of-Band Noise LTE Transmitter With a Class-A/B Power Mixer

Nicola Codega, *Member, IEEE*, Paolo Rossi, *Member, IEEE*, Alberto Pirola, *Member, IEEE*, Antonio Liscidini, *Senior Member, IEEE*, and Rinaldo Castello, *Fellow, IEEE*

Abstract—A complete SAW-less transmitter meeting LTE requirements is presented. High power efficiency and low out-of-band noise are obtained exploiting fully current operation of an analog baseband followed by a class-A/B power mixer. Out-of-band emissions are limited by filtering noise and DAC replicas right before the signal up-conversion through a current-mode Biquad feeding directly the power-mixer. The transmitter, implemented in 55 nm CMOS technology, shows -158 dBc/Hz RX-band noise emission at 30 MHz offset for LTE10, while consuming 96 and 34 mW from the single 1.8 V power supply at 4 and -10 dBm output power, respectively. ACLR is always below -42 dBc up to 4 dBm for both LTE10 and LTE20.

Index Terms—ACLR, active mixer, baseband, Biquad, class A, class A/B, CMOS integrated circuit, current mode, EVM, high efficiency, long-term evolution (LTE), mobile communications, out-of-band noise, phase noise, radio frequency, 3G, transmitter, voltage mode.

I. INTRODUCTION

INTEGRATED transceivers for long-term evolution (LTE) must process signal bandwidths significantly wider than those of previous mobile standards and require a signal processing even more complicated, entailing high power consumption. Besides being compatible with all of the preexisting communications standards, the new 4G terminals also have to support WiMAX, Wi-Fi, Bluetooth, and GPS. Because of a congested frequency spectrum and the close proximity on the handset board with all of the different systems-on-chip (SOCs), the LTE transceiver must face severe coexistence challenges.

The most critical situation is when the receiver (RX) and transmitter (TX) operate in the same time slot. 3G and 4G standards supporting FDD suffer from this issue. A partial isolation is given by the duplexer that, through the use of two sharp bandpass filters, can de-couple the TX and RX paths from each other. However, due to the finite isolation of the duplexer, a leakage from the TX reaches the RX-path (Fig. 1). There are two problems arising from this leakage which, for large-signal bandwidths as it occurs in 4G, become especially critical. First, the

(attenuated) transmitted signal represents the most critical interferer for the receiver, increasing its linearity requirements, e.g., IIP2, IIP3, 1 dB compression point. Second, the TX leakage that lies in the RX-band directly impacts the receiver sensitivity. The latter problem is traditionally resolved using a surface acoustic wave (SAW) filter at the output of the integrated transmitter and before the external power amplifier (PA), as shown in Fig. 1.

Nowadays, given the increasingly larger number of bands to be supported, the trend is to increase the level of integration of the transceiver and make it reconfigurable while at the same time removing the external nonreconfigurable blocks like the SAW filter. As a consequence, the transceiver must achieve extremely low out-of-band emissions. The main contributors to such unwanted signals are the digital-to-analog converter (DAC) replicas, noise, and nonlinear distortion components. For large-signal bands and narrow TX–RX frequency spacing, the dominant contributor is noise. For the 3G case, improvements in the transceiver TX chain made it possible to eliminate the SAW filters. However, LTE forced to reintroduce them for the most critical working bands, for which the ratio between the RX-to-TX frequency spacing and the signal bandwidth is very small (e.g., about two for LTE20 in Band20). Finally, the use of OFDMA and of complex modulation schemes in 4G leads to up to 9 dB peak-to-average power ratio (PAPR). This mandates high power efficiency and linearity in the entire chain that delivers the signal power to the PA.

State-of-the-art integrated transmitters for mobile communications can be divided in two main groups, depending on the type of up-converter used, i.e., voltage-mode (based on passive mixers) and current-mode (based on active mixers). The first voltage-mode transmitter was implemented by Xin and Van Sinderen [1] and subsequently improved by Giannini *et al.* [2], [3]. The proposed solutions drive the mixer through a filtering stage that attenuates the out-of-band emission (DAC replicas, nonlinearities, and noise), while a pre-PA (PPA) transforms the mixer output RF voltage into current for the LC-tank load. However, the passive mixer approach has three main problems. First, the I and Q paths crosstalk with each other. Second, the input capacitor of the PPA appears as a switched capacitor load for the passive mixer driver [4], which needs to have a sufficiently low output impedance, increasing power consumption. Finally, the mixer switches must bear a very large voltage swing while maintaining high linearity.

On the other hand, current-mode transmitters based on a power mixer that acts as a PA driver [5] are immune from

Manuscript received December 14, 2013; revised March 08, 2014; accepted March 18, 2014. Date of publication April 21, 2014; date of current version June 23, 2014. This paper was approved by Guest Editor Yann Deval. This work was supported by the European M. Curie Grant 251399.

The authors are with Marvell Italy SRL, 27100 Pavia, Italy (e-mail: nicola.codega@gmail.com; ncodega@marvell.com).

Color versions of one or more of the figures in this paper are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/JSSC.2014.2315643

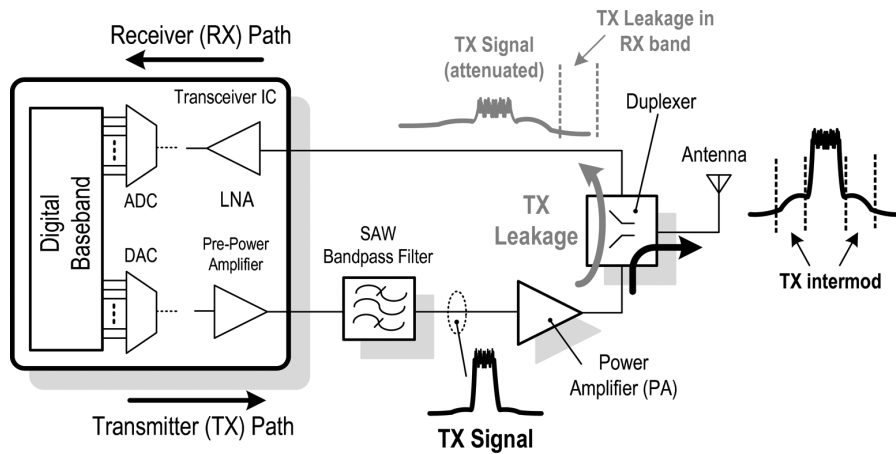


Fig. 1. Traditional block diagram of an integrated transceiver: Usually, nonlinearities corrupt other frequency channels, while out-of-band noise corrupts the integrated receiver.

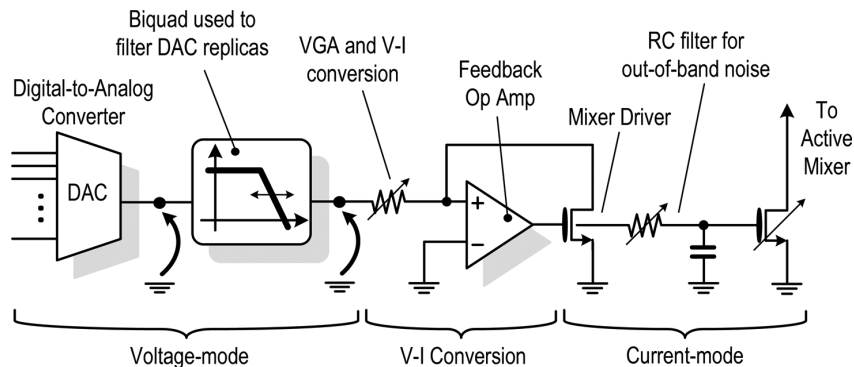


Fig. 2. Traditional mixed-mode baseband implementation of a transmitter using an active mixer.

the aforementioned problems [6], [7]. However, traditionally, the baseband (e.g., DAC and filtering stage) is operated in the voltage domain, while moving into a current mode in front of the power mixer [6], [7]. This creates the necessity of an additional linear voltage-to-current ($V-I$) converter to drive the active mixer, increasing the baseband (BB) power consumption. Moreover, the BB out-of-band noise is only loosely filtered through passive filtering, since there is no place for an active stage with complex poles (and hence sharp filtering and low droop) before the up-converter.

This paper describes a fully current-mode multistandard transmitter operated in class A/B [10] that combines the advantages of the two transmitter types, i.e., reduced noise of the power mixer and the possibility of placing an active filter just before the up converter, as in voltage-mode transmitters. Moreover, the use of a class-A/B approach permits to further reduce noise and increase efficiency. This paper is organized as follows. In Section II, the main building blocks of the proposed current-mode transmitter are introduced in a conceptual way and the advantages of using a class-A/B approach along the chain are explained. Section III details the circuits used in the realized prototype, following the ideas discussed in Section II. Section IV presents the measurements of the realized prototype, comparing them with recent state-of-the-art transmitters. Finally, Section V draws the conclusions of the work.

II. CURRENT-MODE TRANSMITTER: BUILDING BLOCKS

The starting point to develop a fully current-mode TX is the power mixer-based TX presented in [7] and depicted in Fig. 2. In this architecture, DAC and filter operate in voltage mode while the portion of the TX feeding the power mixer in current mode. The $V-I$ conversion is realized after the BB filter by a resistor connected to a virtual ground. The voltage applied to the resistor generates a current that is absorbed by the virtual ground and mirrored into the transconductor of the power mixer [5], [8], [9]. The value of the resistor and the mirror factor can be scaled in order to realize a variable gain amplifier (VGA). In addition, an RC pole is inserted in the mirror to filter the noise generated by the $V-I$ converter.

Fig. 3 shows the steps necessary to modify such an architecture to obtain the proposed fully current-mode transmitter. The voltage DAC is transformed into a current-steering DAC that feeds a scalable current mirror implementing a VGA. Finally, the active low-pass filter is moved at the end of the BB chain before mirroring the signal into the up-converter. Compared to the traditional approach of Fig. 2, placing the filter at the end of the BB chain allows more suppression of the out-of-band noise. In addition, combining the filter with the up-converter driving stage potentially reduces also the power consumption.

Moving toward the RF section, power consumption of the chain is scaled up to lower out-of-band noise and to handle the

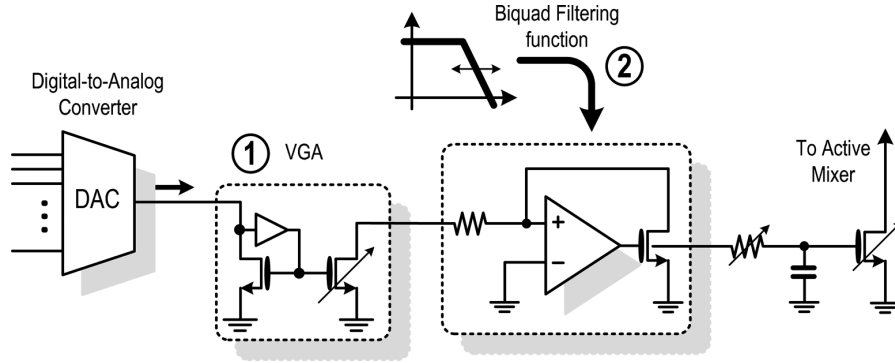


Fig. 3. Two steps to create a current-mode baseband: introduction of a VGA based on a current mirror and Biquad function combined in the active mixer driver.

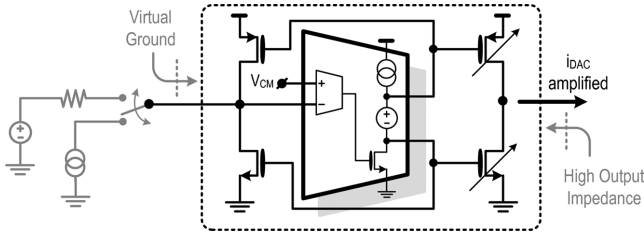


Fig. 4. Conceptual schematic of the proposed VGA.

signal swing, hence, the up-converter is the most power-hungry section of the transmitter. The Biquad/mixer driver, feeding the power mixer in class A/B, lowers the power consumption of the entire chain even more. The building blocks are described in detail below.

A. Variable Gain Amplifier

Since the transmitted signal can have up to 9 dB of PAPR, the use of class-A/B stages allows a significant reduction of the power consumption and out-of-band noise emission compared with a class-A stage (as discussed in Section II-C). For this reason, the VGA is implemented with a class-A/B current mirror that provides also a low input impedance to limit the voltage swing at the DAC output.

The VGA schematic (in its single-ended version) is reported in Fig. 4. The low input impedance is realized closing in feedback an amplifier formed by an OTA followed by a push-pull stage. The current absorbed by the push-pull stage is delivered to the following stage by a programmable mirror. To bias the push-pull input stage and its replica in class A/B, the output stage of the OTA uses the Huijsing floating battery [11] stacked on a common-source amplifier. Notice that the virtual ground, used to absorb the signal from the current DAC, can also implement a $V-I$ converter, adding a resistor at its input (Fig. 4).

B. Current-Driven Biquadratic Cell

The mixer driving stage can be transformed into a Biquad cell as shown in Fig. 5. Since the cell is now current-driven by the VGA, a $V-I$ conversion is no longer necessary and, thus, its input virtual short can be used to implement a filtering transfer function. The key idea is to synthesize an active inductor by boosting the voltage across the input resistor R_1 at high frequency. This is obtained inserting a high-pass filter (C_2R_2) between the terminals V_a and V_- , the inverting input of the Op Amp. At low frequency, all of the input current i_{in} flows through

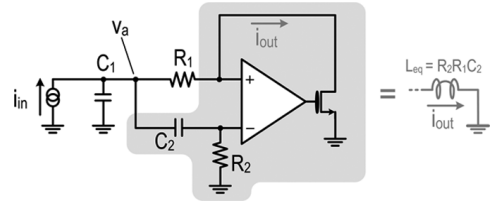


Fig. 5. Single-ended schematic of the proposed current-driven Biquad.

R_1 since C_1 and C_2 are open circuits and terminal V_+ is virtually shorted to ground. On the other hand, above the cutoff frequency $1/R_2C_2$, the two terminals of R_1 are virtually shorted, preventing any flows of current into the Op Amp output stage (represented by the MOS transistor). The active inductor and the grounded capacitor C_1 leads to the following second-order low-pass transfer function

$$H(s) = \frac{i_{out}}{i_{in}} = \frac{1/L_{eq}C_1}{s^2 + s\left(\frac{R_1}{L_{eq}}\right)\left(\frac{C_1+C_2}{C_1}\right) + \frac{1}{L_{eq}C_1}} \quad (1)$$

where L_{eq} is the synthesized inductor whose expression is given by

$$L_{eq} = R_2R_1C_2. \quad (2)$$

Inserting (2) in (1) gives the ω_0 and quality factor Q as function of the design variables R_1 , R_2 , C_1 , and C_2 , obtaining

$$\omega_0 = \frac{1}{\sqrt{C_1C_2R_1R_2}}, \quad Q = \frac{\sqrt{C_1C_2R_2}}{(C_1 + C_2)\sqrt{R_1}}. \quad (3)$$

Assuming $C_1 \gg C_2$ (valid in the proposed design), the term $((C_1 + C_2)/(C_1))$ in (1) is ≈ 1 and the expression of Q becomes the ratio of the two time constants

$$Q \approx \sqrt{\frac{C_2R_2}{C_1R_1}}, \quad (if \ C_1 \gg C_2). \quad (4)$$

Equation (4) will be used to provide an easy frequency tuning of the cutoff frequency to implement multistandard capabilities. Equations (3) and (4) show that it is possible to change ω_0 without changing the Q , therefore maintaining the same filtering shape.

Compared with other gm-C-based solutions for the same applications [8], our Biquad has the advantage [10] that its transfer

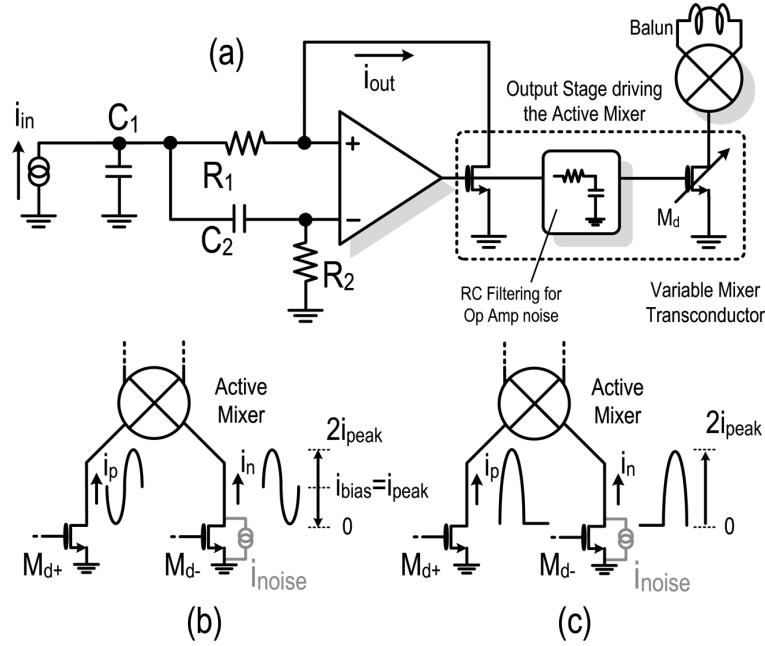


Fig. 6. (a) Proposed Biquad as a mixer driver: (b) class-A and (c) class-B behavior of the mixer transconductors.

function depends only on passive elements and, thus, it is not influenced by signal level, as it occurs in the approach reported in [8].

In terms of out-of-band noise, our solution is similar to the $V-I$ converter of Fig. 2 [7]: R_1 injects the same out-of-band noise, while R_2 sees low-pass transfer function to the output and does not contribute significantly to the overall out-of-band output noise.

C. Class-A/B Power Mixer

The conceptual scheme of the current-driven Biquad/mixer driver is given in Fig. 6(a). The role of the active mixer is to deliver power to the balun placed at his output. This operation is generally performed biasing the mixer in Class A where there is a tradeoff between the voltage and current swings necessary to deliver a given power [7]. A large voltage swing on a high-Q balun improves the efficiency, requiring a lower bias current, but leads to a worse transmitted power/noise spectral density ratio, that will be called Phase Noise (PN) of the mixer. On the other hand, large current swing reduces the overall efficiency but improves the PN.

The mixer PN improvement can be understood from the schematic in Fig. 6(b). For each transconductor M_{d+} and M_{d-} , the PN of the output current is given by

$$\text{PN}_{\text{gm}} = \frac{i_{\text{RMS}}^2}{di_{\text{noise}}^2/df} \quad (5)$$

where i_{RMS} is the root mean square (RMS) value of the current signal and di_{noise}^2/df is the transistor current noise power spectral density (PSD), which is proportional to its transconductance gm. Assuming for di_{noise}^2/df the expression $4kTgm$ (for simplicity with $\gamma = 1$), (5) can be rewritten as

$$\text{PN}_{\text{gm}} = \frac{i_{\text{RMS}}^2}{4kTgm} = \frac{V_{\text{ov}} \cdot i_{\text{peak}}^2}{8kT \cdot \text{PAPR} \cdot i_{\text{bias}}} \quad (6)$$

where PAPR is the ratio between the signal peak and the RMS values ($i_{\text{peak}}^2/i_{\text{RMS}}^2$) and gm can be expressed as $2i_{\text{bias}}/V_{\text{ov}}$, where V_{ov} is the saturated transistor overdrive. In Class A [Fig. 6(b)], the bias current must be at least equal to i_{peak} and thus (6) becomes

$$\text{PN}_{\text{gm}} = \frac{i_{\text{bias}} V_{\text{ov}}}{8kT \cdot \text{PAPR}} \quad (7)$$

From this equation, we can see that, for a given delivered power, increasing i_{bias} while maintaining a constant V_{ov} permits to improve the mixer PN by increasing the current signal swing (and correspondingly reducing the output voltage swing). However, this approach has the drawback to increase the overall power consumption, reducing the efficiency.

Starting from (5), it is possible to obtain a higher efficiency if the transistors are biased in class B [Fig. 6(c)]. In this case, each transistor has to process only half of the signal waveform and hence i_{bias} is not constrained to be larger than i_{peak} . Ideally, i_{bias} could go to zero, but then nonlinearity problems arise, so a finite i_{bias} is always used, thereby moving from class-B to class-A/B operation. Nonetheless, bias current will always be much less than in class A. This makes current noise lower and the mixer PN much higher, especially for signals with high PAPR (e.g., for 4G).

III. DETAILED IMPLEMENTATION OF THE PROTOTYPE

The fully current-mode transmitter has been implemented starting from the one presented at ISSCC in 2013 [7], reusing the original current-steering DAC and the additional voltage Tow-Thomas (TT) Biquad, allowing to still implement a fifth-order filter for some particularly critical bands. As a consequence, we had to make the VGA presented in Section II-A compatible with the old architecture. Finally, the original

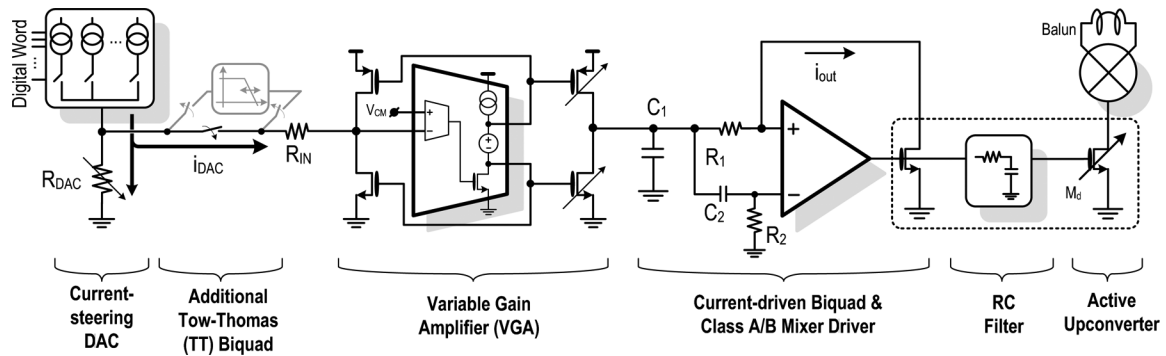


Fig. 7. Third- and fifth-order filtering configuration of the proposed transmitter, I-path only.

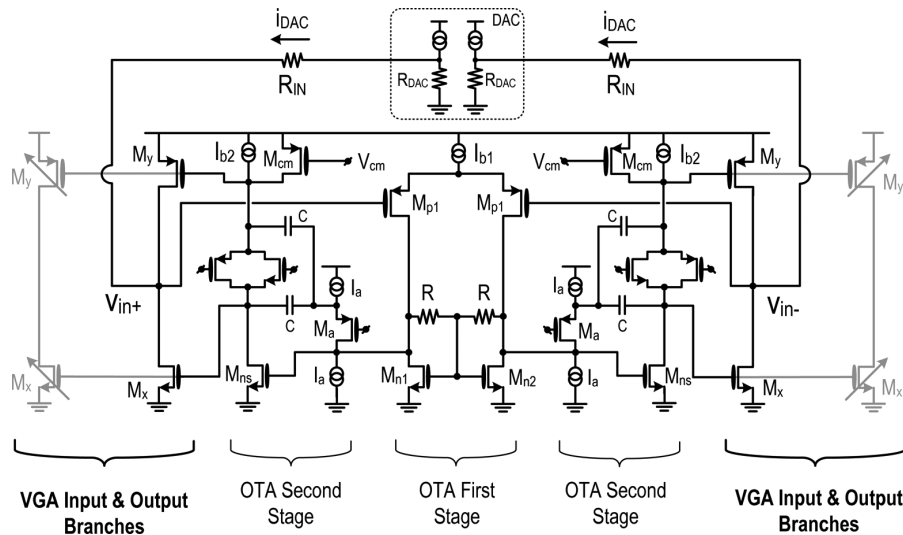


Fig. 8. Detailed schematic of the proposed VGA.

$V-I$ converter/mixer driver has been transformed into the current-driven Biquad previously described.

The detailed block diagram of the proposed current-mode transmitter is shown in Fig. 7 in its single-ended version, I-path only. Since in the original transmitter the DAC was operated in voltage mode, by delivering its current to an output resistor R_{DAC} , a resistor R_{IN} is connected to the virtual ground of the VGA. If such a resistor is $\gg R_{DAC}$, the voltage swing at to DAC output and its behavior remain practically unchanged. The only difference is for the third-order filtering configuration, where the DAC output current undergoes a partition between R_{DAC} and R_{IN} .

On the other hand, for the fifth-order filtering configuration case, the TT Biquad operates in voltage mode and the DAC works exactly as in the original design. In this case, to return to current mode, a $V-I$ conversion takes place (as mentioned in Section II-A) at the output of the TT Biquad by driving the virtual ground of the VGA through resistor R_{IN} . Let us first discuss the transmitter in the third-order configuration.

A. VGA for Third-Order Filtering Configuration

The schematic of the differential OTA inserted in the current mirror is shown in Fig. 8. The differential current i_{DAC} represents the portion of the DAC current that reaches the VGA (after

the current partition), while the two R_{IN} are the VGA input resistors shown in Fig. 7. The low impedance virtual ground is achieved embedding the VGA input branches into a feedback loop that includes a three-stage differential OTA that is loaded by the resistor $R_{IN} + R_{DAC}$.

The first stage is a differential pair loaded by a large differential resistor ($2R$) in parallel to a current source. The structure permits to set the output dc operating point without requiring a common-mode feedback while giving a large voltage gain. This is because, from the common-mode point of view, the two load transistors (M_{n1} and M_{n2}) are equivalent to two diodes, while from the differential point of view they look like current sources (their gates are at virtual ground). The second stage uses an NMOS common-source topology that also implements the Huijsing floating battery [11]. The bias current is set by the current generators I_{b2} , while the transistors M_{cm} are part of a common-mode feedback (not shown in Fig. 8 for simplicity) that forces the OTA common-mode voltage (both input and output) to $V_{dd}/2$. The floating battery outputs drive both the input and output branch of the PN current mirror, making it behave as a push-pull stage.

The uncompensated amplifier would have two low-frequency poles (at the outputs of the first and of the second stage) and one extra pole at much higher frequency (at the output of the third stage of the OTA). This is because the output stage is loaded by

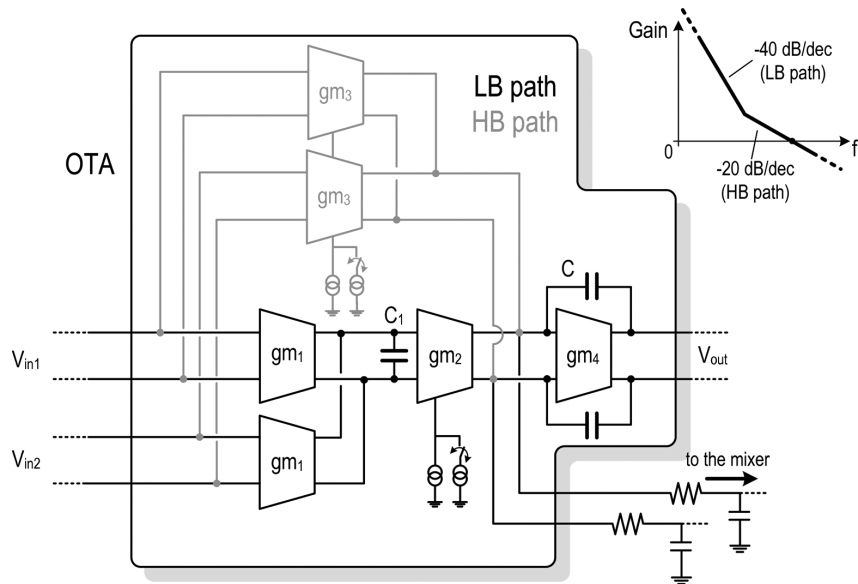


Fig. 9. Block diagram of the multipath OTA.

a relatively small resistance (the series of R_{IN} and R_{DAC}) and a small parasitic capacitance, that pushes the pole at several hundreds of megahertz. Using a simple Miller compensation, the pole associated with the second stage of the OTA could give stability issues since the parasitic capacitors of the variable current mirror can be relatively large. The problem could be solved increasing the bias current in M_{ns} to increase his gms thereby push such a pole at higher frequency. A more current-efficient solution is the Ahuja compensation [12].

The current consumption in the various branches of the OTA is decided by noise, stability and linearity. A high-input gm is necessary in the first stage to provide low noise and large bandwidth. As a consequence, I_{b1} has been chosen to be $90 \mu A$. The second stage sets the position of the nondominant poles, defining the stability margin of the overall loop. Thanks to the Ahuja compensation, a current of $160 \mu A$, divided between I_{b2} and the common-mode feedback transistor M_{cm} , is sufficient for this branch. Finally, the class-A/B quiescent current in the output stage of the OTA (mirror input branch) sets the linearity of the VGA, the current efficiency of the class-A/B current mirror and affects the overall stability. A quiescent current of $5 \mu A$ is set through the floating battery in the current mirror input branch, while at the output branch this value is amplified with a factor programmable from 1 to 32.

B. VGA for Fifth-Order Filtering Configuration

When the TT Biquad is added in front of the VGA, the virtual ground and the resistor R_{IN} will be now used as a $V-I$ converter, since the output signal of the TT Biquad can be considered as a voltage source (very low impedance).

In the previous case, R_{IN} was chosen $\gg R_{DAC}$ to not disturb the behavior of the DAC. In the present case, this is not necessary since the TT Biquad interfaces the DAC and the resistor can be scaled down (provided it can be driven by the last OTA of the TT Biquad) to increase the transconductance of the $V-I$ converter. Since the Tow-Thomas cell re-used from the previous transmitter [7] already implements a voltage gain of two

from input to output, R_{IN} has been halved with respect to the 3rd order filter configuration. As a consequence, the signal current at the input of the VGA becomes four times larger. To preserve the current range at the output of the variable mirror (input of the current-driven filtering stage/mixer driver), the size of the input transistors of the mirror needs to be increased by a factor of four while keeping unchanged the size of the output branch (that can still programmed over a 1 to 32 ratio). To accommodate the larger current signal, the quiescent current in the input branch of the current mirror is increased to $20 \mu A$, which also increases its transconductance. To maintain approximately constant the gain-bandwidth product of the feedback loop around the VGA, the current I_{b1} (see Fig. 8) of the OTA differential pair can be programmed from $90 \mu A$ to $70 \mu A$.

C. Current-Driven Biquad's Multipath OTA: Main Structure

The single-ended current-driven Biquad presented in the previous section (Fig. 5) uses both input terminals of the OTA. As a consequence, in a differential implementation there is the need for a four-inputs/two-outputs OTA. Furthermore, to achieve a sufficiently high gain across the band of interest (for linearity reason), a single-pole OTA would have an excessive unity gain bandwidth, creating stability issues. A more effective solution is to use a multipath OTA to implement a $-40/-20$ dB per decade slope in the OTA transfer function [13].

The used structure, depicted in Fig. 9, is based on the sum of two different paths, a low-bandwidth/high-gain path (LB) path and a high-bandwidth/low-gain path (HB). At low frequency, the LB path dominates while the HB path dominates at high frequency. Two in-band poles in the LB path create an initial slope of -40 dB/dec in its transfer function (instead of the classical -20 dB/dec). As a consequence, the gain of the LB path falls much more rapidly than that of the HB path. When the LB path gain becomes lower than that of the HB path, the latter becomes the dominant path and the global transfer function shows a zero that increases its phase. The relative value of the unity gain bandwidth of the two parallel paths is chosen in such a way that

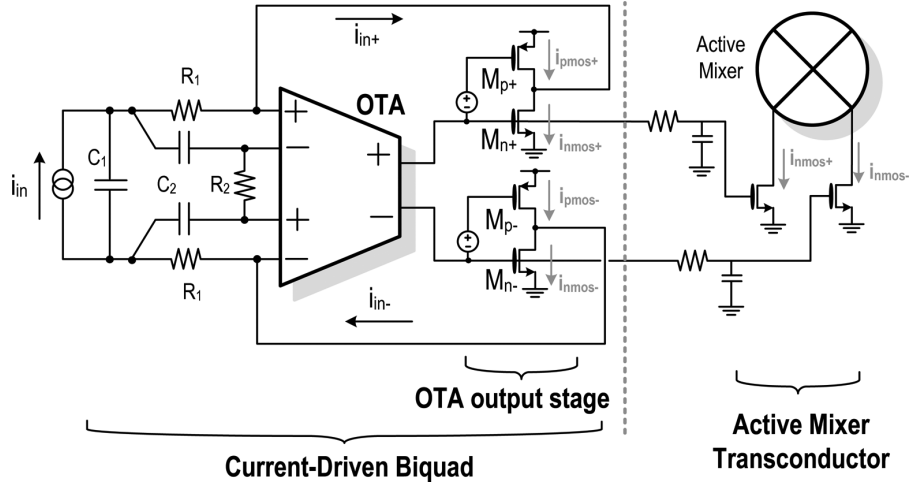


Fig. 10. Current-driven Biquad OTA output stage in class-A/B driving the active mixer.

the 0 dB axes is crossed with a slope of -20 dB/dec and phase and amplitude margins exceeds 60 degrees and 10 dB respectively, insuring a very stable behavior [14]. At the same time, the unity gain bandwidth is much smaller than the gain-bandwidth product computed at the frequency of interests, allowing excellent linearity and simultaneously robustness against parasitic poles, temperatures, and process variations.

As said, the fully differential OTA needs to have a four input/two output structure. This is achieved duplicating the input stage of both the main and feed-forward path and combining them before reaching the output as shown in Fig. 9. Furthermore, the current consumption of the second and feed-forward stages can be increased under digital control: this is required because the OTA must drive the programmable RC filter inside the output current mirror. For large bandwidth signals (e.g., LTE20), the risk of slew rate on the capacitor can arise, so the current biasing is increased. The gm blocks of Fig. 9 are realized as differential pairs with active loads.

D. Current-Driven Biquad's Multipath OTA: Class-A/B Output Stage

The output stage of the OTA, depicted as a single NMOS in Figs. 5–7, will drive the mixer in class A/B, as discussed in Section II-C. A traditional approach to create a class-A/B output stage is shown in Fig. 10, where the schematic of the differential current-driven Biquad and the mixer transconductors are reported. The circuit is basically an inverter with a floating battery between the PMOS and NMOS gates that sets its quiescent current. The voltage signal at the NMOS gate is hence DC-shifted to the PMOS transistor, making the stage work in a push-pull fashion.

In this configuration, the input current signal i_{in+} ($= i_{in-}$) is divided between the output transistors M_{p+} , M_{n+} (and M_{p-} , M_{n-}). Unfortunately, the differential current at the mirror output (assuming a mirror factor equal to one) becomes

$$i_{mixer} = i_{nmos+} - i_{nmos-} \quad (8)$$

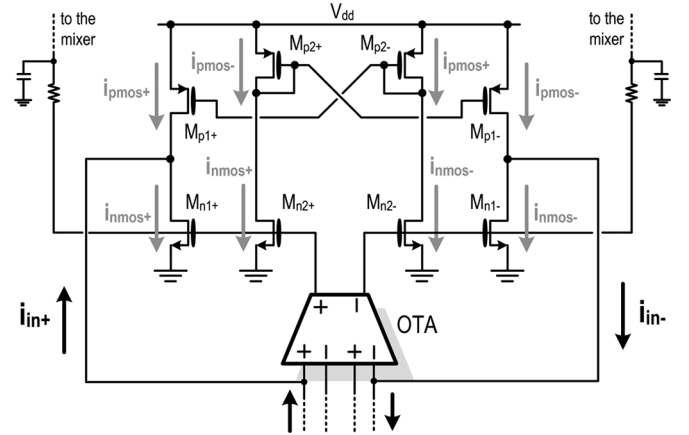


Fig. 11. Proposed class-A/B output stage of the current-driven Biquad OTA.

which is not equal to the input current $i_{in+} = i_{nmos+} - i_{pmos+}$, leading to signal distortion. For a correct operation, the complete signal information should be provided by the NMOS transistors, since the transconductors that drive the active mixer uses NMOS-only devices.

The circuit configuration that correctly drives the mixer using only NMOS transistors [7] is shown in Fig. 11, where the gates of M_{n1+} and M_{n1-} are connected to the gate of the mixer transconductors. In this case, for the positive side of the circuit, although the current signal i_{in+} is divided between M_{p1+} and M_{n1+} as before, the cross-connected current mirror forces i_{pmos+} to be equal to the current i_{nmos-} flowing in M_{n1-} . Since the same behavior is valid for the negative side of the circuit, the differential output current (that will be mirrored toward the mixer) $i_{nmos+} - i_{nmos-}$ becomes

$$(i_{nmos+} - i_{nmos-}) = (i_{nmos+} - i_{pmos+}) = i_{in+} \quad (9)$$

i.e., the differential signal current flowing into the mixer is equal to the input signal current of the Biquad.

Finally, two type of common-mode feedbacks (CMFBs) are necessary [7], one to control the quiescent bias current of the output PN stage and one to control the output CM voltage of

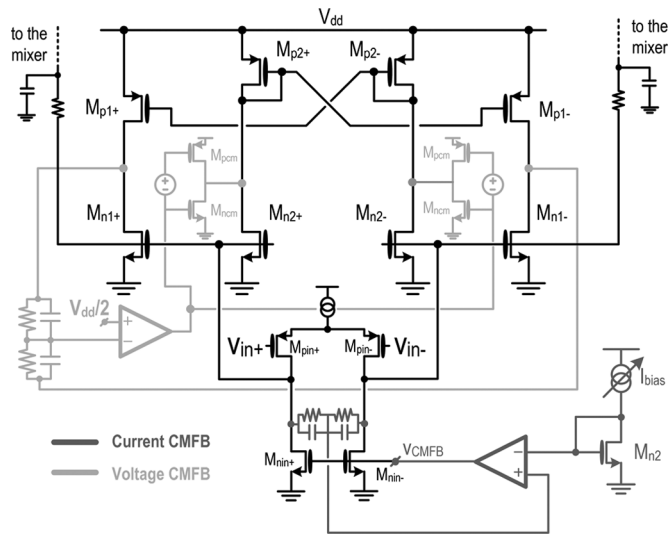


Fig. 12. Common-mode loops to control the output voltage and the bias current of the proposed class-A/B stage.

the same stage, setting it to $V_{dd}/2$: the detailed schematic is reported in Fig. 12, where the PMOS differential pair together with the NMOS active load that drives it represent the transconductors gm_2 and gm_3 . The current CMFB senses the input common-mode voltage of the class-A/B stage and acts on the driving stage to force reference current I_{bias} to flow in the output branches in quiescent conditions, whereas the voltage CMFB senses the output common-mode voltage and injects (draws) a current into (from) the central branches to set its value to $V_{dd}/2$.

The power consumption of the OTA and the relative bias current level used in its various stages depends on many considerations including the required bandwidth, the target noise density at a given frequency, and the load to be driven. In an FDD transceiver, TX-path noise is generally more critical out-of-band than in-band to satisfy spurious emission specifications. The critical frequency range corresponds to the offset between the TX and the RX band which, for the different standards and working bands, goes from some megahertz to several hundreds of megahertz. When using a multipath architecture, the input noise density at low frequency (up to several times the dominant pole location) is totally dominated by the main input stage. On the other hand, when approaching the amplifier unity gain frequency, the contribution of the other stages (including those of the secondary path) starts to appear and possibly become dominant depending on their relative bias current level.

The bandwidth of this OTA ranges from 140 to 110 MHz (depending on the bandwidth of the passive elements it needs to drive), so the noise of all stages (and especially the last ones) can become critical. This is why a significant portion of the total bias current is given to the second and the feed-forward stages in addition to the fact that they decide the size of the capacitor that the OTA can drive and its stability, respectively. The first stage ($2 \cdot gm_1$, see Fig. 9) draws $120 \mu A$, while the second and the feed-forward stages (gm_2 and $2 \cdot gm_3$), draw 400 and $600 \mu A$, respectively, which become 1 and 1 mA when processing large bandwidth signal. The output class-A/B stage (gm_4) has a quiescent bias current which can be controlled acting on the CMFB

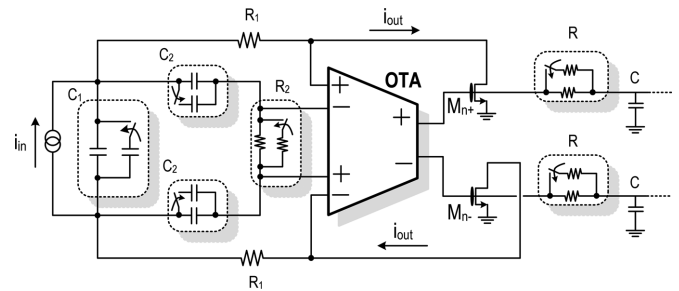


Fig. 13. Passives reconfiguration of the current-driven Biquad.

reference. This programmability strongly affects power consumption since it affects the scaled-up class-A/B up-converter, i.e., the most power-hungry stage of the transmitter. Changing the quiescent current of the stage (from 100 up to $275 \mu A$ for each one of the four branches of Fig. 11) permits to trade off nonlinearity/noise and power consumption.

E. Filtering Reconfigurability

The passive elements of the proposed current-driven Biquad and those of the RC passive filter have been made reconfigurable to adapt to the various standard supported (i.e., from $3G$ to LTE for both TDD and FDD standards) and to compensate for temperature/process variations.

Using (3), the ω_0 of the current-driven Biquad can be programmed while keeping the same Q (and, in particular, a $Q = 1$ to implement a Butterworth transfer function) by changing either the R or the C and temperature/process compensation was achieved acting on the C . The following associations between the current-driven Biquad and the passive filter ω_0 have been made.

- For $LTE20$ and $LTE15$, the Biquad's and RC 's ω_0 is 18 MHz.
- For $LTE10$, the Biquad's and RC 's ω_0 is 9 MHz.
- For narrower bandwidths, the Biquad ω_0 is set at 6.3 MHz and the RC ω_0 at 4.5 MHz.

While the change of ω_0 from 18 to 9 MHz was possible by doubling both the capacitors of the current-driven Biquad and the R of the real pole, for the narrower bandwidth case, it was possible to double R_2 but not R_1 , thereby decreasing ω_0 by only about 30% . This is because the last configuration corresponds to standard with 6 and 9 dB of PAPR, so the voltage swing on R_1 , that is maximized for 6 dB PAPR standards, would have saturated the VGA output for standards with 9 dB PAPR for a constant RMS power to be delivered. On the other hand, this problem did not arise for the passive filter, given its limited voltage swing, so in this case the R was actually doubled.

The resulting transfer function for this last case is no longer a Butterworth one: however, simulations and measurements proved that this creates no problems in terms of error vector magnitude (EVM) [15]. A similar situation occurs when the additional TT Biquad is activated to implement the fifth-order configuration. The reconfigurable current-driven Biquad schematic is shown in Fig. 13. Most of C_1 has been grounded as opposed to connecting it differentially (which would have saved a factor of four in area) because, with a class-A/B VGA and mixer transconductors, part of the noise coming from

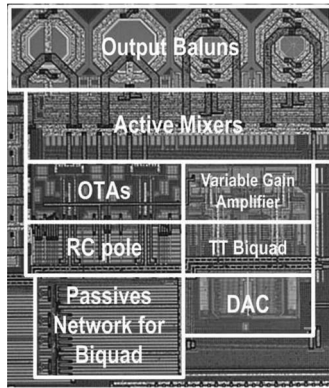


Fig. 14. Transmitter chip microphotograph.

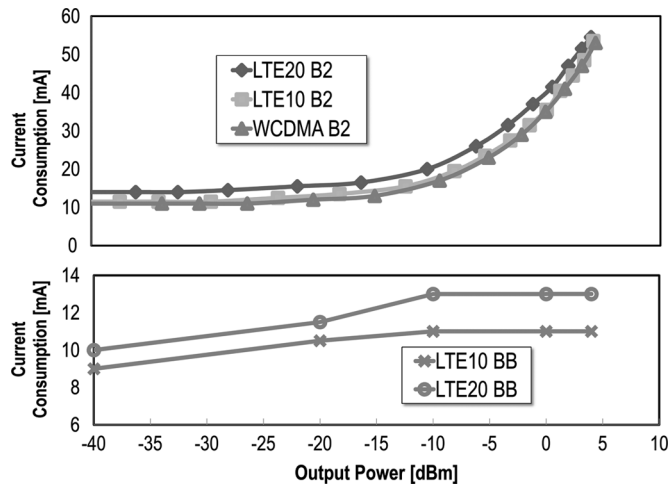


Fig. 15. Transmitter current consumption and baseband current consumption from 1.8 V versus the output power transmitted.

common-mode portions leaks into the differential path. This can degrade performances since the power consumption of the common-mode circuits is much less than that of the differential ones making their noise higher.

The values of the single-ended passives in the current-driven Biquad for the highest cutoff frequency case are given below: $R_1 = 175 \Omega$, $R_2 = 3.6 k\Omega$, $C_1 = 50 pF$, and $C_2 = 2.5 pF$, while for the passive RC filter $C = 18 pF$, $R = 500 \Omega$.

IV. MEASUREMENTS

The transmitter has been implemented as a part of a fully reconfigurable transceiver, manufactured in 55 nm CMOS technology. In Fig. 14, the microphotograph of the transmitter is reported. The whole analog section (BB plus up-converter) uses a single 1.8 V supply and occupies an active area of $1.5 mm^2$, almost equally divided between the RF and the BB sections. About half of the BB area is occupied by the capacitors of the filters.

The current consumption of the complete transmitter and that of the sole baseband (DAC and TT Biquad excluded) when transmitting in Band2 for LTE20, LTE10, and 3G are reported in Fig. 15. The LTE10 measured output spectrum is reported in Fig. 16.

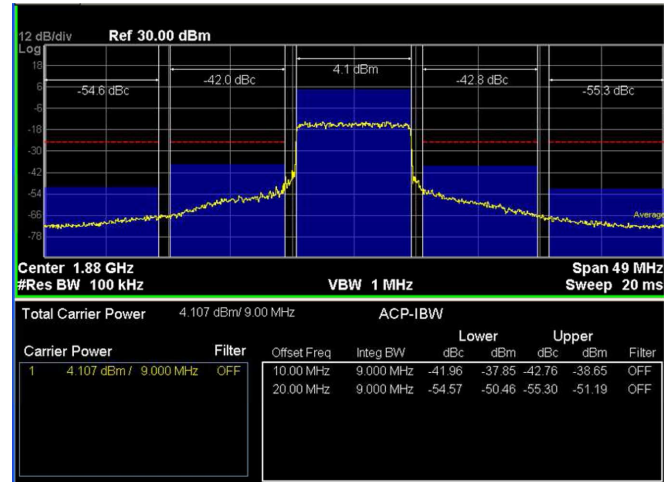


Fig. 16. Measured output spectrum for LTE10, Band2.

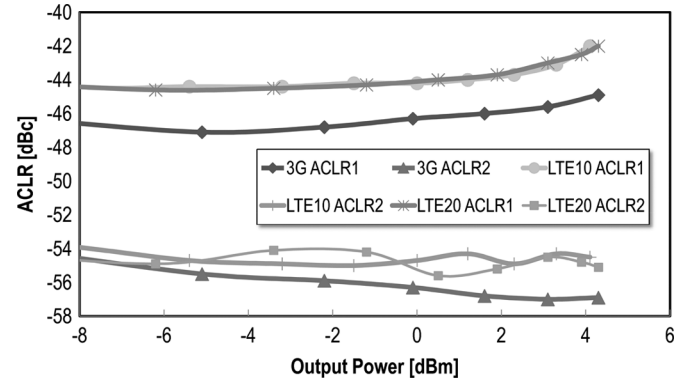


Fig. 17. Transmitter linearity parameters versus transmitted power.

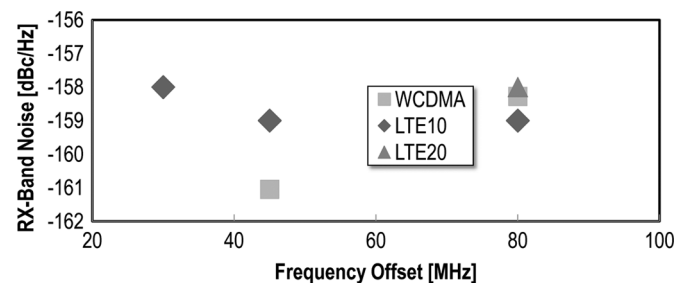


Fig. 18. Out-of-band noise performances versus TX-RX frequency offset.

The advantages associated with the use of a class-A/B up-converter can be appreciated noticing that, while delivering the same RMS power, the current consumption is almost the same for the various standards even if they have significantly different PAPR. This is not the case for a transmitter that uses a class-A up-converter as the one reported in [6]. When the output power is lowered below $-10 dBm$ (reducing the output mirror input-to-output current ratio), the most power-hungry section becomes the BB, while the up-converter absorbs only a small fraction of the total current (less than 20 mA). The small dc current difference between 3G/LTE10 and LTE20 is due to a larger OTA current in the output transistor for the latter case. This is due to the need to drive a smaller resistance when

TABLE I
COMPARISON WITH A VOLTAGE-MODE TRANSMITTER FROM [2]

Parameter	Unit	[2]			This Work		
		LTE10	LTE10	LTE20	LTE10	LTE10	LTE20
Band	-	5	12	2	5	17	2
Output Power (OP)	dBm	2.45	0.4	2.6	2.8	0.2	3.1
$ACLR_{E-UTRA1}$ @OP	dBc	-41.4	-41	-38.4	-43.4	-44	-43
$ACLR_{UTRA2}$ @OP	dBc	-63	-67	-59	-54.9	-57.4	-54.5
EVM @OP	%	1.7	1.9	2.4	1.4	1.4	1.4
Consumption @OP	mW	111.2	101.2	126.4	97	90	93
RX-band noise @OP)	dBc/Hz	-160.5 ^a	-159 ^a	-162.5 ^a	-159 ^b	-158 ^b	-158 ^c
		@45MHz	@30MHz	@80MHz	@45MHz	@30MHz	@80MHz
Supply Voltage	V	1.1/2.5			1.8		
Area	mm ²	0.98			1.06 ^d		
Technology	nm	40			55 LP		

(a) Carrier-to-Noise ratio; (b) measured with 20 RB; (c) measured with 50 RB;
(d) without DAC, TT Biquad and 2 baluns

TABLE II
COMPARISON WITH A CURRENT-MODE TRANSMITTERS FROM [6] AND [7]

Parameter	Unit	[6]	[7]	This Work	[6]	[7]	This Work
			LTE10			LTE20	
Max Output Power	dBm	3.7	6	6	4	6	6
Output Power (OP)	dBm	3.7	4	4	4	4	4
$ACLR_{EUTRA1}$ @OP	dBc	-40.3	-44	-42	-40.3	-40.9	-42.5
$ACLR_{EUTRA2}$ @OP	dBc	NA	-55	-54.5	NA	-55	-54.8
Consumption @OP	mW	186	101	96	199	101	98
Consumption @-10dBm	mW	56	39.5 ^a	34	70	39.5 ^a	36
EVM HB (LB) @0dBm	%	0.66 (NA)	1.8 (1.4)	1.8 (1.4)	1.05 (NA)	1.4 (1)	1.4 (1)
RX Noise@0dBm	dBc/Hz	-155	-154	-158	-157	-155	-158
		@30MHz	@30MHz	@30MHz	@120MHz	@80MHz	@80MHz
Supply Voltage	V	1.55/2.7	1.8	1.8	1.55/2.7	1.8	1.8
Area	mm ²	5.06	1.3	1.5	5.06	1.3	1.5
Technology	nm	90	55 LP	55 LP	90	55 LP	55 LP

(a) ISSCC13 Visual Supplements [7]

the pole of the last RC passive filter is tuned to high frequency (see Fig. 9).

The possibility of controlling the TX output power also by programming the current ratio in the VGA mirror allows to decrease also the BB current consumption at very low output power (Fig. 15). The total current consumption decreases at a very small rate when the output power is reduced below -15 dBm. This is because the fractional mirror factor of the up-converter was not used during the measurements, instead the output power was scaled down using the programmable attenuators at the balun level (which is nominally activated below -40 dBm). As a consequence, the current consumption of the up-converter is not minimized. Such a choice was made to reduce the LO leakage to an acceptable level without activating the calibration loop.

In Fig. 17, the adjacent channel leakage ratio (ACLR) versus output power for LTE20, LTE10, and 3G are reported in Band2 for the portion of the RF signal located on the left-hand side of the carrier, which shows a worse behavior than the one on the right-hand side. $ACLR_{E-UTRA1}$ and $ACLR_1$ stay below -42 and -45 dBc (for 4G and 3G) up to 4 dBm. At low power, linearity is limited by the BB (dominated by the last current mirror because of the presence of the passive filter), while at higher power by signal compression in the up-converter.

RX-band noise measurements for the bands with the most critical TX-RX offsets are reported in Fig. 18, at 0 dBm output power. The measurements for 4G standard have been made with transmitted signals composed of partial resource block (RB), as specified by 3 GPP, while in the 3G case the full signal was used. The TX output was fed to the antenna port of a duplexer tuned to the target band and measurements were done on the RX port (with the TX port terminated on 50Ω), de-embedding the duplexer and cable attenuations. In this way, the transmitted signal was sufficiently suppressed by the stop-band of the duplexer to make it possible to measure the RX-band noise without saturating the spectrum analyzer. The worst case is the LTE10 Band17 which has a TX-RX frequency offset of 30 MHz, where the transmitter shows a noise equal to -158 dBc/Hz.

Finally, a comparison with the state of the art is provided. In Table I, the comparison is done with a transmitter that uses a voltage-mode approach [1]–[3] while in Table II the comparison is done with two current-mode transmitter [6], [7]. Notice that the DAC is excluded from all comparisons.

Table I compares for similar output powers and TX-RX offsets. Our transmitter shows better $ACLR_{E-UTRA1}$ and less power consumption and, featuring only one 1.8 V supply as opposed to two (at 1.1 V and 2.5 V), is less costly. RX-band noise is generally a bit larger for our implementation. However, in [2],

the noise testing condition used (1 MHz BB tone [3]) is not 3 GPP compliant and can give significantly better results. Chip area (considering the same building blocks) is less than 10% larger in our implementation, but using an older technology.

Comparing with two recent current-mode transmitters (Table II), the following conclusion can be drawn. With respect to the first TX [6] that uses a class-A up-converter, our work shows similar performance but requires about one quarter of silicon area and significantly less current consumption, especially in the range of output power from 4 dBm and -10 dBm. This is because we use a class-A/B approach in the up-converter that dominates the consumption above -10 dBm. Finally, the use of a single supply as opposed to two makes our solution cheaper. Compared with the transmitter described in [7], on which our implementation is based, the new solution shows an improvement of 4 dB in LTE10 and 3 dB in LTE20 in the RX-band noise and requires, respectively, about 3 and 2 mA less current thanks to the new BB architecture. In LTE10, the power saving, although very small at 4 dBm, is already about 16% at -10 dBm and exceeds 25% at very low output power. On the other hand, the area is increased by about 15% primarily due to the size of the capacitors (single-ended) used in the passive filters.

V. CONCLUSION

This paper describes a complete SAW-less multistandard transmitter in 55 nm for 3G/4G applications. The proposed architecture operates entirely in current mode from the DAC to the up-converter and is based on a reconfigurable active filtering block merged with the active mixer driver. This permits to attenuate out-of-band emissions just before the up-converter, as in state-of-the-art transmitters using passive voltage mixers. Furthermore, the use of a class-A/B approach along the entire chain, and especially in the up-converter, further reduces the out-of-band emission and the power consumption. The realized prototype occupies 1.5 mm^2 and, compared with passive and with active mixer based transmitters, shows high power efficiency (less than 100 mW at 4 dBm of output power) and low out-of-band emissions for small TX-RX frequency offsets ($\leq -158 \text{ dBc/Hz}$).

ACKNOWLEDGMENT

The authors would like to thank Marvell for technology access and the members of Marvell Italy and Aliso Viejo (USA) Mobile Transceiver groups, in particular, F. Rezzi, D. Gerna, D. Ottini, E. Sacchi, A. Loke, S. Tadjpour, R. Chokkalingam, H. Amir Firouzkouhi, Y. He, and C. Çakir.

REFERENCES

- [1] H. Xin and J. van Sinderen, "A low-power, low-EVM, SAW-Less WCDMA transmitter using direct quadrature voltage modulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3448–3458, Dec. 2009.
- [2] V. Giannini *et al.*, "A multiband LTE SAW-less modulator with -160 dBc/Hz RX-band noise in 40 nm LP CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 20–24, 2011, pp. 374–376.

- [3] J. Craninckx, J. Borremans, and M. Ingels, "SAW-less software-defined radio transceivers in 40 nm CMOS," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 19–21, 2011, pp. 1–8.
- [4] E. Sacchi, I. Bietti, S. Erba, L. Tee, P. Vilmercati, and R. Castello, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 21–24, 2000, pp. 459–462, vol., no..
- [5] S. Kousai and A. Hajimiri, "An octave-range, watt-level, fully-integrated CMOS switching power mixer array for linearization and back-off-efficiency improvement," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3376–3392, Dec. 2009.
- [6] O. Oliaei *et al.*, "A multiband multimode transmitter without driver amplifier," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 19–23, 2012, pp. 164–166.
- [7] P. Rossi *et al.*, "An LTE transmitter using a class-A/B power mixer," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 340–342, vol., no..
- [8] M. Cassia *et al.*, "A low-power CMOS SAW-less quad band WCDMA/HSPA/HSPA+/1X/EGPRS transmitter," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1897–1906, Jul. 2009.
- [9] J. C. Rudell *et al.*, "A 1.1 V 5-to-6 GHz reduced-component direct-conversion transmit signal path in 45 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 8–12, 2009, pp. 418–419, 419a.
- [10] N. Codega, A. Liscidini, and R. Castello, "A low out-of-band noise LTE transmitter with current-mode approach," in *Proc. ESSCIRC*, Sep. 16–20, 2013, pp. 283–286.
- [11] R. Hogervorst *et al.*, "A compact power-efficient 3 V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries," *IEEE J. Solid-State Circuits*, vol. 29, no. 12, pp. 1505–1513, Dec. 1994.
- [12] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-18, no. 6, pp. 629–633, Dec. 1983.
- [13] J. Huijsing, *Operational Amplifiers: Theory and Design*, 2nd ed. Berlin, Germany: Springer-Verlag, 2011.
- [14] J. D'Azzo and C. Houpis, *Linear Control System Analysis and Design: Conventional and Modern*, 4th ed. New York, NY, USA: McGraw-Hill, 1995.
- [15] Q. Gu, *RF System Design of Transceivers for Wireless Communications*, 1st ed. Berlin, Germany: Springer, 2006.



Nicola Codega (S'08–M'10) was born in Sondrio, Italy, in 1986. He received the M.Sc. degree (*summa cum laude*) and Ph.D. degree in electronic engineering from University of Pavia, Pavia, Italy, in 2010 and 2013, respectively.

He was a Ph.D. Intern with Marvell Italy from 2010 to 2013 and Marvell, Aliso Viejo, CA, USA, in 2012, working on multistandard reconfigurable transceivers for mobile communications. In 2013, he joined Marvell Technology Group, Pavia, Italy, as Analog Design Engineer, where he is currently

working on transceivers for high-speed serial communications.



Paolo Rossi (M'05) received the Laurea degree and Ph.D. degree in electrical engineering and computer science from the University of Pavia, Pavia, Italy, in 2000 and 2004, respectively.

During his studies, he worked on analog and RF integrated circuits for wireless communications, in CMOS and BiCMOS technologies, with particular focus on RF front-ends for multistandard applications. From 2005 to 2006, he was a Member of Technical Staff with Maxim Integrated Products, Milan, Italy, where he designed linear and switching regulators. In 2006 he joined Marvell Technology Group, Pavia, Italy, where he worked on low-power wireless radios. He is currently a Staff Engineer/Manager, developing RFICs for cellular applications. His research interests include the design of RF, analog, and mixed-signal circuits.



Alberto Pirola (M'10) was born in Pavia, Italy, in 1983. He received the M.Sc. degree (*summa cum laude*) in microelectronic engineering and Ph.D. degree from University of Pavia, Pavia, in 2007 and 2010, respectively.

He currently works with Marvell, Italy, Pavia, Italy, as a Senior Analog Design Engineer, where he is working on multistandard RF transceivers.



Antonio Liscidini (S'99–M'06–SM'13) was born in Tirano, Italy, in 1977. He received the Laurea degree (*summa cum laude*) and Ph.D. degree in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was a Summer Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS LNAs. From 2008 to 2012, he was an Assistant Professor with the University of Pavia, Pavia, Italy, and a Consultant for Marvell Semiconductors in the area of integrated circuit design. Since December 2012, he has been an Assistant Professor with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. His research interests are in the implementations of transceivers and frequency synthesizers for cellular and ultra low power applications.

Dr. Liscidini was the recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits and the Best Invited Paper Award at the 2011 IEEE Custom Integrated Circuit Conference. From 2008 to 2011, he served as an associate editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II—EXPRESS BRIEFS, and he served as a guest editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS for the special issue on ESSCIRC conference July

2013. Currently he is member of the TPC of the European Solid State Circuit Conference (ESSCIRC) and of the International Solid State Circuit Conference (ISSCC).



Rinaldo Castello (S'78–M'78–SM'92–F'99) received the B.S. degree (*summa cum laude*) from the University of Genova, Genova, Italy, in 1977, and the M.S. and Ph.D. degrees from the University of California, Berkeley, CA, USA, in 1981 and 1984, respectively.

From 1983 to 1985, he was Visiting Assistant Professor with the University of California, Berkeley, CA, USA. In 1987, he joined the University of Pavia, Pavia, Italy, where he is now a Full Professor.

He consulted for ST-Microelectronics, Milan, Italy, until 2005. In 1998, he started a joint research center between the University of Pavia and ST and was its Scientific Director up to 2005. He promoted the establishing of several design centers from multinational IC companies in the Pavia area, among them Marvell, for which he has been a Consultant since 2005.

Dr. Castello has been a member of the TPC of the European Solid State Circuit Conference (ESSCIRC) since 1987 and of the International Solid State Circuit Conference (ISSCC) from 1992 to 2004. He was Technical Chairman of ESSCIRC '91 and General Chairman of ESSCIRC '02, an associate editor for Europe of the IEEE JOURNAL OF SOLID-STATE CIRCUITS from 1994 to 1996 and guest editor of the July 1992 special issue. From 2000 to 2007, he was a Distinguished Lecturer of the IEEE Solid-State Circuits Society. He was named one of the outstanding contributors for both the first 50 and 60 years of ISSCC and was a corecipient of the Best Student Paper Award at the 2005 Symposium on VLSI of the Best Invited Paper Award at the 2011 CICC and of the Best Evening Panel Award at ISSCC 2012. He was one of the two European representatives at the Plenary Distinguished Panel of ISSCC 2013.