13.6 A 600µW Bluetooth Low-Energy Front-End Receiver in 0.13µm CMOS Technology

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One of the main goals for the next generation of radios for wireless sensor and body-area networks (WSN and WBAN) is a sub-mW receiver (RX) compliant with energy-harvested supplies. In this direction, the Bluetooth standard has introduced a low-energy operative mode (BLE) with wider channel spacing (2MHz) and relaxed blocker tolerance. The minimum sensitivity required is -70dBm but even with a sensitivity 10dB lower the BLE receiver can have a noise figure close to 19dB [1]. Although linearity and noise specs have been significantly relaxed, the design of a sub-mW solution remains challenging since the power dissipation cannot be simply scaled with the spurious-free-dynamic-range (SFDR). In fact, the ultimate bound is set by the power burned in the voltage-controlled oscillator (VCO), which is used for the generation of the local oscillator (LO) necessary for the signal downconversion. Since, for a targeted phase noise, the current required by the VCO is inversely proportional to the quality factor of the resonator adopted, a straightforward approach is to use a high-Q tank like the FBAR used by Wang et al. [2]. However in low-cost CMOS processes, when high-Q resonators are not present, an alternative strategy is to share the VCO bias current with the other blocks of the RF front-end as in the LMV cell proposed by Tedeschi et al. [3].

This paper presents a sub-mW BLE receiver based on the LMV cell reported in [3]. In the proposed solution a complementary P-N LMV cell has been introduced to reduce the current necessary to sustain the oscillation by half (Fig. 13.6.1). Furthermore, in order to operate under a 0.8V supply (even in presence of a P-N structure), a novel low-voltage quadrature low-noise amplifier (QLNA) was adopted. The integrated receiver includes also a transimpedance amplifier (TIA) and a current-recycling gm-C baseband complex filter. The TIA is biased with a fraction of the bias current of the QLNA and compensates for the conversion losses present in the classical LMV cell topologies, overcoming a fundamental limitation for this kind of downconverter.

The low-voltage-drop QLNA adopted is shown in Fig. 13.6.2. The quadrature is generated by an RC network that works as a lowpass filter for the Vgs of M0I and as a highpass filter for the Vgs of M0Q. By choosing C0 much larger than gate-source capacitances of M0I/M0Q, a wideband quadrature relationship is obtained between the two output currents (equal in magnitude around the filter cut-off frequency 1/RC). Since the BLE standard bandwidth is only 83.5MHz around 2.44175GHz, amplitude matching and good image rejection can be obtained over the entire bandwidth without re-centering the 1/RC cut-off frequency for each channel. The I/Q quadrature relationship is also independent of the matching network preceding the LNA, guaranteeing robustness with respect to external component variations. The QLNA requires only one voltage overdrive and can easily be stacked under the P-N LMV cell allowing a 0.8V voltage supply.

In classical LMV cell topologies, common-mode parasitic capacitances at the IF output of the cell lead to a loss in conversion gain [3]. The losses were mitigated by adopting the TIA shown in Fig. 13.6.3 where a resistor (Rx) was added in series with the gate of CG transistors. For common-mode signals the resistor Rx (combined with transistors M1) creates an active inductor that resonates at the LO frequency with the common-mode capacitance at the output of the LMV cell. The resistor does not affect the differential input impedance that remains equal to 2/(gm+sCgs). This stage is similar to the one proposed by Greenberg et al. to build a current-mode biquad [4]. The TIA not only minimizes conversion-gain losses, but also shares completely its bias current with the LNA.

Channel selection and image rejection are performed by the Gm-C filter, shown in Fig. 13.6.4. This filter is derived from the solution proposed by Lin et al., where the bias current is recycled among the transistors forming the Gm-C cell [5]. Unfortunately in the original scheme, transistors MIM-MRE (see Fig. 13.6.4) formed a positive feedback loop for common-mode signals that could cause the filter to latch if $gm_{IM}>gm_{RE}$. Under this restriction the imaginary part of the pole could not be larger than the real one resulting in a filter center frequency smaller than the filter passband. This constraint has been removed by adding the highlighted cross-coupled transistors MNEG. This pair produces different gains for common-mode and differential signals, damping the former with a positive resistance and boosting the latter with a negative one. The differential negative resistance in parallel to the diode-connected transistor MRE sets the filter passband while the gain of the common-mode feedback loop is kept lower than unity (damped by the positive resistance) preventing the latching. The result is the flexibility in the choice of the pole location without compromising the stability of the system. To be compliant with the BLE standard, a 2nd-order filter centered at 2MHz with a bandwidth of 1MHz was realized.

The chip was fabricated in 0.13µm IBM CMOS technology (with regular voltage threshold) to limit the cost of the wireless node. A summary of the most important measurements is reported in Fig. 13.6.5. The $|S_{11}|$ measurement shows good matching over the entire Bluetooth Low Energy spectrum (<-15dB). Figure 13.6.5 also reports the transfer function of the entire chain, measured by sweeping the RF input across the LO frequency. The asymmetry between positive and negative frequency offsets with respect to the LO frequency is due to the presence of the complex filter that amplifies the wanted signal and rejects the image. The reported transfer function corresponds to the first channel of BLE. This channel is representative of the worst-case measure in terms of gain and image rejection. In this configuration the RX provides a gain of 55.5dB with minimum 30.5dB rejection of the image. Figure 13.6.5 includes also the gain, image rejection, noise figure and IIP3 measurements for all the BLE channels. The gain varies less than 1dB across the channels while the image rejection is between 30.5dB and 37.3dB, achieved without any calibration. The minimum of 30.5dB is well above the required 21dB demanded by the BLE standard. The noise figure varies between 15.1dB and 15.8dB which results in a minimum receiver sensitivity of -84.2dBm. The IIP3 was measured through a two-tone intermodulation test, while placing blockers in the adjacent channels at 5MHz and 8MHz. At maximum gain the receiver has an IIP3 higher than -17dBm.

A summary of the receiver performance is reported in Fig. 13.6.6 along with a comparison to the state of the art for BLE and ZigBee receivers. The proposed design has the lowest power consumption among the BLE receivers in the table and consumes well below 1mW of power. Compared to the solutions present in the literature with similar performances ([1] and [2]), the proposed design consumes only a fraction of the power. The other designs reported in the table have better noise figures but also report much higher power consumption. Although in this case a fair comparison is difficult to make, it can be verified that the power consumption required to generate the local oscillator in [3], [5], and [6] is either higher or comparable to the power consumption of the entire receiver front-end proposed in this paper. Therefore, even if the performances of the other RX chains were significantly compromised in favor of a lower consumption (by scaling the power consumption of LNA, mixers, and base-band section), it would be difficult to achieve an overall power consumption below the one reported here since the power necessary for LO generation cannot be arbitrary scaled. A CMOS die micrograph is shown in Fig. 13.6.7. The design occupies an active area of only 0.25mm^2. Despite using a 0.13µm technology node, the proposed design has demonstrated the lowest power consumption, occupies one of the smallest areas, and is fully compliant with BLE requirements.

References:

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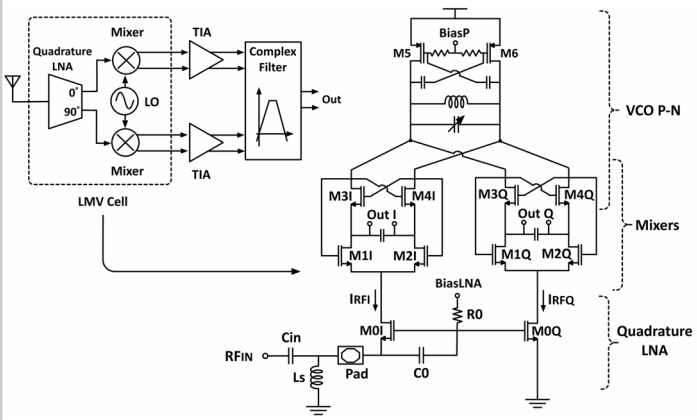

Figure 13.6.1: Block diagram of the integrated BLE receiver and P-N LMV cell (bias not shown).

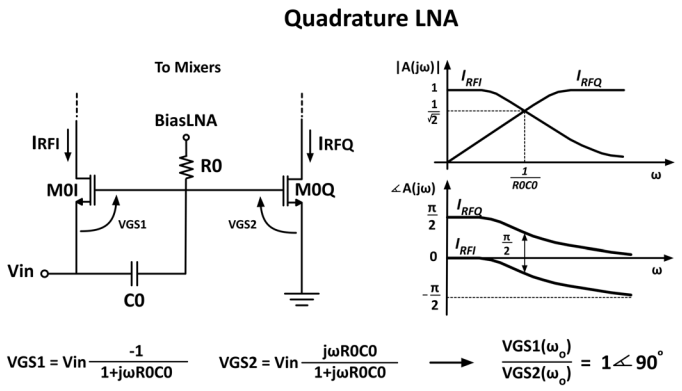

Figure 13.6.2: Quadrature Low-Noise Amplifier working principle (bias not shown).

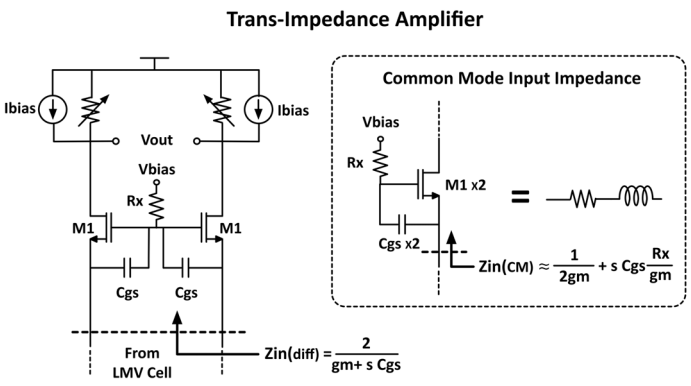

Figure 13.6.3: Common-gate TIA with common-mode inductive input impedance.

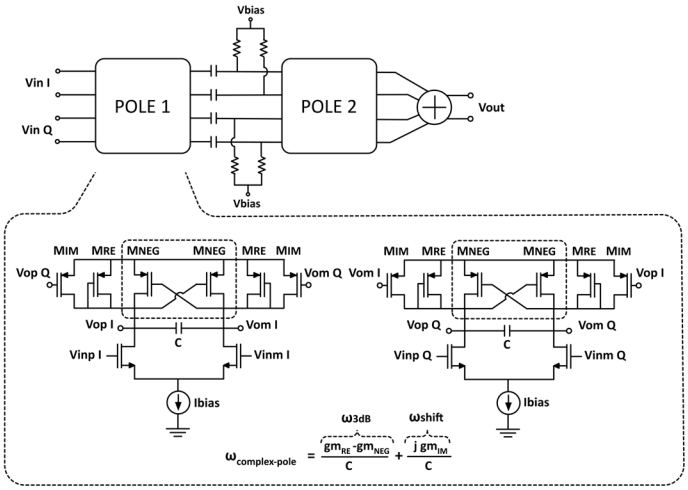

Figure 13.6.4: Baseband complex filter block diagram and schematic of complex pole.

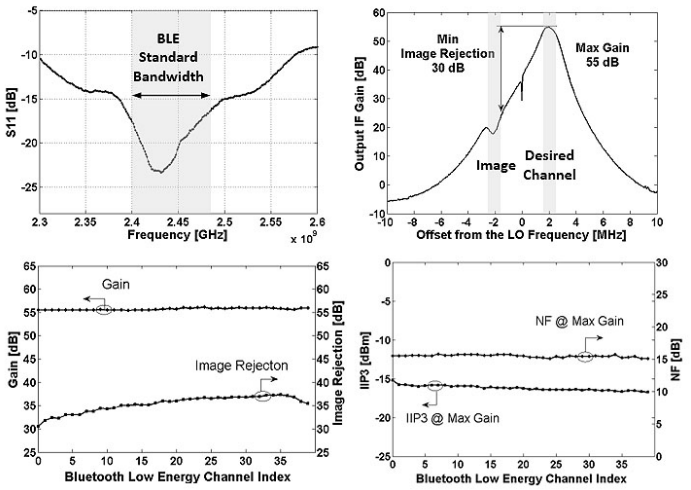

Figure 13.6.5: Summary of the chip measurements: S_{11}, Transfer function, Gain and Image Rejection vs. BLE channel, IIP3 and NF vs. BLE channel.

	This work	[1]	[2]	[3]	[5]	[6]
Power Consumption [mW]	0.6	1.1	1.8	3.6	2.7	1.6
RF Input Freq [MHz]	2400	2400	2400	2400	2400	2400
Voltage Gain [dB] (min/max)	55.5/56.1	-	57.8	75	55	83
Sensitivity [dBm] (min/max)	-84.9/-84.2	-81.4	-88	-	-	-94
NF [dB] (min/max)	15.1/15.8	16*/16.6*	15.7	9	9	6.1
IIP3 [dBm] (min/max)	-15.8/-16.8	-2.9**	-18.5**	-12.5	-6	-21.5
IRR [dB] (min/max)	30.5/37.3	-	37/40	35	28	-
Supply Voltage [V]	0.8	1	1	1.2	0.6/1.2	0.3
Technology	130nm	130nm	65nm	90nm	65nm	65nm
Active Area [mm²]	0.25	-	0.45	0.35	0.26	2.496

* Baseband filter not included in measurement
** Measured at moderate or minimum gain

Figure 13.6.6: Chip summary and comparison with the state of the art.

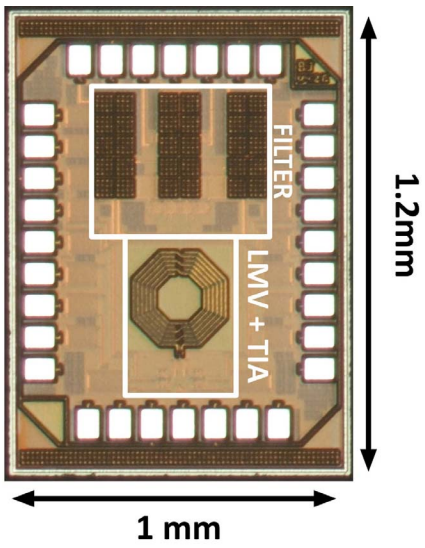

Figure 13.6.7: Die micrograph.

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