Bluetooth Low Energy Receiver System Design

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***Abstract*— An efficient algorithm for a link budget definition of a Bluetooth Low Energy (BLE) receiver is presented. The aim of this paper is to provide a simple procedure that the analog designers can use for a preliminary but reliable definition of the BLE RX building blocks specs. Starting from the BLE standard, the global specifications of the analog front-end are derived (noise figure, IIP3, IIP2, etc.) and, in a second phase, distributed among the building blocks. Finally the system design is validated through simulation results obtained from a Simulink analysis.**

Keywords— RF front-end, analog base-band, link budget, RX architecture, NF, IIP3, IIP2, Bluetooth Low Energy.

I. INTRODUCTION

Several wireless communication standards have been introduced during the past decades with challenging system specifications in order to ensure higher performance in terms of band, cost and quality. One of these is the Bluetooth Low Energy (BLE), that is an extension of the conventional Bluetooth characterized by increased channel spacing and a relaxed interference tolerance to allow for low power implementation. The aim of this paper is to provide the specs for each block of the BLE receiver through a procedure here proposed, whose flowchart is shown in Fig. 1 and that is divided in two main steps. In the first step all the information contained in the standard in terms of sensitivity and linearity are translated into RX global specs in terms of noise figure (NF), third intercept point (IP3), phase noise (PN), etc. These specs are referred to the antenna and are independent of the architecture that will be chosen. In a second phase, once the receiver architecture is defined, the global specs are distributed among the building blocks.

The paper is organized as follows. In Section II all the specifications are derived applying the algorithm, then some simulation results obtained through the Simulink tool and a comparison with the dimensioning reported in literature is reported in Section III. Finally Section IV concludes the paper.

II. BLE RECEIVER: SYSTEM DESIGN

BLE operates in the 2.4GHz ISM (Industrial Scientific Medical) band between 2400-2483.5MHz. There are 40 channels spaced 2MHz with a 1MHz-channel bandwidth B. The modulation is GFSK (Gaussian Frequency Shift Keying), with a modulation index of 0.5, a bandwidth-bit period product equal to 0.5 and a bit-rate of 1Mbps [1,p.16-17]. In the following the standard definition is translated into RX specs in term of noise (quoted as Noise Figure) and linearity (from the analysis of signal spectrum to the IP2 and IP3 request).

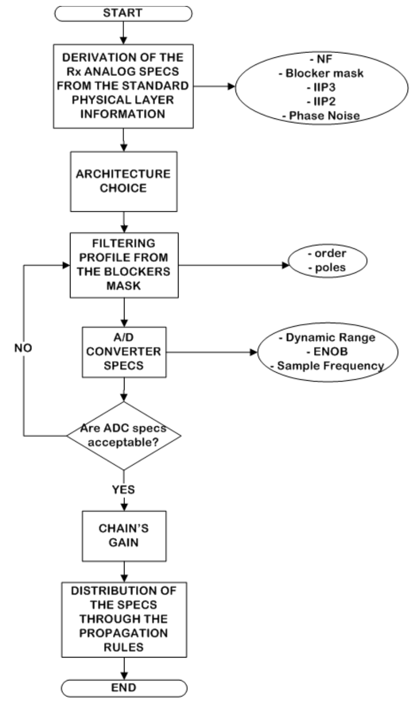

Fig. 1. Flowchart of the system design algorithm.

A. From the Sensitivity to the RX noise figure

The first step is to define the Noise Figure (NF). In BLE, the maximum required BER is 10^{-3}. This BER spec has to be translated into a minimum SNR for the analog front-end ($SNR_{out,min}$). This depends on the modulation scheme adopted by the standard and the assumed type of digital demodulation algorithm. There are several demodulation algorithms[2], which require different $SNR_{out,min}$. In our design, for example, an optimal demodulator will be assumed that requires a $SNR_{out,min}$ equal to 12dB [3]. Other demodulation algorithms would require different $SNR_{out,min}$.

The BLE standard provides a sensitivity level $S_{in|dBm}$ equal to -70dBm. In real design a safe margin is assumed to take into account realization non-idealities effects that would deteriorate the BER. A good compromise for BLE receiver is $S_{in|dBm}$ equal to -80dBm [4][5]. Given that, the NF can be derived from (1) [6][7]:

$$\begin{aligned} NF &= S_{in|dBm} + IL - N_{s|dBm} - SNR_{out,min|dB} = \\ &= -80dBm - 2dB - (-114dBm) - 12dB = 20dB \end{aligned} \quad (1)$$

where $N_{s|dBm}$ = 10log(kTB) is the in-band noise source that

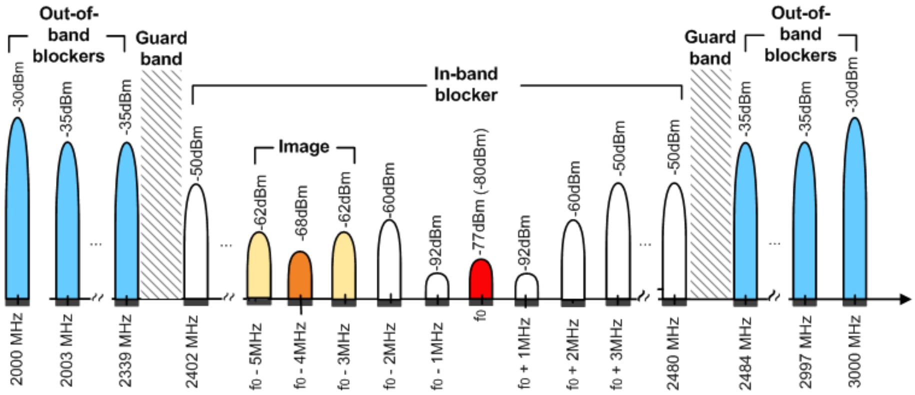

Fig. 2. Blocker mask for the BLE Standard.

depends on the Boltzmann constant k, the signal bandwidth B and the absolute temperature T (300K); IL is the insertion loss of the SAW external filter placed in front of the actual RX. A typical IL value is around -2dB [8]. With a 20dB NF, the resulting Noise Floor is given by [9]:

$$N_{floor} = N_{s|dBm} + NF = -94dBm \tag{2}$$

B. Blocker mask

To achieve linearity specs, an accurate knowledge of the input spectrum is necessary. The useful information to define the blocker mask are reported in the interference performance and out-of-band blocking sections [1,pp.20-21], where all possible interferers that can be present during the radio reception are indicated. These interferers are divided in two main types, the in-band ones and the out-of-band ones[1]. The in-band interferers are channels controlled by the standard and defined in frequency and amplitude w.r.t. the desired signal. The out-of-band interferers are signals due to other standards and have an absolute power in correspondence to an absolute frequency, independently on the received signal. In the blocker spectrum, the received signal (P_{sig}) is not reported at $S_{in|dBm}$ (-80dB, as above defined assuming 10dB safe margin), otherwise in presence of higher interferers, the output SNR would be lower than the required $SNR_{out,min}$. For this reason the standard indicates a margin Δ to $S_{in|dBm}$ that in this case is equal to 3dB, leading to a wanted signal power of -77dBm. A blocker power is intended integrated in 1MHz defining in this way the bandwidth of each interferer. Finally for the out-of-band blockers, the wanted signal should be centered at 2440MHz. The combination of all these information leads to the blocker mask reported in Fig. 2. In the interference section, the standard gives a specific set of power for the image and its adjacent channels suggesting that the most suitable architecture for the receiver is a Low-IF as the one reported in Fig. 3.(a). A complex filter is adopted that offers both channel selection and image rejection. A good choice for the intermediate frequency f_{IF} is 2MHz, resulting from a compromise between the baseband frequency operation (that would require lower f_{IF}) and the power of the image signal (that would require larger f_{IF}) [10][11].

[1] With the term "band", we mean the standard band and not that of the received channel only.

C. From the intermodulation test to IIP3 and IIP2

Once the input spectrum is defined, the linearity spec in terms of IP2 and IP3 can be derived starting from the intermodulation test defined by the standard. According to this test, a minimum BER of 10^{-3} must be achieved when at the input of the receiver the wanted signal 6dB (Δ) higher than $S_{in|dBm}$ and two blockers with a power P_{int} of -50dBm are present [1,p.22]. In order to have an output SNR larger than $SNR_{out,min}$, the sum of the IM3 product and the $SNR_{out,min}$ must be lower than the sensitivity plus the margin Δ. This leads to a maximum IM3 given by N_{floor} + Δ; thus the entire chain minimum IIP3 is equal to [9]:

$$\begin{aligned} IIP3 &= \tfrac{1}{2}(3P_{int} - IM3) = \tfrac{1}{2}(3P_{int} - N_{floor} - \Delta) = \\ &= \tfrac{1}{2}(3*(-50)-(-94)-6) = -31dBm \end{aligned} \tag{3}$$

In BLE standard, there is no a specific scenario for the calculus of the IIP2, but a worst-case combination among the interferers can be derived from the blocker mask. Observing Fig. 2 the worst-case scenario is generated by two in-band blockers with a power level of –50dBm placed at 3MHz and 6MHz from the wanted channel. Assuming P_{int}=-52dBm (considering the SAW IL), the minimum IIP2 is [7]:

$$\begin{aligned} IIP2 &= (2P_{int} - IM2) = (2P_{int} - N_{floor} - \Delta) = \\ &= (2*(-52)-(-94)-6) = -16dBm \end{aligned} \tag{4}$$

This value does not represent an issue since it is definitely below the ones achievable with any architecture.

D. Filtering profile and ADC specs

Once that noise and linearity specs are defined at RX level, the analysis enters into the architecture structure and addresses the spec for the single blocks, as shown in Fig. 3.(a). Starting from the blocker mask, the base band filter and the ADC specs can be determined through an iterative process. Since the filter order determines the maximum blocker amplitude and so the full scale $FS_{@ADC|dB}$, an optimization loop is used to find the best compromise between the filter complexity (and power consumption) and the ADC resolution (in terms of Equivalent Number of Bits (ENOB)). ENOB is defined as [6]:

$$ENOB = (SNDR - 1.76)/6.02 \tag{5}$$

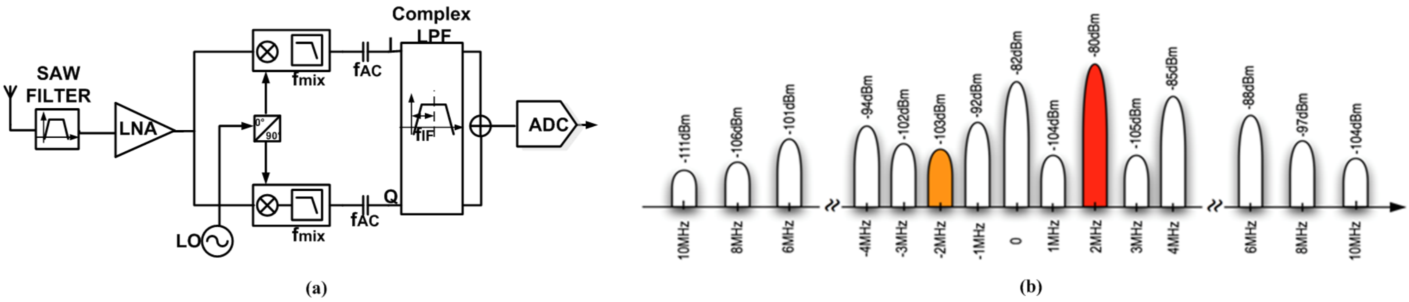

Fig. 3. (a) The proposed architecture for the BLE receiver, (b) filtering effect on the blocker mask.

TABLE I.
DIFFERENT FILTERING PROFILE SCENARIOS

Mixer pole f_{mix} [MHz]	Filter Order	f_{AC} [kHz]	Critical blocker Amplitude [dBm]	Critical blocker frequency [MHz]	SNDR [dB]	ENOB
5	1	200	-72	6	51	8.18
5	**≥2**	**200**	**-80**	**2**	**24**	**3.69**
3	1	200	-73	0	41	6.52
3	≥2	200	-81	2	24	3.69
5	1	100	-72	6	51	8.18
5	≥2	100	-80	2	24	3.69
3	1	100	-73	0	41	6.52
3	≥2	100	-81	2	24	3.69

where SNDR represents the Signal-to-Noise-Distortion ratio at the ADC input that can be evaluated from (6):

$$SNDR = FS_{@ANT|dB} - N_{floor|dB} + Margin_{FS|dB} \qquad (6)$$

where $FS_{@ANT|dB}$ corresponds to the amplitude of the maximum signal in the blocker mask once the filtering profile is applied around the wanted channel, while $N_{floor|dB}$ is given by (2). A margin $Margin_{FS|dB}$ is taken into account to model some non-idealities such as: modulated signal crest factor, DC offset control gain and mismatches. In this case $Margin_{FS|dB}$ has been set equal to 9dB coming from a 3dB crest factor of the modulated channels (GFSK) and 6dB of minimum gain step ΔG that the standard allows at the receiver input once the signal increases above the minimum level. Notice that the SNDR has been evaluated at the antenna, normalizing $FS_{@ADC|dB}$ and $N_{floor@ADC|dB}$ for the chain total in-band gain. In this way the choice of the base-band filtering profile/order and the ADC ENOB are independent on the receiver chain overall gain, simplifying significantly the dimensioning. Although the blockers are mainly attenuated by the base-band filter, the filtering profile must include the effect of all the building blocks preceding it. The LNA can be considered wideband for the in-band blocker since even in presence of a resonant LNA, the typical quality factor would be around 10 at 2.4GHz. The mixer generally provides at its output a first attenuation of the in-band blockers through a 1st-order low-pass filter (generally implemented by a RC load). In this case, having adopted a Low-IF architecture, an AC coupling can be added after the mixer in order to suppress the blocker around DC. Assuming for the channel selection filter a Butterworth profile, center frequency and bandwidth can be defined. The center frequency will be equal to the adopted IF (i.e. 2MHz) while the bandwidth will be slightly larger than the desired channel (1.2MHz) to guarantee good flatness in the signal band. Once set these parameters, through an iterative process it will be possible to find: the complex filter order, the LP filter cut-off frequency f_{mix} due to the pole at the mixer output and the cut-off frequency f_{AC} of the AC coupling. In Table I, some combinations are reported and for every case SNDR and ENOB have been calculated using (5) and (6). It is possible to verify that a 2nd or higher order profile for the complex filter allows lowering the blockers below the wanted signal. This situation represents the best condition for the ADC resolution since the SNDR is limited by the required $SNR_{out,min}$. Assuming the configuration highlighted in Table I, the blocker mask at the input of the ADC becomes the one reported in Fig. 3.(b). The number of bit required to the ADC is equal to 4 considering that the SNDR is roughly 24dB given by: $SNR_{out,min|dB}$=12dB, $Margin_{FS|dB}$=9dB, and 3dB due to interferers intermodulation product falling in the wanted signal band. From the diagram in Fig. 3(a) and supposing a Nyquist ADC, it is possible to fix the minimum ADC sampling frequency f_s = 10MHz, in order to have that the power of the interferer folded in band is below the Noise Floor of more than 10dB and it does not deteriorate the SNR. Notice that for other ADC architectures, as the oversampling one, f_s would be higher, relaxing also the requirement on the filter order.

E. Chain's gain and specs distribution

Once the global specs have been defined, the linearity performances (in consideration of the input spectrum) have driven the filter order and the ADC resolution. Now the maximum chain gain G_{max} can be evaluated and the noise performance will drive the definition of the gain distribution along the chain, in order to have the noise level negligible w.r.t. the linearity performance. For this example the ADC input swing is set equal to 1V (assuming 1.2V supply voltage), leading to a maximum swing tolerable at the input of the ADC $S_{maxADC|dBV}$ equal to 0dBV. With a maximum signal (in this case the wanted one) $A_{maxSignal|dBV}$=-90dBV, G_{max} is given by:

$$\begin{aligned} G_{max} &= S_{max\,ADC|dBV} - A_{max\,Signal|dBV} - \Delta G = \\ &= 0dBV - (-89dBV) - 6 = 83dB \end{aligned} \qquad (7)$$

A summary of the overall specifications of the BLE receiver is shown in Table II and compared with a design present in literature [5], exhibiting a good matching.

The last step in the system level design consists on assigning gain, NF and linearity to each RX block in such a way to fulfill the global specs. The gain distribution among the

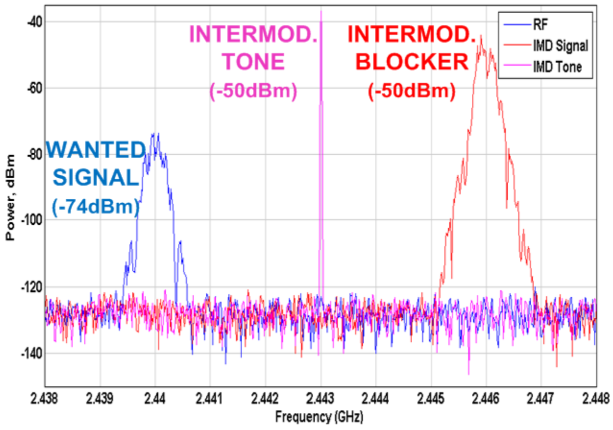

Fig. 4. Receiver Input signals.

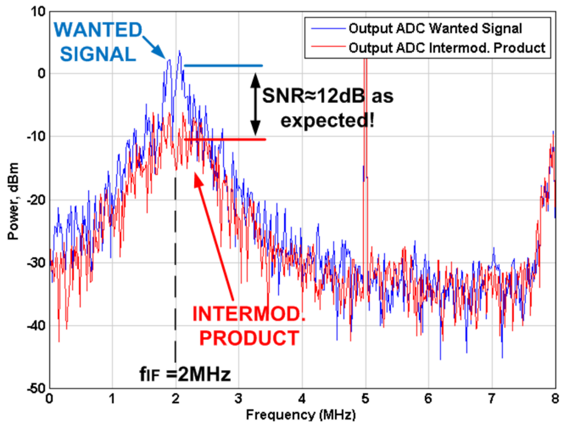

Fig. 5. Output ADC signal: desired signal (blue line) and intermodulation product (red line).

TABLE II.
BLE Rx SPECIFICATIONS AND COMPARISON WITH STATE OF ART

Parameter	This Work	[5]
Sensitivity	-80dBm	-81.4dBm
NF	20dBm	16dBm
IIP3	≥-31dBm	-2.9dBm
$SNR_{out,min}$	12dB	14.8dB
ENOB	4	4
Sample Frequency	≥10MHz	20MHz
Supply voltage	1.2V	1V

TABLE III.
EXAMPLE OF SPECS DISTRIBUTION FOR BLE RECEIVER

Parameter	LNA	AC coupling	Mixer	Complex filter	Total specs	Target specs
Gain	5mS	-0.04dB	2kΩ	63dB	82.3dB	83dB
NF[dB]	14	0	0.25	30.82	15.83	20
IIP3[dBm]	-25	134	-46	-5	-28.42	-31
IIP2 [dBm]	10	134dB	24	20	0.34	-16

different building blocks requires a second iterative optimization because the gain preceding and following each block determines its impact on the overall specs of noise and power consumption. The specs distribution has been performed automatically in Excel, using the so-called *'propagation rules'* [6][12]. In Table III, an example of specs distribution compared with the target ones obtained through the algorithm is indicated, with the following assumptions: the LNA has a transconductance gain; the mixer is in current with a resistive gain (over a load or a trans-impedance amplifier).

III. SIMULATION RESULTS

In order to verify the performance of the BLE receiver dimensioned as indicated in section II, the architecture shown in Fig. 3(a) has been simulated in a time-domain system level simulation tool as Simulink, using the SimRF toolbox. A two-tone test has been set up, as indicated in the standard. Fig. 4 shows the input signals, in Fig. 5 ADC output signals can be observed, i.e. the desired signal (blue line) and the IM product fallen in band (red line). There are about 12dB between the two signals at 2MHz, that is the expected SNR.

IV. CONCLUSIONS

Starting from the BLE standard, a quick and efficient dimensioning of each building block of the receiver chain (LNA, mixer, base-band filter, ADC) has been derived. The used algorithm is easy to be used and implemented with a software (in MATLAB or Excel) to achieve fast and large optimization. For the BLE case, here developed in details, the achieved results simulated in SimRF time-domain environment have validated the approach, with also a good matching with the other solutions provided in literature.

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