# Sub-mW Current Re-Use Receiver Front-End for Wireless Sensor Network Applications

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***Abstract*—In this paper, a receiver front-end tailored to Bluetooth Low Energy applications is presented. In the proposed solution, the LNA, mixers, VCO, quadrature scheme and the first stage of the analog base-band share the same bias current under a 0.8 V voltage supply leading to a sub-mW power consumption. A channel selection filter, implemented through a current re-use gm-C topology, completes the design. The presented prototype, realized in 130 nm CMOS technology, occupies an active area of 0.25 mm$^2$ while consuming only 0.6 mW. With a NF of 15.8 dB, an IIP3 of −17 dBm at the maximum gain and an image rejection above 30 dB the receiver front-end meets BLE noise figure, image rejection, phase noise and linearity requirements.**

***Index Terms*—Biquad, BLE, complex poles, current re-use, Gm-C filter, LMV cell, low power, receiver, RF front-end.**

## I. Introduction

BLUETOOTH LOW ENERGY (BLE) is the new operative mode introduced in the fourth release of the Bluetooth wireless technology standard [1]. BLE operates in the same 2.4 GHz ISM radio band as classic Bluetooth, however is tailored towards ultra-low power devices powered by coin-cell batteries, such as wireless sensor networks (WSN) for indoor localization, wireless payment tags, and wearable devices. In such applications, performance can be sacrificed in favor of an extended battery-life obtained by minimizing the overall power consumption of the radio. With a target sensitivity of −70 dBm, a BLE-compliant receiver can have noise figure (NF) close to 30 dB, 21 dB of image rejection and IIP3 higher than −30 dBm [2]. Such relaxed specifications make BLE-based transceivers ideal for reducing the cost and power consumption in short-range communication devices. Although linearity and noise specs have been significantly relaxed, the design of a sub-mW solution remains challenging since the power dissipation cannot be simply scaled with the spurious-free dynamic range (SFDR). In fact, the ultimate bound is set by the power burned in the voltage-controlled-oscillator (VCO), which is used for the generation of the local oscillator (LO) that is necessary for signal down-conversion. In this case the spectral purity for the local oscillator demands a minimum phase noise lower than −102 dBc/Hz at an offset of 2.5 MHz from the carrier [2]. Although such relaxed specifications could be satisfied with a ring oscillator, in ultra-low power applications the use of LC topologies is generally preferred since, for a given phase-noise requirement, the former consumes more power than the latter [3]. Nevertheless, the LC-VCO remains to be one of the most power-hungry blocks in the receiver chain, owing to the current required to sustain the tank oscillation. Using an LC oscillator, a straightforward approach to reduce the power consumption of the VCO is to use a high-Q tank like the FBAR as suggested by Wang *et al.*, paying an extra cost for the use of a non-conventional technology [4]. An alternative strategy widely used in literature is to share the bias current among different blocks of the receiver chain [5]–[10].

This work is based on the LMV cell topology originally introduced by Liscidini *et al.* in 2006, where the low noise amplifier (LNA), mixer and VCO and quadrature scheme share the same bias current without requiring extra voltage headroom compared to the nominal voltage supply (Fig. 1) [10]. Starting from the design described by Tedeschi *et al.* [5], the proposed receiver will reach sub-mW power consumption by introducing four key elements: a complementary LC VCO shared between I and Q paths, a low voltage quadrature LNA, a pseudo-differential trans-impedance amplifier biased with recycled current from the RF front-end, and finally a base-band channel selection filter realized through a current re-use gm-C topology [11].

The paper is structured as follows. In Section II, the current re-use RF front-end will be presented, highlighting the key building blocks that allow for a sub-mW power consumption. Section III will describe in detail the current re-use base-band channel selection filter. Section IV will include some details on the integrated prototype and measurement results, while conclusions will be reported in Section V.

## II. Current Re-Use RF Front-End

The LMV (stacked LNA-Mixer-VCO) cell, shown in Fig. 1, takes advantage of current recycling techniques in order to merge three fundamental blocks in a Low-IF receiver (LNA, Mixer, VCO) into a single, power efficient block [10]. While the LMV cell is an excellent strategy for power savings, it is not without limitations. First, the originally proposed LMV cell uses an oscillator topology that is not fully optimized for low power applications. Specifically, the VCO topology originally presented uses only half the bias current to sustain the tank oscillations in each semi-period, limiting the minimum power consumption for a given tank. Furthermore, in

Manuscript received April 26, 2015; revised July 06, 2015; accepted July 14, 2015. Date of publication August 19, 2015; date of current version November 24, 2015. This paper was approved by Guest Editor Jussi Ryynanen.

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Digital Object Identifier 10.1109/JSSC.2015.2461019

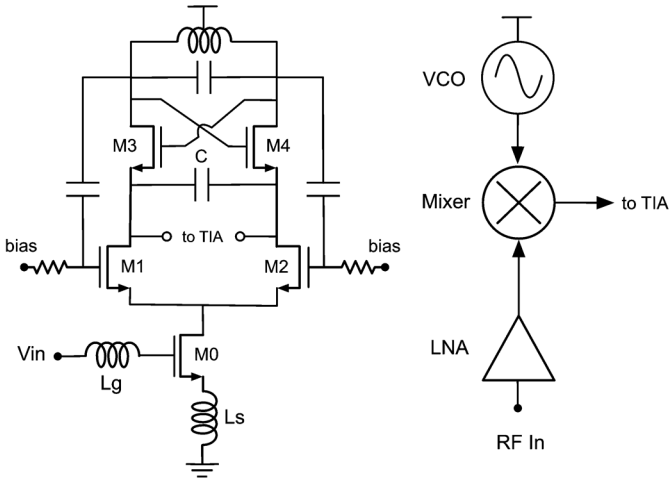


Fig. 1. LMV cell originally proposed by Liscidini *et al.* [9].

low-IF topologies where quadrature paths are required for image rejection, the LMV cell would require the usage of two tanks, drastically increasing the size of the design [10]. Finally, parasitic capacitances at the IF output node of the LMV cell limit the conversion gain of the LMV cell for both current and voltage mode solutions. These limitations, along with the design solutions proposed for realizing the proposed receiver will be addressed next, reaching a sub-mW operation suitable for BLE applications.

### *A. Complementary LMV Cell*

As previously reported, the current required to sustain the oscillations is often the limiting factor for power consumption in ultra-low power receivers, based highly on the quality factor (Q) of the tank. While a low Q tank would require larger bias current to counteract tank losses, it was shown by Tedeschi *et al.* that high Q could negatively affect the conversion gain of the original LMV cell [5]. To counteract this, a variation of the original LMV cell adopting a differential LC tank was proposed in [5]. By adopting a tank resonating at the oscillation frequency only for differential signals and an nMOS-type cross-coupled VCO, Tedeschi *et al.* demonstrated that the quality factor of the inductor plays a negligible effect on the conversion gain of the cell, allowing the use of higher Q tank while consuming less current.

In the topology presented in this paper, a complementary cross-coupled VCO topology has been introduced to further reduce the tail current requirements of the oscillator. The result is that, for a given output amplitude $V_{LO}$, the complementary VCO can be biased with half the current of the nMOS topology [5]. This approach has been adopted previously in another LMV cell architecture proposed by Camponeschi *et al.* halving the minimum power consumption of the cell [6]. However in [6], the quadrature scheme was implemented cross-coupling two independent cells partially eliminating the power advantage obtained by the use of a complementary topology.

Typically, each design solution introduces a trade-off that must be paid. In this case, the cost is an extra overdrive voltage from the additional cross-coupled pair. As mentioned before, the BLE standard has been developed towards autonomous wireless devices supplied by coin batteries and energy-harvesting solutions, such as photovoltaic cells, which are limited

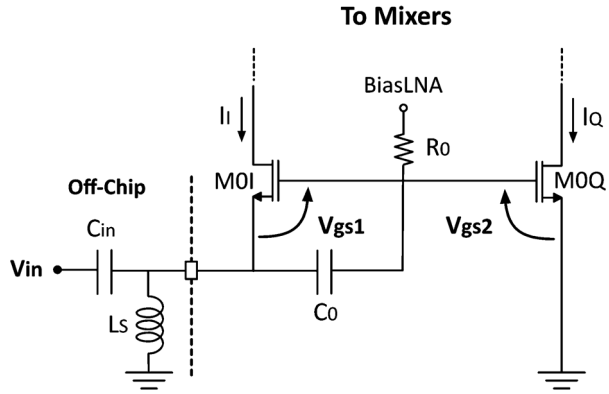


Fig. 2. Quadrature low noise amplifier working principle (bias not shown).

in the voltage supply that they can produce. In favour of maintaining this compatibility, the additional overdrive voltage required by the complementary VCO was recovered through adopting the new low-voltage drop quadrature LNA described in the next section.

### *B. Low Voltage Quadrature LNA and Input Matching*

In traditional RF front-end receivers, quadrature generation is implemented at level of the local oscillator (LO) used to drive independent I and Q mixers. A common approach to generate a quadrature LO is through a VCO operating at twice the LO frequency followed by a divider. While this implementation is able to generate accurate quadrature signals, the dividers operating at the double of the carrier frequency leads to high power consumption when a low cost technology (e.g., 130 nm and above) is adopted. Such strategy becomes competitive only for shorter channel length as shown in [12], [13]. Quadrature LO signals can also be generated through poly-phase RC filters, which rely heavily on the matching of the devices to provide adequate quadrature accuracy. Although passive, such networks demand more current to be driven, increasing the overall power consumption of the receiver. In low-IF architectures, image rejection presents a major challenge due to non-idealities in quadrature generation, which limits the maximum level of rejection achievable. For this reason, in the case of strict requirements the former of the two solutions described is often used, despite the increased cost in power consumption.

For the up-and-coming low energy standards such as ZigBee or Bluetooth Low Energy, larger tolerances on blockers allows designers to trade off accuracy for power consumption. Bluetooth Low Energy, for example, requires only 21 dB of image rejection [1]. This relaxes the accuracy requirement on quadrature generation and opens to the possibility of performing quadrature on the RF signal path. By implementing quadrature generation on the RF signal path as opposed to LO, Tedeschi *et al.* demonstrated that a differential LC tank can be shared between the I and Q paths [5]. This not only results in less space that would otherwise be occupied by two inductors dominating chip area, but through tank sharing the bias current between the I and Q can be used at the same time to sustain a single oscillation, improving the overall power efficiency of the cell.

In the proposed design, the low noise amplifier drawn in Fig. 2 generates the quadrature on the RF signal path. A single RC network behaves, at the same time, as a low-pass filter for the common-gate stage (CG) implemented by M0I, and as a

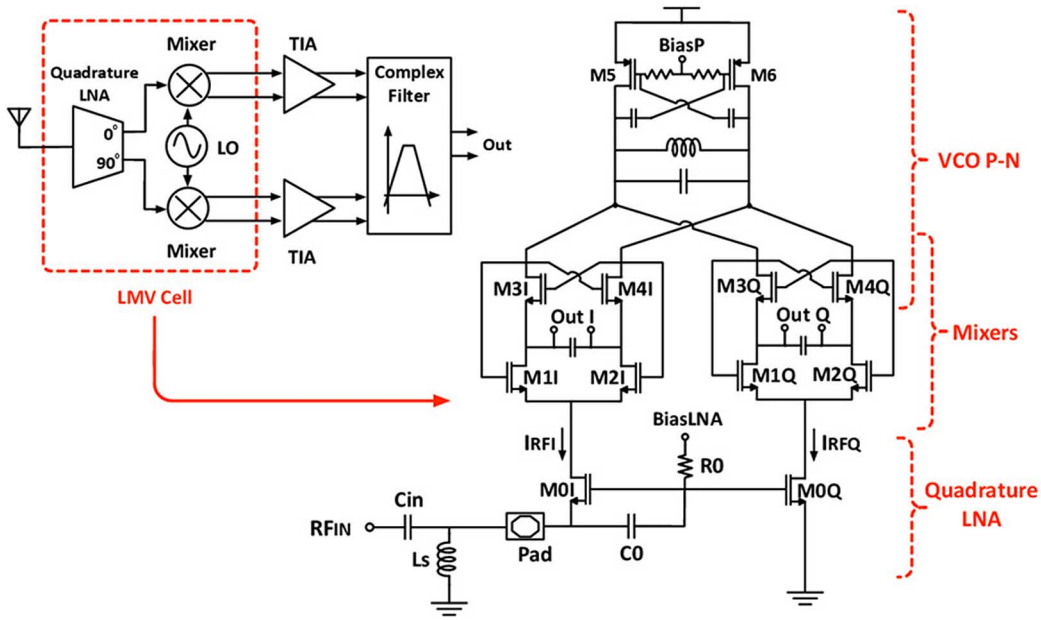


Fig. 3. Block diagram of the integrated BLE receiver and P-N LMV cell (bias not shown).

high-pass filter for common source stage (CS) realized with M0Q, generating a 90-degree shift between the two outputs currents. A wideband quadrature is guaranteed by choosing C0 larger than gate-source capacitances of M0I/M0Q, while amplitude matching is obtained only around the filter cut-off frequency $1/\mathrm{R_0C_0}$. The accuracy of this approach can be evaluated from the expression of the two output currents ($\mathrm{I_I}$ and $\mathrm{I_Q}$) as function of the input signal $\mathrm{V_{in}}$:

$$\frac{I_I}{V_{in}} = g_m\left(\frac{-1}{1+sR_oC_o}\right) \tag{1}$$

$$\frac{I_Q}{V_{in}} = g_m\left(\frac{sR_oC_o}{1+sR_oC_o}\right) \tag{2}$$

where $\mathrm{g_m}$ is the transconductance of the two transistors. From (1) and (2) it is clear that the quadrature phase relationship between the I and Q paths occurs over a wide range. On the contrary, precise amplitude matching can only be obtained around filter cut-off frequency $\omega_0 = 1/\mathrm{R_0C_0}$. However, since the BLE standard bandwidth is of only 83.5 MHz around 2.44175 GHz, good amplitude matching and image rejection can be obtained over the entire bandwidth without re-centering the $\omega_0$ for each channel. In fact, by examining equations (1) and (2), it can be shown that the amplitude mismatch between the I and Q paths is equal to:

$$|I/Q| = \omega_c R_o C_o = \frac{\omega_c}{\omega_o} \tag{3}$$

where $\omega_\mathrm{c}$ is the carrier frequency and $\omega_0$ the RC cut-off frequency. In the case of BLE, by choosing $\omega_0$ at the center of the ISM band, the largest amplitude error between I and Q paths, occurring for the first and the last channel of the standard (i.e., channels 1 and 40), is approximately 6%. Such amplitude mismatch leads to a maximum image rejection around 30 dB, leaving a 9 dB margin above the BLE standard requirements of 21 dB. Typically, a single-stage poly-phase filter relies on two RC networks to realize a 90-degree shift, one used to generate a high-pass response and one to generate low-pass response [5]. In this topology a single RC network is used to implement both allowing an easier calibration. In fact, any PVT variation in the resistor or the capacitor affects both I and Q paths equally by shifting only the center frequency, while maintaining a quadrature relationship. To assure adequate amplitude matching, a single calibration is required to center the filter cut off frequency in the ISM band. This can be performed through use of a transistor operating in triode region in series with the resistor R. The I/Q quadrature relationship is also independent of the matching network preceding the LNA, guaranteeing robustness with the respect to external components variations.

Input matching is obtained through the use of an external inductor and capacitor (Fig. 3). The inductor not only provides the path for the DC bias current of the in-phase component, but also compensates for the variability of the bond-wire variations from chip to chip. By choosing $\mathrm{C_0} = \mathrm{g_m}/\omega_0$ (i.e., $\mathrm{R_0} = 1/\mathrm{g_m}$) the LNA input impedance has the following expression:

$$Zin = \frac{1 + j\omega_0 \mathrm{g}_m L_s - C_{in}L_s\omega_0^2}{j\omega_0 C_{in} - \mathrm{g}_m C_{in} L_s \omega_0^2} \tag{4}$$

where $\mathrm{g_m}$ is equal to the transconductance of input transistors M0I/MOQ, and $\mathrm{L_s}$ and $\mathrm{C_{in}}$ correspond to the external matching components, as shown in Fig. 3. By setting $\omega_0$ to the center frequency of the ISM band, the imaginary component of the input impedance can be nulled through selecting:

$$C_{in} = \frac{1 + (\mathrm{g}_m L_s \omega_0)^2}{L_s \omega_0^2} \tag{5}$$

Matching to the source resistance Rs can then be achieved by choosing the external inductor value to be equal to the following expression:

$$Ls = \sqrt{\frac{Rs}{\mathrm{g}_m \omega_0^2 (1 - \mathrm{g}_m Rs)}} \tag{6}$$

This analysis led to actual component values of 900 fF and 3.9 nH for $\mathrm{C_{in}}$ and $\mathrm{L_s}$, respectively.

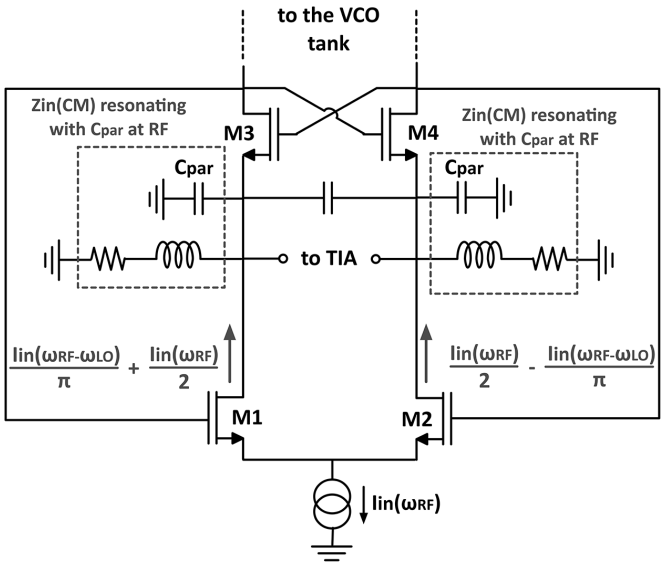


Fig. 4. Resonant output network for RF common-mode signal.

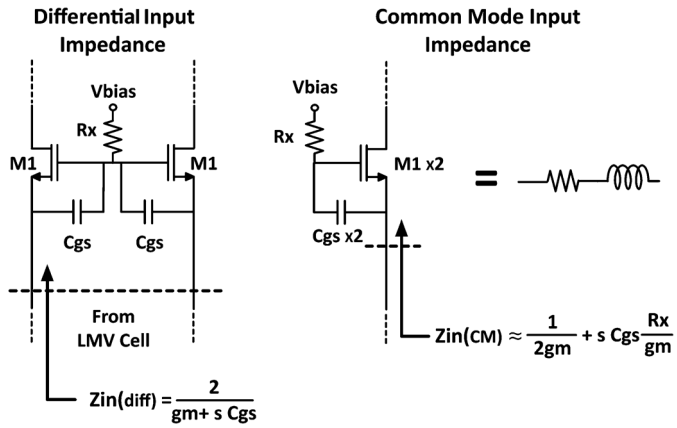


Fig. 5. Common gate TIA with common-mode inductive input impedance.

Notice also that $C_{in}$ and $L_s$ together form a narrow-band filter network with a certain quality factor. This is beneficial for two reasons: the amplification of the signal by a factor of Q at the resonant peak tuned to the input frequency, and the filtering of unwanted components around $2f_{LO}$ from being injected into the system and potentially locking the oscillator (see further details in Section IV).

### C. Current Re-Use TIA and Loss Cancellations

In all of the LMV cells presented in literature, the trans-impedance amplifier used to sense the down-converted signal does not share its bias current with the RF front end of the cell [5], [10]. The reason is due to the need to minimize the common-mode parasitic capacitances at the output of the cell, responsible for conversion losses [10]. In this section it will be shown that a simple common gate stage, that usually offers a large common-mode input capacitance, can be modified to be fully compliant with the LMV cell, allowing bias sharing and the minimization of conversion losses.

In [10], it was demonstrated that common-mode parasitic capacitances at the output node of the LMV cell reduce the conversion gain of the cell. In particular, the switches of the LMV cell can be seen as the cascade of two mixers (M1-M2 and M3-M4) with a conversion gain of $1/\pi$. As shown in Fig. 4, the first mixer (M1-M2) has a common-mode component at RF, which is later down-converted by M3-M4. Common mode parasitic capacitances at the output of the cell filters this common-mode RF component before entering the second switching-pair M3-M4, leading to a conversion loss. For this reason, the TIA following the LMV cell must have a large common-mode input impedance at RF to minimize these losses, but at the same time, have a low differential input impedance at IF to absorb the down-converted signal.

The proposed TIA has been implemented with a differential common gate stage with the addition of a common-mode resistor $(R_x)$ in series to gates of the transistor (Fig. 5). Due to the presence of resistor $R_x$, the common-mode input impedance of the CG $(Z_{in,CM})$ is equal to:

$$Z_{in,CM} = \frac{1}{2}\left(\frac{1}{g_m} + \frac{j\omega R_x C_{gs}}{g_m}\right) \tag{7}$$

where $g_m$ is the transconductance of M1s, while differential input impedance remains equal to approximately $2/g_m$ below the transistor cut-off frequency. For the common-mode signal, the resistor $R_x$, combined with the transistor capacitances $C_{gs}$, creates an active inductor that not only provides an high impedance at RF but it can be strategically chosen to resonate at the LO frequency with the common-mode capacitance $C_{par}$ already present at the output of the LMV cell (Fig. 5). At resonance, the original parasitic impedance $(1/\omega_{RF}C_{par})$ is multiplied by the quality factor of the resonance that is dominated by the quality factor of the active inductor, expressed by (7) at $\omega_{RF}$ (i.e., $\omega_{RF}R_xC_{gs}$). Notice that the common-mode resistor $R_x$ has no effect on differential signals for both noise and signal transfer function. The use of a common gate stage, not only allows for the reduction of conversion gain losses, but also allows for the sharing of the entire TIA bias current with the LNA, minimizing the overall power consumption. The complete RF portion of the BLE Receiver plus the TIA is shown in Fig. 6.

The benefit of the use of the proposed approach can be appreciated by the plot reported in Fig. 7, where the gain of the RF front-end (sensed at the output of the TIA) is plotted versus $R_x$. For small values of $R_x$, the LMV cell experiences a low conversion gain due to the presence of large common-mode capacitors at the output of the cell formed by transistor parasitic capacitances from M2, M4, and the TIA. This parasitic load absorbs part of the RF signal before it can be fully down-converted by the LMV cell. On the contrary, for very large values of $R_x$, the common-mode input impedance of the TIA increases and with it the conversion gain of the cell. This, however, does not eliminate the parasitic capacitances of transistors M2 and M4, which is still able to degrade the cell's gain performance. The maximum gain is reached for an intermediate value (around 800 Ω), where the inductive common-mode impedance presented by the

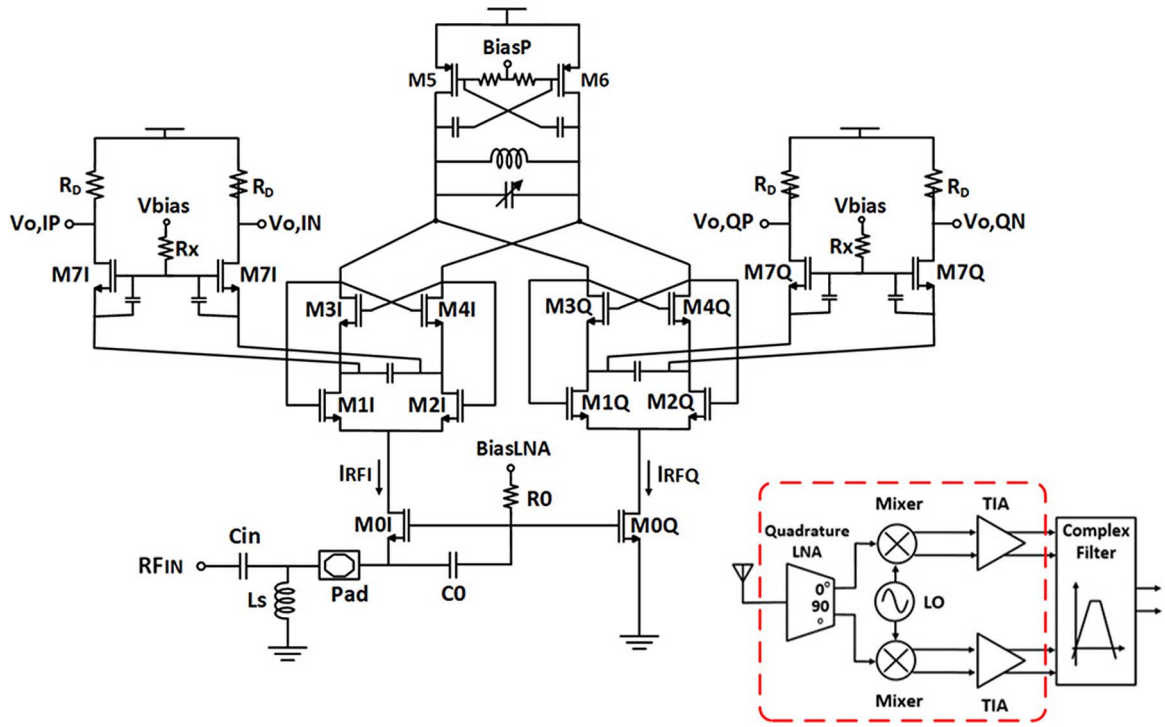


Fig. 6. Complete quadrature RF front-end with baseband TIA.

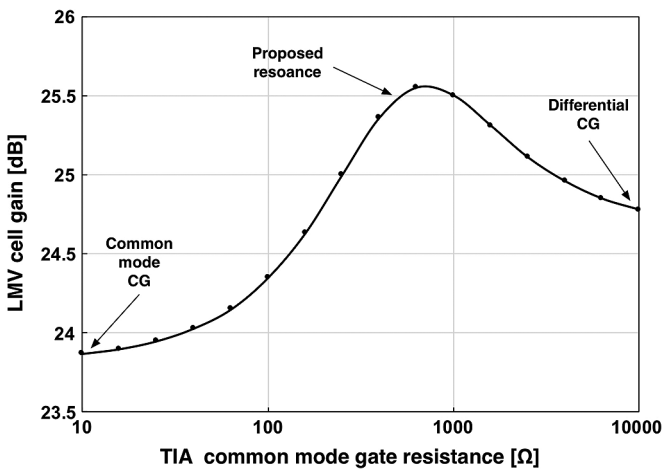


Fig. 7. Simulation impact of TIA gate resistance in LMV cell gain.

TIA resonates with the common-mode parasitic capacitances at the output of the cell.

## III. Current Re-Use Base-Band Filter

The trans-impedance amplifier is followed by a gm-C complex filter used for channel selection and image rejection (Fig. 8). In this topology, a real Gm-C filter is transformed into a complex one, by introducing cross-connected transconductance $\mathrm{gm_{IM}}$ between the I and Q paths (by the use of the additional transistors $\mathrm{M_{IM}}$). This creates a frequency shift that is proportional to $\mathrm{gm_{IM}}$ resulting in an asymmetry in the frequency response appropriate for image rejection:

$$\omega_{complex} = \frac{gm_{RE}}{C} + j\frac{gm_{IM}}{C} = \omega_{3\ \mathrm{dB}} + j\omega_{shift}. \qquad (8)$$

A clever implementation of the Gm-C filter is in the hybrid solution presented by Lin *et al.* [8]. In this topology, the filter response is produced by a complex load that shares its bias current with the preceding gain stage. Unfortunately in the original scheme, the transistors forming the complex load creates a positive feedback loop for common-mode signals that sets a constraint in the choice of $\mathrm{gm_{RE}}$ and $\mathrm{gm_{IM}}$.

Generally, in fully differential structures a positive feedback loop can occur for common-mode signals, when an inversion in sign is exploited by cross coupling the positive to negative branches. However, this generally is not an issue due to the high common-mode rejection in a fully differential structure. In the structure proposed by Lin, however, the load is pseudo-differential and therefore the common-mode and differential signals have the same gain. For this reason, a stability issue occurs. In particular, considering just the load, it is possible to identify 4 inversion stages that form the positive feedback loop. This makes the structure latch if the loop gain is greater than 1, (i.e., $\mathrm{gm_{IM}} > \mathrm{gm_{RE}}$). Under this restriction the imaginary part of the pole cannot be larger than the real one resulting in a filter center frequency smaller than the filter pass-band.

This constraint has been removed in the topology presented in this paper, by adding cross-coupled transistors $\mathrm{M_{NEG}}$ in parallel to the complex load. This technique, introduced for the first time by Nauta *et al.* in [14], was used to produce different gains for common-mode and differential signals, damping the former with a positive resistance and boosting the latter with a negative one. This strategy for improving the stability of the hybrid complex filter has been discussed in [11] but it was implemented for the first time in this design.

The differential negative resistance in parallel to the diode-connected transistor $\mathrm{M_{RE}}$ sets the filter pass-band while the gain

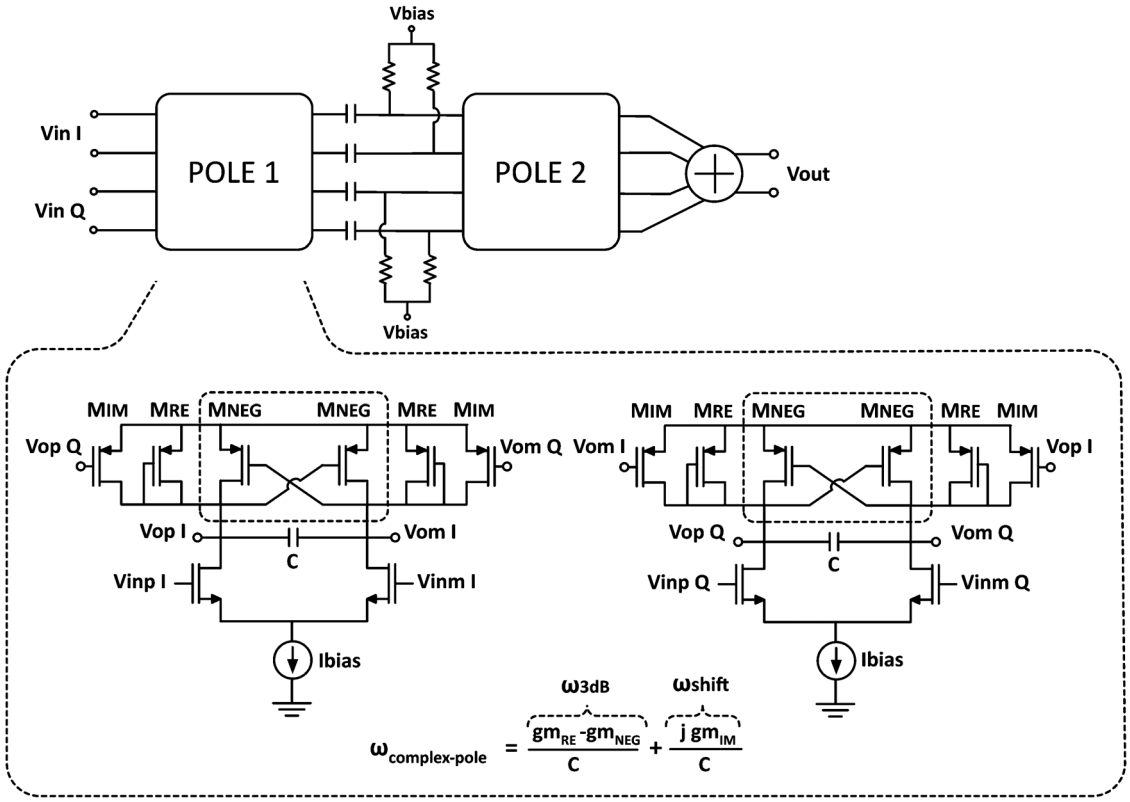


Fig. 8. Baseband complex filter block diagram and schematic of complex pole.

TABLE I
POWER CONSUMPTION BY SUB-BLOCK

| Sub-block | Consumption |
|---|---|
| **LMV+TIA** | **530uA** |
| VCO 170uA | |
| TIA 180uA x2 | |
| LNA 530uA | |
| Baseband Filter | 150uA |
| Total Current | 680uA |
| Total Power (Supply 0.8V) | 544uW |

of the common-mode feedback loop is kept lower than one preventing the latching. The new location of the complex pole can be shown to be:

$$\omega'_{complex} = \frac{gm_{RE}(eff)}{C} + j\frac{gm_{IM}}{C} = \frac{(gm_{RE} - gm_{NEG})}{C} + j\frac{gm_{IM}}{C} \quad (9)$$

The result is the flexibility in the choice of the pole location without compromising the stability of the system.

## IV. SUB-MW RECEIVER DESIGN AND MEASUREMENT RESULTS

The RF front-end in Fig. 6 was integrated in a front-end receiver for BLE applications along with a second-order Butterworth complex filter (center frequency 2 MHz, bandwidth 1 MHz) realized using the gm-C cell in Fig. 8. The input transistor pair M0I, M0Q amplifies the incoming RF signal and

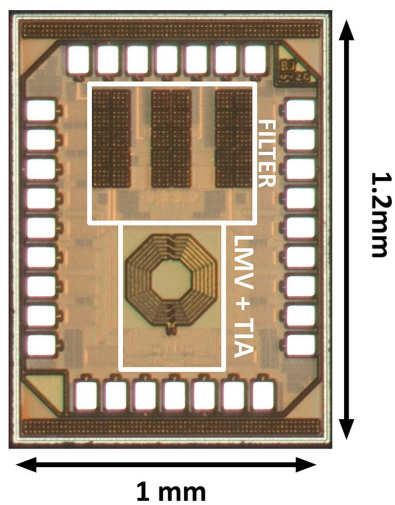


Fig. 9. Die micrograph.

generates the in-phase and quadrature components. These signals are then down converted to 2 MHz using M1I to M4I and their corresponding counterparts in the quadrature path. At this point, the TIA amplifies and delivers the baseband I and Q components to the complex base-band filter. The chosen architecture is a low-IF at 2 MHz. The chip was fabricated in 130 nm IBM CMOS technology (with regular voltage threshold) to limit the cost of the wireless node. The chip occupies a footprint of 1.0 mm by 1.2 mm, with an active area of 0.25 mm$^2$. A micrograph of the die is shown in Fig. 9.

The current consumption for the different building blocks is shown in Table I. The LMV cell and the TIA consume a total of 530 uA. This current, totally absorbed by the quadrature

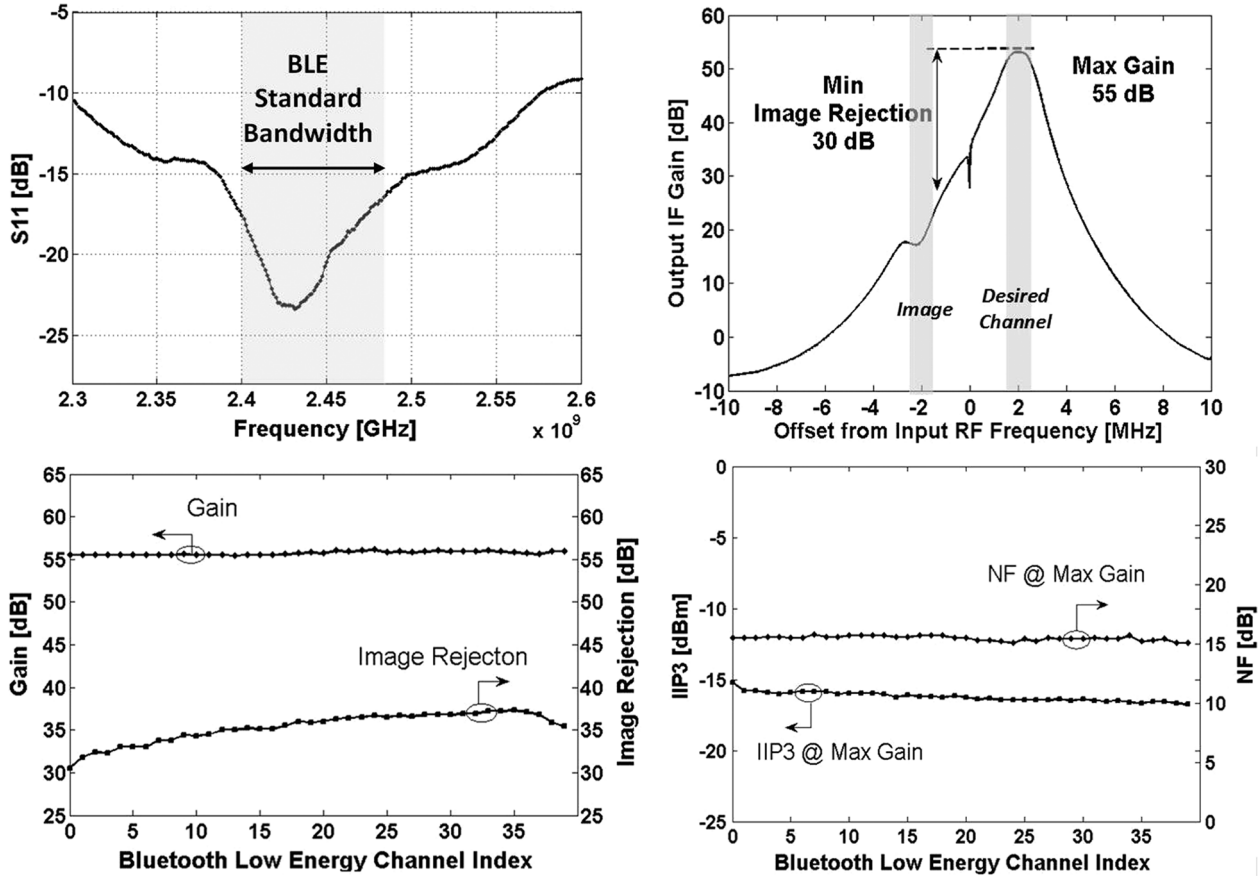


Fig. 10. Chip measurements showing S11 matching, AC transfer function, gain and image rejection vs. BLE channel, IIP3 and NF vs. BLE channel.

LNA, is divided between the VCO (which is also the mixers) and the TIAs. Thanks to the complementary cross-coupled VCO topology, only 170 uA was required to guarantee a proper oscillation. The VCO tank is based on an integrated inductor of 9.8 nH with a quality factor from simulation equal to 16. Channel selection is achieved by tuning the local oscillator on board. Although the PLL has not been included in this design, the power estimated for the required dividers and additional building blocks would not exceed 200 microwatt in the IBM 130 nm technology upon the implementation proposed in [2] assuming a voltage supply of 0.8 V. While 85 MHz tuning range is sufficient for BLE, a tuning range of 20% was designed for to account for PVT variations of the oscillator.

The $|S11|$ measurement, obtained using the Rohde & Schwarz ZVH8 shown in Fig. 10(a), shows good matching over the entire Bluetooth Low Energy spectrum ($<-15$ dB) bandwidth of 83.5 MHz. Fig. 10(b) reports the transfer function of the entire chain, measured at the maximum gain by sweeping the RF input across the LO frequency with an input tone power of $-70$ dBm, the minimum sensitivity requirement for BLE. The transfer function shown corresponds to the first channel of Bluetooth Low Energy at 2.402 GHz. Measurements report a maximum gain of 55.5 dB (with an in-band gain variation less than 1 dB) and a minimum image rejection of 30.5 dB across the 2 MHz channel bandwidth. The gain is sub-divided in 25 dB and 30 dB from the RF front end and complex filter, respectively. This measurement is representative of the worst case measure in terms of maximum gain and image rejection.

Fig. 10(c) and (d) shows gain, image rejection, noise figure and IIP3 measurements for all the BLE channels. The gain varies less than 1 dB across the channels demonstrating that the LNA bandwidth is wide enough to operate in the entire ISM band. Image rejection ranges between 30.5 dB and 37.3 dB across all channels (well above the required 21 dB demanded by the BLE standard), achieved without any calibration. The noise figure varies between 15.1 dB and 15.8 dB, which correspond to an equivalent receiver front-end sensitivity of $-84.2$ dBm. The IIP3 was measured through a two-tone intermodulation test, placing blockers in the adjacent channels at 5 MHz and 8 MHz to produce an in-band tone. Notice that the IIP3 remains relatively constant over the entire Bluetooth Low Energy spectrum with less than 2 dB variation. At maximum gain the receiver has an IIP3 higher than $-17$ dBm. The measured phase noise of the receiver is $-109$ dBc/Hz at 2.5 MHz carrier offset, meeting the requirements of BLE with considerable margin (see Fig. 11). Since no test point has been added at the output of the VCO, the phase noise measure has been realized by down-converting the LO at the output of the TIA and thus, above 2 MHz, the measure is affected by the noise produced by the cell.

For the first time in literature, the susceptibility of the LMV cell to injection pulling by nearby blockers has been measured. The pulling has been measured in two different conditions: by

TABLE II
CHIP SUMMARY AND COMPARISON WITH STATE OF THE ART

| | [2] | [4] | [5] | [8] | [12] | [17] | This work |
|---|---|---|---|---|---|---|---|
| **Power Consumption [mW]** | 1.1*** | 1.8 | 3.6 | 2.7 | 0.55 | 1.6 | 0.6 |
| **RF Input Freq [MHz]** | 2400 | 2400 | 2400 | 2400 | 2600 | 2400 | 2400 |
| **Voltage Gain [dB] (min/max)** | - | 57.8 | 75 | 55 | 41 | 83 | 55.5/56.1 |
| **NF [dB] (min/max)** | 16*/16.6* | 15.7 | 9 | 9 | 9.6 | 6.1 | 15.1/15.8 |
| **IIP3 [dBm] (min/max)** | -2.9** | -18.5** | -12.5 | -6 | -30 | -21.5 | -15.8/-16.8 |
| **IR [dB] (min/max)** | - | 37/40 | 35 | 28 | - | - | 30.5/37.3 |
| **PN [dBc/Hz] @ 2.5MHz** | - 118.1 | -142 | -121 | -112 | - | -142 | -109 |
| **Supply Voltage [V]** | 1 | 1 | 1.2 | 0.6/1.2 | 0.85 | 0.3 | 0.8 |
| **Technology** | 130nm | 65nm | 90nm | 65nm | 65nm | 65nm | 130nm |
| **Active Area [mm$^2$]** | - | 0.45 | 0.35 | 0.26 | 0.15 | - | 0.25 |

* Baseband filter not included in measurement
** Measured at moderate or minimum gain
*** Includes power consumption of PLL

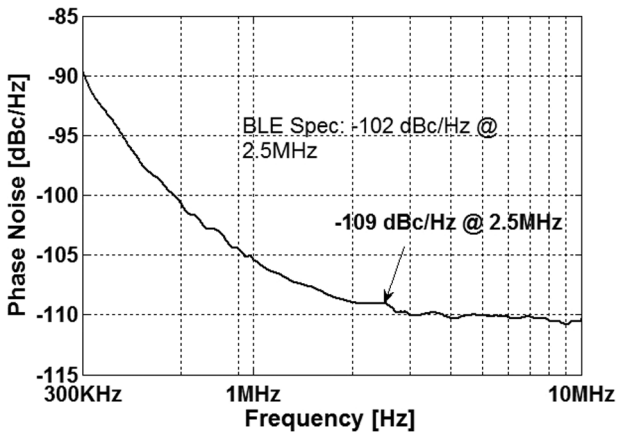


Fig. 11. Chip phase noise measurement.

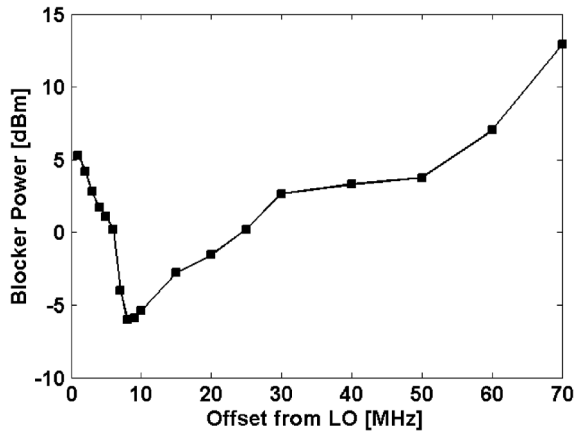


Fig. 12. Injection pulling susceptibility due to nearby interferer by blocker power.

injecting a blocker around twice of the oscillation frequency (i.e., 2 $\omega_{LO}$) or by injecting a large interfer close to the carrier $\omega_{LO}$. The former case is important because the LMV cell operates as an injection locking frequency divider and is very sensitive to signal entering at the double of the oscillation frequency [5]. However, thanks to the presence of the narrow-band input matching network, the pulling in such condition occurs only for input signals larger than $-2.5$ dBm.

In the second test, the sensitivity of the cell changes significantly upon the position of the interferer as shown in Fig. 12 where the power required to lock the oscillator is plotted vs. the frequency offset with the respect to the oscillation frequency $f_{LO}$. At a frequency offset of 1 MHz, the oscillator can be locked only with an input power of 5 dBm (well above the saturation point of the receiver chain at maximum gain). This can been explained considering that a signal close to the oscillation frequency would appear at the VCO as a tone near DC, that has been significantly attenuated by the narrow-band Q of the tank. Increasing the frequency offset, the locking power decreases since the down-converted tone moves toward the resonance of the tank. However measurements show that beyond 10 MHz the power required to pull the oscillator increases again. While for very large frequency offsets, the power increment is explained by the presence of filtering produced by the narrow-band matching network, the reduced sensitivity to the pulling only after 10 MHz could not be explained. The problem is that, when the input power is above $-5$ dBm, the LMV cell and the TIAs are operating in an abnormal state, making the analysis of the problem very difficult. The measurement in Fig. 12 demonstrated a good immunity of the proposed design to pulling effects since it is not possible to have such large value of input signal power feeding directly the LMV cell. In fact when in-band signals reach such value of power, an attenuator is typically used in front of the RF front-end to prevent the system saturation [2].

A summary of receiver performance is reported in Table II along with a comparison to the state of the art. Although

in literature several examples of low power receiver front-ends are present, [15]–[20], for an easier comparison only Bluetooth and ZigBee receivers demonstrating similar sensitivity or comparable power consumption have been included. This is because, as previously explained, performance and power consumption cannot be scaled easily together. Compared to the solutions present in literature with similar performances, [2] and [4], the proposed design consumes only a fraction of the power. The other designs reported in the table have better noise figures but also report much higher power consumption. Although in this case a fair comparison is difficult to make, it can be verified that the power consumption required to generate the local oscillator in [5], [8], [17] is either higher or comparable to the power consumption of the entire receiver front-end proposed in this paper. Therefore, even if the performances of the other receiver chains were significantly compromised in favour of a lower consumption (by scaling the power consumption of LNA, mixers, and base-band section), it would be difficult to achieve an overall power consumption below the one reported here since the power necessary for LO generation cannot be arbitrary scaled.

## V. Conclusions

A current-reuse receiver front end for WSN applications consuming only 0.6 mW of power and operating under a low 0.8 V supply has been presented. Its ultra-low power consumption was achieved through the use of the LMV cell. Despite using a 130 nm technology node, the proposed current re-use design has demonstrated the lowest power consumption, occupies one of the smallest areas, and is compliant with BLE noise figure, linearity, phase noise and image rejection specifications.

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