A current re-use PA-VCO cell for low-power BLE transmitters

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***Abstract*—A current re-use PA-VCO cell for FSK transmitters is presented. High efficiency and low phase noise are obtained through the stacking of a PA and a class-C VCO. Without the use of any DC-DC converters, the voltage headroom of these two blocks can be set maximizing the efficiency of both the PA and the VCO. The structure is inserted in a 130nm CMOS BLE transmitter. A TX efficiency of 17.5% is achieved delivering an output power of -1dBm at 2.4GHz with a VCO phase noise of -129dBc/Hz @ 2.5MHz frequency offset.**

Keywords—BLE, TX, current-reuse, PA, VCO, high efficiency

I. INTRODUCTION

Bluetooth Low Energy (BLE) is an ultra-low power operative mode tailored to shot-range communication such as body area networks, in-door location, and contactless payments. In these applications, the maximum delivered power can be significantly reduced (e.g. below 0dBm) in favor of a long-lasting battery life. When the power amplifier (PA) operates in such conditions, the design of a high-efficient transmitter becomes very challenging since the overhead due to the power burned by the other building blocks constitutes the real bottleneck for the entire system. In addition to that, since the efficiency of the PA itself is maximized when operating at the maximum output voltage swing, a small output power requires large load impedance that becomes more sensitive to parasitic elements. This problem can be overcome adopting a lower voltage supply for the PA with the cost of an extra DC-DC converter.

The transmitter presented in this paper tries to solve the above issues by adopting the current re-use architecture drawn in Fig. 1 where the PA is merged with a class-C voltage-controlled-oscillator (VCO). When the power consumption required by the VCO is comparable to the one burned by the PA (like in some BLE applications), the proposed solution offers three main advantages. First, the regular voltage supply can be subdivided between the two blocks without the use of extra DC-DC converters. Second, the PA can deliver efficiently the targeted output power driving a smaller load, being less sensitive to parasitic elements. Third, the VCO can operate at half of the output carrier frequency exploiting an intrinsic property of the class-C oscillator that works as a frequency doubler when the output signal is sensed in the center tap of the inductor.

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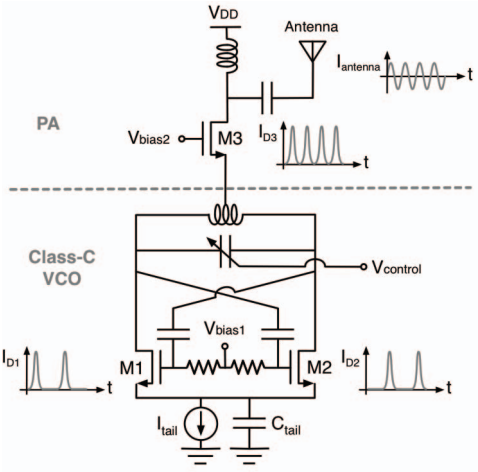

Fig. 1. Class-C VCO and PA stacking

The proposed solution is inserted in a fractional phase-locked-loop (PLL) used for channel selection, while the transmission occurs in open loop by applying the GFSK modulation directly at the input of the VCO [1]. The paper is structured as following: Section I is focused on the merged VCO and PA structure, Section II describes in detail the transmitter implementation, and Section III includes the measurement results on a 130nm CMOS prototype.

II. MERGING PA AND CLASS-C VCO

The proposed solution is based on oscillator topology proposed by Mazzanti and Andreani, where the cross-coupled pair operates in class-C to maximize the amplitude of the current injected into the tank at the oscillation frequency [2]. As in the original design, the class-C operation of the VCO in Fig. 1 relies on two key elements: a capacitance C_{tail} in parallel to the current source biasing the VCO and a proper bias scheme to keep transistors M1-M2 in saturation region during the conduction phase [3].

A. Class-C VCO as a frequency multplier

In a class-C oscillator, as the one drawn in the lower section of Fig. 1, the cross-coupled pair generates a train of pulses that is injected into the tank. While in general the output

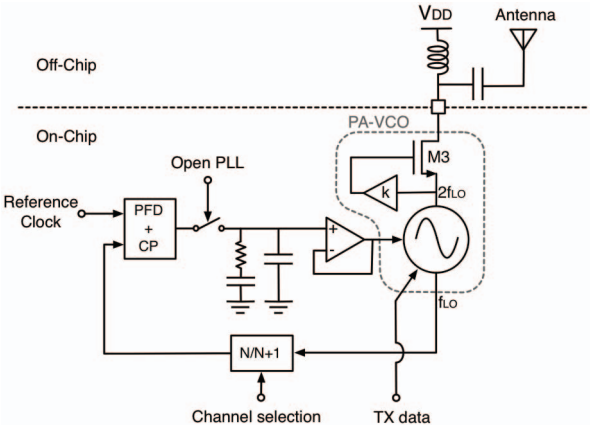

Fig. 2. Transmitter architecture

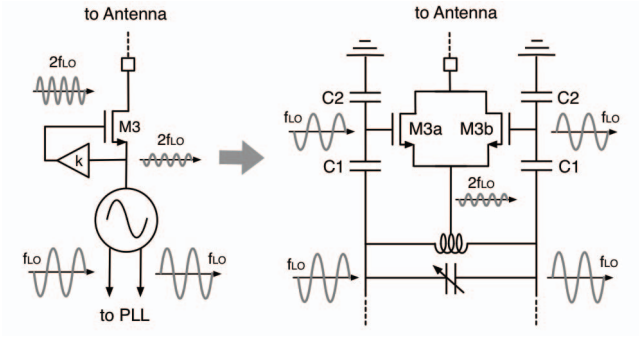

Fig. 3. Boosted common-gate PA (bias not shown)

signal is sensed as a voltage across the tank, in this case it is collected as a current flowing out from the center tap of the inductor. In this way, it is possible to exploit an intrinsic property of the class-C oscillator that works as a frequency doubler. As shown in Fig. 1, the center tap of the inductor collects both the current injected by M1 and M2 providing a train of pulses with a frequency doubled with respect to the fundamental one (f_{LO}) sensed across the tank.

The sensing of the signal at the center tap of the inductor leads to several advantages: the oscillator can operate at half of the carrier frequency, it is possible to perform a differential to single-end conversion, the bias current can be re-used for the PA, and no buffers are required to drive the PA, which does not load directly the tank.

B. Stacking PA and VCO

As shown in Fig. 1, the power amplifier is added by using a common-gate stage that will intrinsically operate in class-C since fed by a train of narrow pulses. A resonant LC network at the output of the PA is used to provide a DC path, filter higher harmonics and scale the impedance of the antenna (in order to maximize the efficiency for a given output power).

The impact of the PA on the class-C VCO can be studied by using the small-signal time-variant approach proposed by Mazzanti and Andreani [2]. In this analysis, the M3 transconductance $g_m(\omega_{LO}t)$ can be described by the following Fourier series

$$g_m(\omega_{LO}t) = \sum_p g_p \cos(p\omega_{LO}t) \qquad (1)$$

where $\omega_{LO}=2\pi f_{LO}$ and the coefficients g_p are determined by both the large-signal regime and the MOS device parameters [2]. For the signal at the second harmonic of the oscillation frequency (i.e. p=2), the input impedance provided by the PA in Fig. 1 is equal to $1/g_2$ and appears in series to capacitor C_{tail}, since the current generator I_{tail} behaves as an open circuit. It is possible to demonstrate that, in order to maintain a class-C operation, g_2 must respect the following condition

$$g_2 > 2\omega_{LO}C_{tail} \qquad (2)$$

With a simple common-gate stage as the one shown in Fig. 1, the satisfaction of (2) can become challenging when the PA transmits a low output power, since g_2 tends to be small. To increase the value of g_2, a boosted common-gate stage will be introduced in Section III.

The second element in the design of the VCO-PA stack is the division of the available voltage supply (V_{DD}) between two blocks. In this operation, the main trade-off is between the minimum voltage required by the VCO ($V_{DD,VCO}$) and the overall efficiency of the transmitter. In particular, for a given efficiency of the PA (η_{PA}), the overall efficiency of the stack is given by:

$$\eta_{STACK} = \eta_{PA}\left(1 - \frac{V_{DD,VCO}}{V_{DD}}\right) \qquad (3)$$

From (3) it is clear that when the voltage headroom reserved for the VCO is reduced, the overall efficiency grows. This property fits very well with class-C VCO that has its maximum efficiency with lower voltage supply compared to other topologies. When the VCO and PA have comparable power consumption, $V_{DD,VCO}$ can be set equal to $V_{DD}/2$ and the TX efficiency cannot exceed 50%. However since the power consumption dissipated by the PA is generally higher than the one required by the VCO, $V_{DD,VCO}$ should be set lower than $V_{DD}/2$. The voltage headroom reserved for the VCO can be easily set by acting on the DC bias at the gate of M3 (Fig. 1) offering a degree of freedom in the power optimization without requiring any additional DC-DC converter.

III. BLE TRANSMITTER

The proposed PA-VCO stack has been used in the design of a transmitter for a BLE beacon. The TX architecture is shown in Fig. 2. The PA-VCO stack is inserted in an analog PLL used for channel selection while the transmission occurs in open loop by modulating the VCO [1]. Since the oscillator works in open loop, its phase noise affects the TX output spectrum and the frequency drift of the carrier, limiting the length of data-packet. As it will be shown in the measurements section, the proposed solution allows to have a very low phase noise without compromising the TX efficiency.

A. Boosted Common-Gate PA

As shown in the previous section, in order to maintain an efficient class-C operation, the transconductance g_2 of the common-gate PA must be relatively large. Since an active amplification of the signal at $2f_{LO}$ presenting at the source of M3 would have compromised the overall efficiency of the stack, the scheme drawn in Fig. 3 was used. The key idea is to

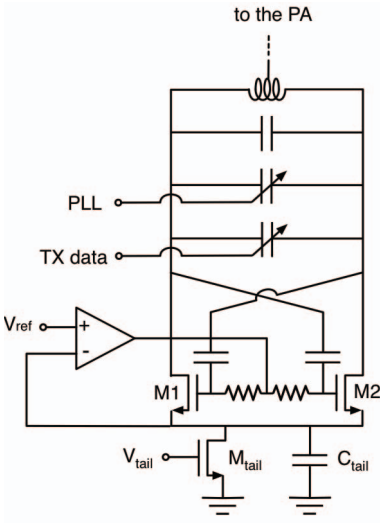

Fig. 4. Boosted common gate PA (bias not shown)

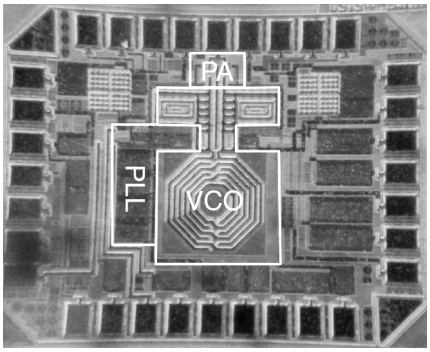

Fig. 5. Transmitter Die-Photo

split the PA in two parts, each of them driven at the gate with one of the two phases of the voltage signal developed across the tank at f_{LO}. In order to keep the transistors M3a and M3b in saturation, a capacitive divider is used to scale properly the oscillator amplitude. The solution drawn in Fig. 3 is very efficient and allows to extract the second harmonic of the circuit without additional power consumption. In the realized prototype, the attenuation provided by the capacitive divider can be tuned with 3-bit resolution in order to adjust the amplitude at the gates when the bias current is swept to deliver different output powers.

B. Class-C biasing and VCO tank

The class-C VCO has been biased by adopting the scheme proposed by Fanori and Andreani drawn in Fig. 4 [3]. This solution maximizes the oscillation amplitude without compromising the robustness of the oscillator start-up. An operational amplifier is used to set the dc value of the drain of the current mirror keeping constant the current consumption in both start-up and steady state.

The tank of the VCO consists in a capacitor bank and two varactors assuring a tuning range around 20%. The larger varactor is connected to the fractional-PLL for channel selection and the smaller one is used to provide open-loop

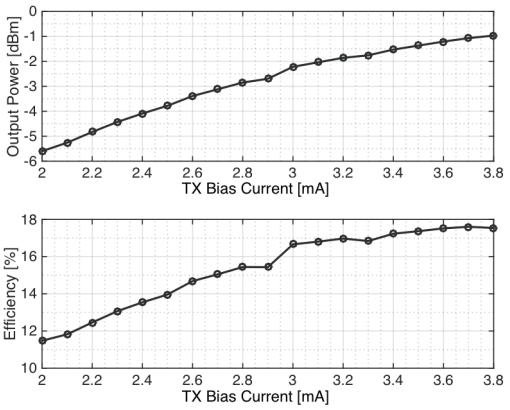

Fig. 6. Power delivered and efficiency vs. TX bias current

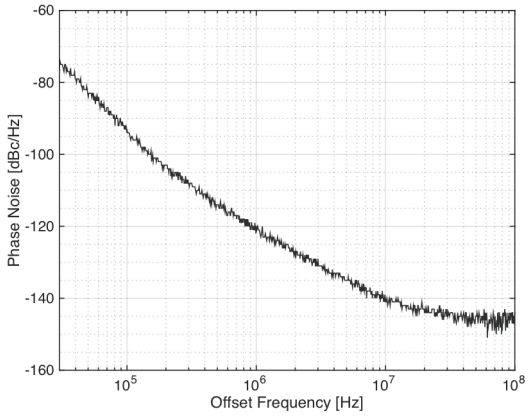

Fig. 7. Phase noise of free running VCO at the 2.45GHz

modulation. The modulated signal is generated on board for the flexibility in the testing measurements.

IV. MEASUREMENTS

The TX prototype, tailored to a BLE beacon for indoor location, has been realized in IBM 130nm CMOS technology. The die photo is reported in Fig.5. The proposed solution occupies an active area of 0.35mm^2 dominated by the inductor used for the VCO. The inductor, with a third terminal at the center tap to sense the second harmonic current, has a nominal value of 6.9nH with a quality factor of 15 at 1.2GHz. The voltage supply for the entire chip was set to 1.2V while the $V_{DD,VCO}$ is set to 500mV in order to give more room to the PA for larger output power.

The output power and the efficiency versus the TX bias current are plotted in Fig. 6. Notice that during transmission the PLL is powered off and the only additional source of power consumption beside the PA-VCO stacks are the two operational amplifiers that draw 100μA in total. The peak efficiency of the transmitter is equal to 17.5% and remains above 11% in the entire current sweep range. From (3) it is possible to estimate the power efficiency of the PA, which in the case of the maximum output power is around 30%. In the plot in Fig. 6, when the bias current is increased above 3mA, the capacitive divider is adjusted in order to keep M3a and

TABLE I. MEASUREMENTS RESULTS AND STATE OF THE ART

	This work	[4]	[5]	[6]	[7]	[1]	[8]	[9]
Max. Transmitted Power	**-1dBm**	+4dBm	-3dBm	+5dBm	-1dBm	+1.9dBm	+1.6dBm	+10.9dBm
Peak Efficiency (@ output power)	**17.5% (@-1dBm)**	9.1% (@0dBm)	9.8% (@-3dBm)	10.5% (@0dBm)	14.7% (@-1dBm)	17.4% (@+1.9dBm)	24.5% (@+1.6dBm)	43.7% (@+10.9dBm)
Modulation Type	**GFSK**	GFSK	GFSK	GFSK	GFSK	GFSK	GFSK	GFSK
Data rate	**1Mb/s**	1Mb/s	1Mb/s	1Mb/s	1Mb/s	1Mb/s	1Mb/s	1Mb/s
Phase Noise @2.5MHz	**-129dBc/Hz**	-	-116dBc/Hz*	-125dBc/Hz	-119dBc/Hz*	-118.5dBc/Hz	-117dBc/Hz	-
Technology	**130nm CMOS**	90nm CMOS	65nm CMOS	65nm CMOS	90nm CMOS	130nm CMOS	130nm CMOS	65nm CMOS
Power dissipation	**4.56mW**	11mW	5.1mW	9.5mW	5.4mW	8.9mW	5.9mW	28.2mW
Supply Voltage	**1.2V**	1.2V	1.1V	1.3V	1.2V	1.0V	1.0V	-
Chip Area	**0.35mm^2****	1.95mm^2	7.84mm^2	0.35mm^2*	3.61mm^2	1.54mm^2	2.1mm^2	1.6mm^2

* Phase noise @2.5MHz was normalized from that at 1MHz
** Core area

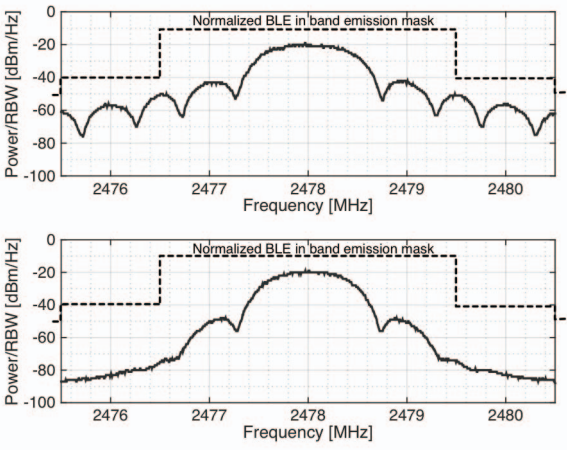

Fig. 8. Transmitted PSP with FSK and GFSK modulation index of 0.5 and a data rate of 1Mb/s. (Span 5MHz, 10kHz resolution bandwidth)

M3b in saturation allowing larger output amplitude. The scalability of the output power is limited by the matching network design in order to have its peak amplitude close to 0dBm.

The free running VCO phase noise is almost constant in entire ISM band; a plot at 2.45GHz is reported in Fig. 7. The measurement was obtained biasing the PA-VCO stack with 2mA while delivering an output power of -5.1dBm. The phase noise achieved at 2.5MHz offset is equal to -129dBc/Hz leading to an oscillator FoM of 189 dBc/Hz. The performances of the structure with modulated signal have been evaluated for both FSK and GFSK signal with a modulation index equal to 0.5 (Fig. 8). In both cases the emission mask is widely respected also due to the low power transmitted.

The overall performances of the transmitter with the state of the art of FSK TX at 2.4GHz are reported in Table I. A comparison between the different solutions proposed in literature is difficult due to the fact that several TX maximize their efficiency for an output power much higher than 0dBm (e.g. [9]) (being less affected by the power consumption drawn by the oscillator and the other building blocks). However, among the design with a sub-mW output power (i.e. [4-7]) the proposed design shows the best efficiency although an older technology was used. In addition, the phase noise performance is outstanding, being as much as 10dB lower than solutions with similar or lower efficiency.

V. CONCLUSIONS

A current re-use PA-VCO topology, targeted for low power FSK transmitter has been presented. Inserted in a TX for BLE applications, it has shown high efficiency and best in class phase-noise performances, particular important in FSK transmitter when open-loop modulations are adopted.

REFERENCES

[1] J. Masuch and M. Delgado-Restituto, "A Sub-10 nJ/b 1.9-dBm Output Power FSK Transmitter for Body Area Network Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 5, pp. 1413–1423, Apr. 2012.

[2] A. Mazzanti and P. Andreani, "Class-C Harmonic CMOS VCOs, With a General Result on Phase Noise," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[3] L. Fanori and P. Andreani, "Low-phase-noise 3.4-4.5 GHz dynamic-bias class-C CMOS VCOs with a FoM of 191 dBc/Hz," Proceeding of ESSCIRC 2012, pp. 406–409, Sept. 2011.

[4] F. Pengg, et al. "A low power miniaturized 1.95mm^2 fully integrated transceiver with fastPLL mode for IEEE 802.15.4/bluetooth smart and proprietary 2.4GHz applications," *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE*, pp.71, 74, 2-4 June 2013

[5] G. Devita, et al. "A 5mW multi-standard Bluetooth LE/IEEE 802.15.6 SoC for WBAN applications," *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014 - 40th*, pp.283, 286, 22-26 Sept. 2014

[6] S. Chakraborty, et al.,"A 1.9nJ/bit, 5Mbps multi-standard ISM band wireless transmitter using fully digital PLL," *Radio Frequency Integrated Circuits Symposium (RFIC), 2013 IEEE*, pp.75, 78, 2-4 June 2013

[7] Liu Yao-Hong, et al., "A 2.7nJ/b multi-standard 2.3/2.4GHz polar transmitter for wireless sensor networks," *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pp.448, 450, 19-23 Feb. 2012

[8] J. Masuch, M. Delgado-Restituto, "A 1.1-mW-RX -81.4dBm Sensitivity CMOS Transceiver for Bluetooth Low Energy," *IEEE Transactions on Microwave Theory and Techniques,* , vol.61, no.4, pp.1660, 1673, April 2013

[9] A. Paidimarri, et al., "13.7 A +10dBm 2.4GHz transmitter with sub-400pW leakage and 43.7% system efficiency," *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International*, pp.1,3, 22-26 Feb. 2013