A Simplified Model for Passive-Switched-Capacitor Filters With Complex Poles

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***Abstract*—This brief demonstrates a method to realize complex conjugate poles using passive-switched-capacitor networks. In addition, a simplified continuous-time model will be introduced so that accurate transfer functions and output noise can be obtained without the need for complicated charge-balance equations and thereby allow a better intuitive understanding of these structures. The developed theory is demonstrated through the design of a second-order low-pass Butterworth biquad with applications intended in the design of wireless RF receivers.**

***Index Terms*—Antialiasing integration sampler, biquad, discrete time (DT) infinite-impulse response (IIR) filter, passive switched capacitor (PSC), switched-capacitor model.**

I. Introduction

PASSIVE switched capacitor (PSC) circuits are a particular subset of switched-capacitor circuits that do not rely on active elements to transfer charge between capacitors. The elimination of the active elements allows one to increase the maximum operating frequency up to the settling time required by the passive charge sharing paths (i.e., limited by the resistance of the switches) as well as reducing power consumption due to active elements [1].

While implementations of PSC circuits were realized in 1978 [2], recently, there has been renewed interest in applying PSC circuits for wireless receiver applications as both an antialiasing integration sampler [3] and a discrete time (DT) infinite-impulse response (IIR) filter within a superheterodyne receiver [4]. The schematics of these two recent filters are shown in Fig. 1. The antialiasing filter [see Fig. 1(a)] is realized by a g_m-C integrator in parallel with a sampling capacitor C_S, and this results in first-order IIR low-pass characteristics with a built-in antialiasing filter. The single real pole of the DT IIR filter in Fig. 1(a) is realized by the sampling capacitor C_S, which takes some of the charge from the integrating capacitor C_{I1} in each cycle and then dumps it to the ground, creating a resistive load [3]. A two-real-pole biquad version can be implemented by connecting C_S to a second integrating capacitor C_{I2} before resetting it to ground [see Fig. 1(b)] [1]. Since both V_1 and $\mathrm{V}_{\mathrm{out}}$ nodes are loaded with C_S, this filter forms two real poles. A clever way to further increase the order of the filter is to add more integrating capacitors and clock phases such that, in each cycle, a single C_S shares sequentially its charge before being reset in the last phase as shown in Fig. 1(c) [4].

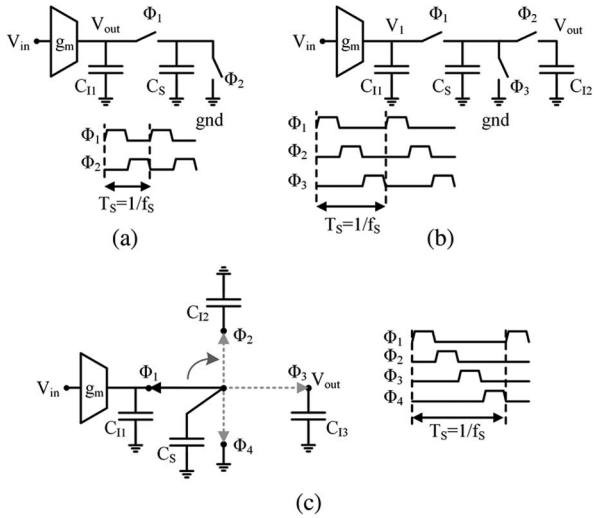

Fig. 1. (a) One-real-pole, (b) two-real-pole, and (c) three-real-pole DT IIR low-pass filters.

The number of integrating capacitors in the filter determines the number of real poles created. Although this approach allows one to implement an arbitrary filter order, only real poles can be realized, preventing the synthesis of sharp filtering profiles such as the ones obtained by using Butterworth and Chebyshev filter responses. Moreover, the analysis of such filters is not intuitive and requires tedious charge-balance equations to obtain the z-domain transfer function.

In this brief, the aforementioned limitations will be addressed by introducing a continuous-time model that will allow one to develop a biquad with complex conjugate poles by offering a simplified analysis of PSC filters. This brief is organized as follows. Section II explains the proposed model. Section III covers the use of the proposed model for noise analysis. In Section IV, a second-order low-pass filter with complex conjugate poles is developed together with noise analysis. Section V briefly covers the effects of parasitic capacitances as well as the nonlinear performance of a typical filter.

II. Switched-Capacitor Continuous-Time Model

A switched-capacitor circuit can be modeled using an equivalent resistance placed between the two nodes that alternatively charges and discharges the capacitor. Assuming a capacitance C_S and a sampling frequency f_S, this equivalent resistance $\mathrm{R}_{\mathrm{eqv}}$ has a value of $1/(f_S \mathrm{C}_S)$. However, when the charge of the capacitor is shared between more than two nodes, this approach cannot be used anymore. For example, in the DT filter shown in Fig. 1(b), the charge of the capacitor C_S is shared among three nodes in three phases. Two nodes are connected to C_{I1} and C_{I2} that act as integrators, and the third node is ground. For this two-real-pole biquad, the charging and discharging of C_S involve

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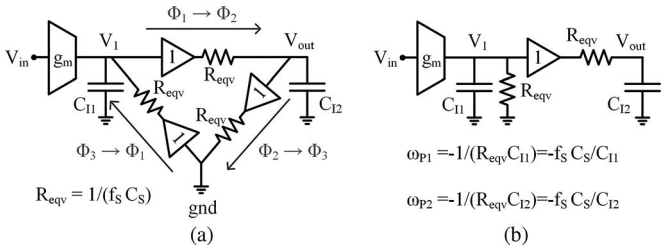

Fig. 2. (a) Proposed continuous-time model for the two-real-pole DT biquad and (b) simplified version of the proposed model.

alternatively two nodes in two consecutive phases, while the third node is alternatively excluded. This circuit arrangement creates a charge flow with a nonreciprocal behavior that cannot be modeled using a resistive network which is, by nature, a reciprocal network with bilateral elements [5]. To solve this issue, a new approach is proposed where each charge/discharge flow is modeled with the traditional $\mathrm{R_{eqv}}$ in series with an ideal voltage buffer which forms a nonreciprocal network.

The proposed model can be used to replace a switching element when, in each phase, the capacitor is connected to an impedance much lower than its capacitance. This condition assures that the memory of the capacitance is reset in each phase, making it behave as a resistor. Furthermore, since, in each phase, the voltage across the capacitor is set by the driving node (having a much lower impedance), the unilateral charge flow modeled by the buffer is guaranteed.

The proposed model has been applied to the circuit in Fig. 1(b), obtaining the continuous-time structure drawn in Fig. 2(a). The equivalent circuit in Fig. 2(a) can be further simplified due to the presence of a ground connection in the loop. This leads to the final scheme drawn as in Fig. 2(b), where the two real poles created by the circuit are highlighted. The proposed model not only highlights the loop present in the charge flow but also allows to find easily the second-order low-pass response of the structure and its poles $(1/(\mathrm{C}_{I1}\mathrm{R_{eqv}})$ and $1/(\mathrm{C}_{I2}\mathrm{R_{eqv}}))$.

The accuracy of the proposed model can be verified by comparison with the poles obtained by analyzing the circuit in the z-domain as done in [1]. This analysis, more complicated and less intuitive, leads to the following results:

$$\frac{\mathrm{V_{out}}(z)}{Q_{\mathrm{in}}(z)} = \frac{1}{\mathrm{C}_S}\left[\frac{z(1-\alpha_1)}{(z-\alpha_1)}\right]\left[\frac{z(1-\alpha_2)}{(z-\alpha_2)}\right] \text{ where}$$

$$Q_{\mathrm{in}}[n] = \int_{(n-1)T_S}^{nT_S} \mathrm{V_{in}}(t) g_m dt \tag{1}$$

where DT poles α_1 and α_2 are equal to $\mathrm{C}_{I1}/(\mathrm{C}_{I1}+\mathrm{C}_S)$ and $\mathrm{C}_{I2}/(\mathrm{C}_{I2}+\mathrm{C}_S)$, respectively. The equivalent continuous-time poles ω_{P1} and ω_{P2} can be approximated using bilinear transformation as follows:

$$\omega_{P1,2} = 2f_S\frac{(\alpha_{1,2}-1)}{(\alpha_{1,2}+1)} = -f_S\frac{\mathrm{C}_S}{\mathrm{C}_{I1,2}+\mathrm{C}_S/2} \approx -f_S\frac{\mathrm{C}_S}{\mathrm{C}_{I1,2}}. \tag{2}$$

The calculated continuous-time poles for the DT filter converge to the proposed model for $\mathrm{C}_{I1,I2} \gg \mathrm{C}_S/2$. This assumption is generally satisfied since it corresponds to a filter cutoff frequency much smaller than the sampling frequency.

The proposed model, when applied to a two-phase switched-capacitor circuit [as the one shown in Fig. 3(a)], converges to the conventional $\mathrm{R_{eqv}}$ representation. In this case, the use

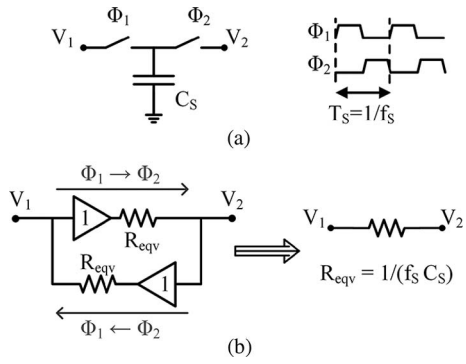

Fig. 3. (a) Basic two-phase switched-capacitor element and its timing characteristics. (b)Proposed continuous-time model.

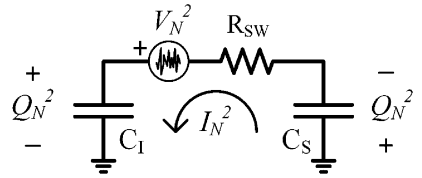

Fig. 4. Correlated noise charge stored in two capacitors with opposite polarities.

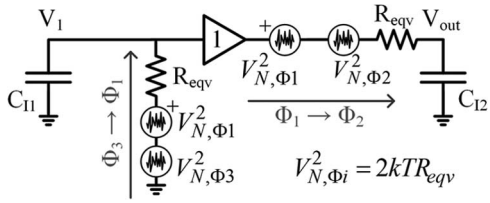

Fig. 5. Second-order real-pole filter proposed model with noise sources, where the two Φ_1 noise sources are fully correlated with inverse polarity.

of the proposed model involves two buffers and two resistors connected back to back, representing two charge/discharge flows [see Fig. 3(b)]. The loop can be further simplified into a simple resistor $\mathrm{R_{eqv}}$.

III. Noise Analysis Using Continuous-Time Model

The model introduced in the previous section can also be used to analyze noise without the need of complex DT charge-balance analyses as the one used in [1]. The noise introduced in each charge/discharge flow is equal to the noise associated with equivalent resistance $\mathrm{R_{eqv}}$ (i.e., $4\mathrm{kTR_{eqv}}$). However, since, in each charge/discharge flow, two switches are involved, this noise must be divided into two uncorrelated noise sources with a power spectral density equal to $2\mathrm{kTR_{eqv}}$. Furthermore, noise created by the same switch in two consecutive charge/discharge flows must be represented by two correlated noise sources with inverse polarity. This can be explained by considering that the noise injected by a switch resistance, which connects two capacitors, is stored with opposite polarity in the two capacitors (e.g., Fig. 4).

The circuit in Fig. 2(b) includes two resistors: one associated with the charge/discharge flow $\Phi_1 \rightarrow \Phi_2$ and one associated with the charge/discharge flow $\Phi_3 \rightarrow \Phi_1$. From the previous assumption, the noise analysis can be performed by considering the model shown in Fig. 5. Note that the noise associated with the Φ_1 switch occurs in both of the transitions and the two Φ_1 noise sources are fully correlated with inverse polarity. From

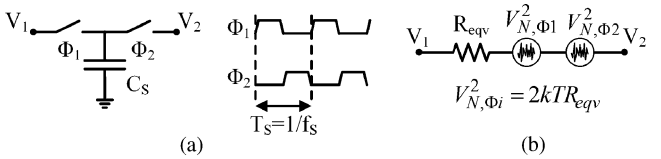

Fig. 6. (a) Two-phase switched-capacitor element and (b) proposed continuous-time model with noise sources.

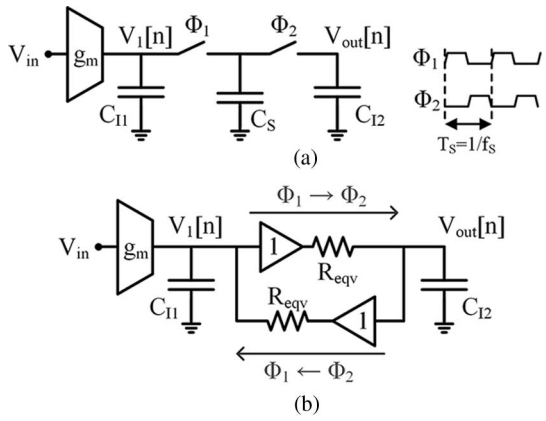

Fig. 7. (a) DT real-pole filter and its timing characteristics. (b) Proposed continuous-time model.

the circuit in Fig. 5, the output noise spectral density can be easily evaluated as:

$$V^2_{N,\text{out}} = 2\text{kTR}_{\text{eqv}}\left[\left|\overbrace{\frac{1}{(1+j\omega \text{R}_{\text{eqv}}\text{C}_{I1})(1+j\omega \text{R}_{\text{eqv}}\text{C}_{I2})} - \frac{1}{1+j\omega \text{R}_{\text{eqv}}\text{C}_{I2}}}^{\Phi_1}\right|^2 + \overbrace{\frac{1}{|1+j\omega \text{R}_{\text{eqv}}\text{C}_{I2}|^2}}^{\Phi_2} + \overbrace{\frac{1}{|1+j\omega \text{R}_{\text{eqv}}\text{C}_{I1}|^2|1+j\omega \text{R}_{\text{eqv}}\text{C}_{I2}|^2}}^{\Phi_3}\right] \quad (3)$$

It can be shown that, when R_{eqv} is replaced by $1/(f_S\text{C}_S)$, the output noise spectral density obtained using the model is approximately equal to the value calculated using DT noise analysis [1].

The proposed noise model can be applied to a two-phase switched-capacitor circuit [as in Fig. 6(a)]. In this case, the model involves two uncorrelated noise sources, each having 2kTR_{eqv} noise spectral density [see Fig. 6(b)]. If R_{eqv} is replaced by $1/(f_S\text{C}_S)$, the integrated noise power over $0 - f_S/2$ bandwidth leads to the known 2kT/C_S.

IV. Second-Order Butterworth Passive DT Biquad

It is well known that passive RC networks can only form real poles [5]. Similarly, the creation of complex conjugate poles in switch capacitor circuits generally involves the use of active components to create a feedback loop able to move the real poles in the complex plane. In this section, it will be shown that such feedback loop can be created with a PSC network by exploiting the unilaterality highlighted by the proposed model.

A. From Real to Passive Complex-Pole Filter

In Fig. 7(a), a switched-capacitor low-pass filter with two real poles is reported. Although, in this case, the two switches and capacitor C_S could be substituted by a simple resistor, the model proposed in the previous section has been used to highlight the presence of a virtual loop [see Fig. 7(b)].

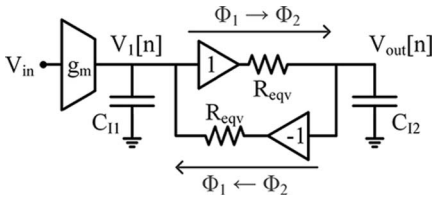

Fig. 8. Complex-conjugate-pole filter involving a negative feedback loop.

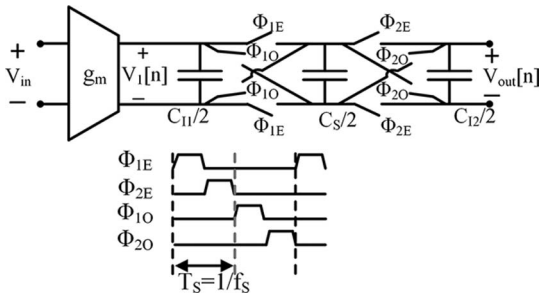

Fig. 9. (a) Differential second-order complex-conjugate-pole DT filter.

It is possible to demonstrate that the real poles of the circuit in Fig. 7(b) can be transformed into complex conjugate ones just by inverting the gain of the buffer in the return path (see Fig. 8). This inversion creates a nonreciprocal network, which makes it possible to obtain complex conjugate poles using passive components. These new poles have a natural oscillation frequency ω_0 and a quality factor Q given by

$$\omega_0 = \frac{\sqrt{2}}{\text{R}_{\text{eqv}}\sqrt{\text{C}_{I1}\text{C}_{I2}}} \text{ and } Q = \frac{\sqrt{2\text{C}_{I1}\text{C}_{I2}}}{\text{C}_{I1}+\text{C}_{I2}} \le \frac{1}{\sqrt{2}}. \quad (4)$$

When Q becomes greater than 0.5 (choosing a $\text{C}_{I1}/\text{C}_{I2}$ ratio in between 0.17 and 5.83), the poles become complex conjugate. When $\text{C}_{I1} = \text{C}_{I2}$, Q reaches its maximum value of $1/\sqrt{2}$ that corresponds to a second-order Butterworth transfer function. The reason for an upper bound in the Q achievable relies on the loop gain that cannot exceed 1 since only passive components are involved.

B. Implementation of the Passive Complex-Conjugate-Pole Filter

The easiest way to create the inverting buffer is to use a differential structure where the charge of the sampling capacitor (C_S) is cross-transferred between positive and negative terminals. This operation is realized by the circuit shown in Fig. 9 based on four phases, two of which are labeled even (Φ_{1E} and Φ_{2E}) and two of which are labeled odd (Φ_{1O} and Φ_{2O}). During the even phase, the circuit behaves like Fig. 7(a), while during the odd phases, charge inversion is obtained. The output is sampled on both Φ_{2E} and Φ_{2O}. In this way, the circuit behaves as a two-phase system from the output perspective. This topology is similar to the one obtained in [6], where, however, two sampling capacitors C_S are required.

By applying the proposed model, the second-order complex-conjugate-pole biquad given in Fig. 9 can be transformed into a continuous-time topology. Considering the four phases, a continuous-time model can be built by using buffer + R_{eqv} branches corresponding to each phase change $(\phi_{1O} \to \phi_{2O},\ \phi_{2O} \to \phi_{1E},\ \phi_{1E} \to \phi_{2E}, \phi_{2E} \to \phi_{1O})$ as shown in Fig. 10(a). $\text{R}_{\text{eqv}} = 1/(f_S\text{C}_S)$, where f_S is defined for two phases, since output is sampled at every two phases. This model can be simplified by merging parallel branches [see Fig. 10(b)]. Moreover, cross-coupled buffer branches can be

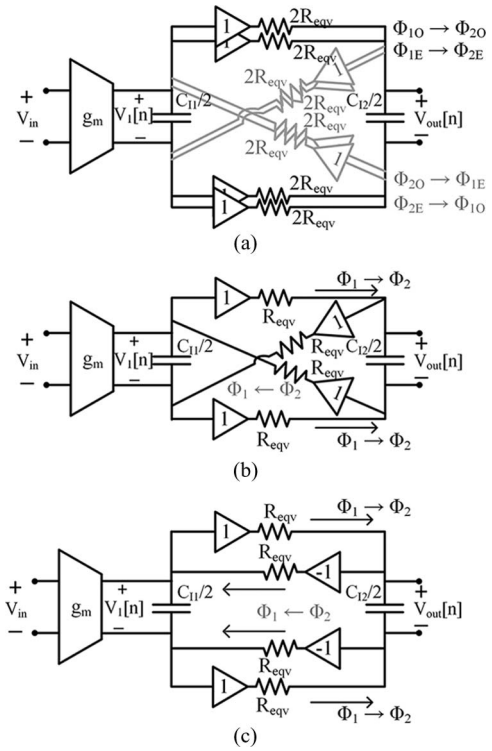

Fig. 10. Differential second-order complex-conjugate-pole biquad continuous-time model. (a) Direct representation of four phases. (b) With parallel branches merged. (c) Cross-coupled buffers are replaced by inverter branches.

replaced with inverter branches since the circuit is differential to obtain Fig. 10(c), which is the fully differential version of the circuit reported in Fig. 8.

The pole locations of the differential second-order complex-pole DT filter can be found by first deriving the filter transfer function in the z-domain and later obtaining the s-domain denominator of the filter transfer function by using bilinear transformation. The details of the derivation are given in the Appendix, which results in the following s-domain ω_0:

$$\omega_0 = \frac{2f_S C_S}{\sqrt{C_{I1}C_S + C_{I2}C_S + 2C_{I1}C_{I2}}} \approx \frac{\sqrt{2}}{R_{eqv}\sqrt{C_{I1}C_{I2}}} \quad (5)$$

with Q given by

$$Q = \frac{\sqrt{C_{I1}C_S + C_{I2}C_S + 2C_{I1}C_{I2}}}{C_{I1} + C_{I2} + C_S} \approx \frac{\sqrt{2C_{I1}C_{I2}}}{C_{I1} + C_{I2}} \leq \frac{1}{\sqrt{2}}. \quad (6)$$

The calculated s-domain ω_0 and Q of the DT filter become the same as the values derived by the proposed model, (4), under the same assumption introduced in Section II for the real-pole filter (i.e., $C_{I1,I2} \gg C_S/2$).

C. Filter Transfer Function Simulations

The second-order Butterworth DT biquad, the two-real-pole biquad [see Fig. 1(b)], and their continuous-time models were simulated in 65-nm CMOS technology by using Spectre Periodic Steady State Analysis-Periodic AC Analysis (PSS-PAC). MOSFET transmission gates were used as switches with on resistance R_{SW} of 1 kΩ and off parasitic capacitance C_{PRS} of 1.8 fF. A sampling frequency of 160 MHz was chosen for a filter passband of 1 MHz.

The simulated magnitude transfer function with $C_{I1} = C_{I2} = 3.56$ pF and $C_S = 400$ fF for the real-pole filter and that with $C_{I1} = C_{I2} = 5.14$ pF and $C_S = 200$ fF for the

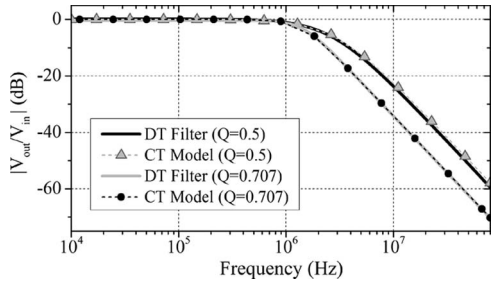

Fig. 11. Simulated magnitude response for -1-dB droop at 1 MHz with $fs = 160$ MHz of the two-real-pole and second-order Butterworth biquads.

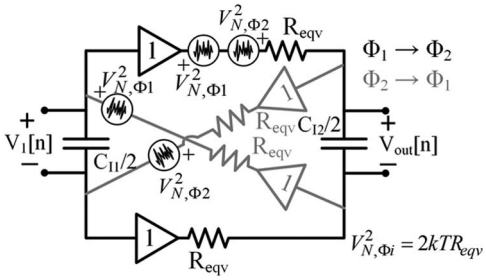

Fig. 12. Second-order complex-conjugate-pole filter proposed model with noise sources, where noise sources associated with the same switch are fully correlated with inverse polarity.

Butterworth filter are reported in Fig. 11. For both of the filters, g_m is set to 32 μS. The small discrepancy between the proposed model and the switched-capacitor implementation is due to the parasitic capacitances of the transmission gates, which shift the expected pole frequencies and also the dc gain $(g_m/(f_S C_S))$ of the filters. Note that the Butterworth filter provides more than 10-dB suppression for frequencies above 7 MHz compared to the real-pole filter.

D. Second-Order Butterworth Biquad Noise Analysis

The noise analysis of the second-order Butterworth biquad was performed by using the model in Fig. 12, developed as described in Section IV-B. Two of the four resistors presented in the model are associated with the charge/discharge flow $\Phi_1 \rightarrow \Phi_2$, and the other two resistors are associated with the charge/discharge flow $\Phi_2 \rightarrow \Phi_1$. Due to the differential nature of the filter, it is sufficient to investigate the noise associated with one of the Φ_1 switches and one of the Φ_2 switches.

In Fig. 12, the noise sources due to the Φ_1 switch are placed in two branches that are connected to the $V_1[n]$ positive terminal. Note that the two Φ_1 noise sources are fully correlated with inverse polarity. Similarly, the noise sources due to the Φ_2 switch are placed in two branches that are connected to the $V_{out}[n]$ positive terminal. Note that the two Φ_2 noise sources are fully correlated with inverse polarity. Using Fig. 12, the noise analysis is straightforward, and the output noise spectral density can be written as

$$V^2_{N,out} = 2\times 2kTR_{eqv}\left[\left|\frac{\overbrace{j\omega R_{eqv}C_{I1}}^{\Phi_1}}{2-\omega^2 R^2_{eqv}C_{I1}C_{I2}+j\omega R_{eqv}(C_{I1}+C_{I2})}\right|^2 + \left|\frac{\overbrace{2+j\omega R_{eqv}C_{I1}}^{\Phi_2}}{2-\omega^2 R^2_{eqv}C_{I1}C_{I2}+j\omega R_{eqv}(C_{I1}+C_{I2})}\right|^2\right]. \quad (7)$$

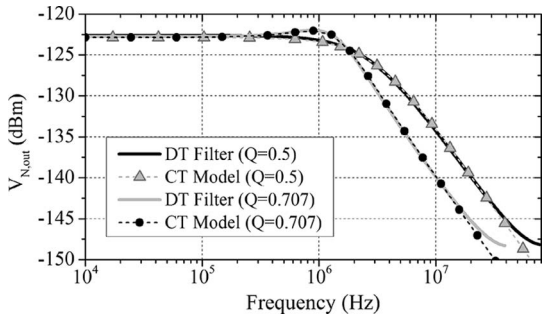

Fig. 13. Simulated output noise spectral density of the two-real-pole and second-order Butterworth biquads for −1-dB droop at 1 MHz.

A coefficient 2 is added in order to include the effect of the differential switches' noise. It can be shown that, when $\mathrm{R_{eqv}}$ is replaced by $1/(f_S \mathrm{C}_S)$, the output noise spectral density obtained using the continuous-time model is approximately equal to the value calculated using DT noise analysis.

The simulated output noise spectral densities are shown in Fig. 13 with both the two-real-pole biquad and the second-order Butterworth DT biquad sized the same as in the previous part. For both the real-pole and Butterworth biquads, simulated noise spectral densities in the passband are approximately equal, and the values are in accordance with the calculated results.

V. Effect of Parasitic Capacitances

The switches and capacitors (C_I and C_S) introduce parasitic capacitances $\mathrm{C_{PRS}}$ to the circuit. The top- and bottom-plate parasitic capacitances of each capacitor are added on itself. $\mathrm{C_{PRS}}$ associated with switches, on the other hand, are added both on C_I and C_S.

For both of the filters, any $\mathrm{C_{PRS}}$ that was added only on C_I shifts the desired pole locations. For the Butterworth filter, as long as C_{I1} and C_{I2} values change similarly, the Q value is not affected by the added $\mathrm{C_{PRS}}$ (6), whereas the $\mathrm{C_{PRS}}$ of the switches added on C_S limits the minimum value of C_S. Choosing smaller size switches results in lower $\mathrm{C_{PRS}}$. However, switch size is also determined by the required switch resistance $\mathrm{R_{SW}}$, where $\mathrm{R_{SW}}$ is limited by the settling error. For a lower settling error, $\mathrm{R_{SW}}$ should be low, which requires larger switches. This creates a tradeoff between the settling error and minimum capacitance value. Moreover, the $\mathrm{C_{PRS}}$ of the switches changes with the signal level and introduces nonlinearity for larger signal amplitudes.

To investigate the nonlinear performance of the second-order Butterworth filter compared to a two-real-pole biquad, both filters (sized the same as in Section IV-C) were simulated using Spectre PSS-PAC with two tones at 10 and 19 MHz. The intermodulation tone was placed close to the filter cutoff. Switch capacitances were the main source of nonlinearity since ideal g_m-cells were used. The out-of-band third-order input intercept point (IIP3) of the second-order Butterworth was simulated at 29 dBm, which compares favorably with the out-of-band IIP3 of the two-real-pole biquad that was simulated at 13 dBm.

VI. Conclusion

In this brief, a simplified model is proposed for PSC filters where the sampling parts of the network are replaced with continuous-time equivalents consisting of resistors and ideal buffers. This continuous-time model results in easy and intuitive analysis compared to the conventional charge-balance equations and leads to accurate transfer function and noise analysis. Moreover, through the use of this model, a PSC filter with complex conjugate poles is realized, which results in a sharper filter profile compared to its real-pole counterparts.

Appendix

This appendix derives the pole locations of the second-order complex-conjugate-pole biquad drawn in Fig. 9 by solving the following system of charge-balance equations derived for two phases:

$$\begin{cases} Q_{\mathrm{in}}[n]+\mathrm{C}_{I1}\mathrm{V}_1[n-1]-\mathrm{C}_s\mathrm{V}_{\mathrm{out}}[n-1]=(\mathrm{C}_{I1}+\mathrm{C}_S)\mathrm{V}_1[n] \\ \mathrm{C}_S\mathrm{V}_1[n]+\mathrm{C}_{I2}\mathrm{V}_{\mathrm{out}}[n-1]=(\mathrm{C}_{I2}+\mathrm{C}_S)\mathrm{V}_{\mathrm{out}}[n] \end{cases}$$

$$\text{with } Q_{\mathrm{in}}[n] = \int_{(n-1)T_S}^{nT_S} \mathrm{V}_{\mathrm{in}}(t) g_m dt \quad (8)$$

where n represents any sampling period with ϕ_1 and ϕ_2 and $n-1$ represents the preceding sampling period. The resulting transfer function in the z-domain is given by

$$\frac{\mathrm{V}_{\mathrm{out}}(z)}{Q_{\mathrm{in}}(z)} = \frac{z^2\left(\frac{\mathrm{C}_S}{(\mathrm{C}_S+\mathrm{C}_{I1})(\mathrm{C}_S+\mathrm{C}_{I2})}\right)}{z^2 - z\left[\frac{\mathrm{C}_{I1}(\mathrm{C}_S+\mathrm{C}_{I2})+\mathrm{C}_{I2}(\mathrm{C}_S+\mathrm{C}_{I1})-\mathrm{C}_S^2}{(\mathrm{C}_S+\mathrm{C}_{I1})(\mathrm{C}_S+\mathrm{C}_{I2})}\right] + \frac{\mathrm{C}_{I1}\mathrm{C}_{I2}}{(\mathrm{C}_S+\mathrm{C}_{I1})(\mathrm{C}_S+\mathrm{C}_{I2})}}. \quad (9)$$

Later, to determine the ω_0 and Q of the DT filter, bilinear transformation $z=(1+\mathrm{s}/2\ \mathrm{fs})/(1-\mathrm{s}/2\ \mathrm{fs})$ can be used, obtaining

$$\omega_0 = \frac{2f_S\mathrm{C}_S}{\sqrt{\mathrm{C}_{I1}\mathrm{C}_S+\mathrm{C}_{I2}\mathrm{C}_S+2\mathrm{C}_{I1}\mathrm{C}_{I2}}}$$
$$Q = \frac{\sqrt{\mathrm{C}_{I1}\mathrm{C}_S+\mathrm{C}_{I2}\mathrm{C}_S+2\mathrm{C}_{I1}\mathrm{C}_{I2}}}{\mathrm{C}_{I1}+\mathrm{C}_{I2}+\mathrm{C}_S}. \quad (10)$$

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