Class-C PA-VCO Cell for FSK and GFSK Transmitters

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***Abstract*— In this paper, a Class-C PA-VCO cell tailored to FSK/GFSK transmitters is presented. In the proposed solution, a Class-C VCO and a common-gate stage PA are stacked in a current-reuse architecture operating with 1.2 V power supply. The PA and the VCO efficiencies are maximized by adjusting their voltage headroom without the use of any DC–DC converters. The PA-VCO is inserted in a transmitter based on an open-loop architecture. The presented prototype, fabricated in 0.13 μm CMOS technology, occupies an active area of 0.2 mm^2. A maximum TX efficiency of 17.5% is achieved while the TX is delivering an output power of −1 dBm at 2.45 GHz. A phase noise of −129 dBc/Hz at 2.5 MHz frequency offset results in a carrier-frequency drift below 7 Hz/s and an FSK error below 0.7%, which allows the transmitter to operate in open-loop while delivering long data-packets. The transmitter is also compliant to BLE specifications when FSK and GFSK modulations with index of 0.5 are applied.**

***Index Terms*— Class-C, current-reuse, FSK, GFSK, high efficiency, low phase noise, low-power, open-loop transmitter, PA, VCO.**

I. Introduction

IN THE ERA of the Internet of Things (IoT), ultra-low power wireless transceivers will play an indispensable role in the creation of energy harvested wireless sensor networks (WSNs) [1]. Bluetooth Low Energy (BLE) and ZigBee are the most popular standards for ultra-low power applications [1]–[3]. In such systems, the transmitter represents the most power hungry section of the transceiver and the main bottleneck in the design of a battery-less device. Frequency shift keying (FSK) and Gaussian FSK (GFSK) are the main modulations adopted by ultra-low power transceivers since for modest data rate they can lead to high efficiency and a simplification of the radio architecture. In particular, the transmitter can be realized with a phase-locked loop (PLL) followed by a nonlinear power amplifier (PA) [4].

In ultra-low power applications, performance and transmitted power are sacrificed in favor of a longer-lasting battery life [3]. When the PA operates in such low-power conditions ($P_{RF} < 0$ dBm), the overall efficiency is affected by power consumption of the other building blocks (e.g., the PLL). In particular, the overall efficiency of the TX (η_{TX}) can be expressed as

$$\eta_{TX} = \frac{P_{RF}}{P_{DC,PA} + P_{DC,MOD}} \tag{1}$$

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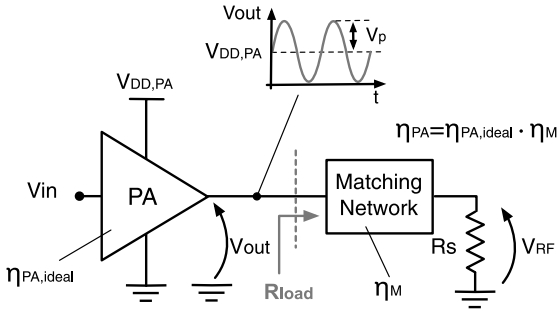

Fig. 1. TX output load and matching network.

where P_{RF} is RF power delivered by the TX, $P_{DC,PA}$ is power dissipated by the PA, and $P_{DC,MOD}$ is the power consumption of the TX excluding the PA. Equation (1) can be rewritten as a function of the PA efficiency (η_{PA}) as

$$\eta_{TX} = \frac{\eta_{PA}}{1 + \eta_{PA} \cdot \frac{P_{DC,MOD}}{P_{RF}}}. \tag{2}$$

From (2), it is possible to verify that, for low output power levels, the overall TX efficiency drops, since $P_{DC,MOD}$ does not typically scale with P_{RF}. Usually, the lower bound for $P_{DC,MOD}$ is set by the voltage-controlled oscillator (VCO), which is the second most power-hungry block after the PA. The delivery of a small output power also sets a constraint in the design of the PA and its output matching network. In fact, since the maximum efficiency of a PA is typically reached when the amplifier operates rail-to-rail, a small output power demands a large resistive load at the output of the PA, becoming more sensitive to parasitic elements and decreasing the overall efficiency [5] (Fig. 1). For a given PA voltage supply $V_{DD,PA}$ and output power P_{RF}, the required load to maximize the η_{PA} is given by

$$R_{load} = \frac{1}{2} \cdot \frac{V_p^2}{P_{RF}} = \frac{1}{2} \cdot \frac{V_{DD,PA}^2}{P_{RF}} \tag{3}$$

where the signal swing at the output (V_p) is assumed equal to $V_{DD,PA}$. As shown in [5], the efficiency of a simple matching network (i.e., with only one inductor) used to transform the impedance of the antenna R_s into R_{load} (with $R_{load} > R_s$) is given by

$$\eta_M \approx 1 - \frac{\sqrt{\frac{R_{load}}{Rs} - 1}}{Q_L} = 1 - \frac{\sqrt{\frac{V_{DD,PA}^2}{V_{RF}^2} - 1}}{Q_L} \tag{4}$$

where V_{RF} corresponds to the voltage amplitude of the delivered power P_{RF} at the antenna and Q_L the quality factor of the inductor (quality factor of the capacitors is neglected since it is typically greater than Q_L). To give an idea of the

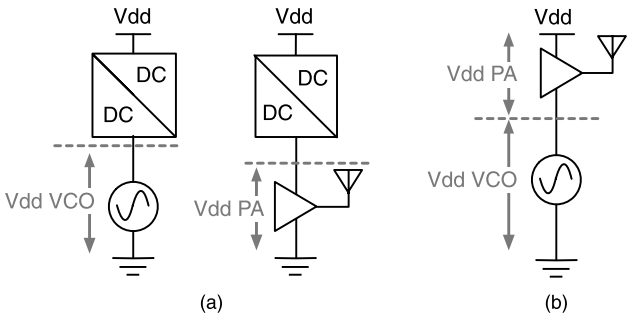

Fig. 2. (a) Supplying the VCO and the PA using DC–DC converters and (b) current-reuse stacking structure.

relevance of this problem at low transmitted power, if V_{RF} is 0.3 V (roughly 0 dBm of power) adopting a power supply of 1.2 V and an inductor with $Q_L = 10 - 15$, the η_M would be between 61% and 74%. In the case of small output power, the impact of parasitic elements can be limited by adopting a multistage matching network [5] (demanding larger area) or a lower voltage supply to the PA, with the cost of an extra DC–DC converter [Fig. 2(a)] [6], [7]. Taking this effect into account, (2) can be rewritten as

$$\eta_{TX} = \frac{\eta_{PA,ideal} \cdot \eta_M}{1 + \eta_{PA,ideal} \cdot \eta_M \cdot \frac{P_{DC,MOD}}{P_{RF}}} \quad (5)$$

where $\eta_{PA,ideal}$ corresponds to the efficiency of the PA by assuming an ideal matching network.

The work presented in this paper tries to solve the above issues by applying the current-reuse architecture as shown in Fig. 2(b), where the PA is stacked on top of a Class-C VCO [8]. When the power burned by the PA is of the same order as the one dissipated by the VCO, the proposed design offers four main advantages. First, a single V_{DD} can be subdivided between the VCO and the PA without any DC–DC converters. Second, the targeted low output power can be delivered by the PA with a smaller load, which is less sensitive to parasitic elements and makes the design of the matching network easier. Third, the supply voltage ratio between the VCO and the PA can be adjusted, offering a degree of freedom for power optimization for different targeted output powers and phase noise (PN) specs. Finally, the Class-C VCO can operates at half of the carrier frequency, exploiting an intrinsic property of the Class-C VCO that can be used as a frequency doubler, if the output signal is sensed at the center tap of the inductor in the *LC*-tank. For testing purposes, the proposed PA-VCO cell is inserted in a fractional PLL for channel selection. Although, in the proposed prototype, the transmission occurs in open-loop by directly modulating the VCO (thanks to the low carrier-frequency drift and FSK error achieved), the structure is also fully compatible with closed-loop direct modulators.

This paper is organized as follows. Section II is focused on the details of the Class-C VCO and the stacking structure. Section III describes in detail the boosted common-gate topology adopted for the PA. Section IV offers a design methodology to dimension the PA-VCO structure for a targeted output power and the PN, and Section V shows the details of a prototype implemented in 0.13 μm CMOS technology. Finally, measurement results are discussed in Section VI.

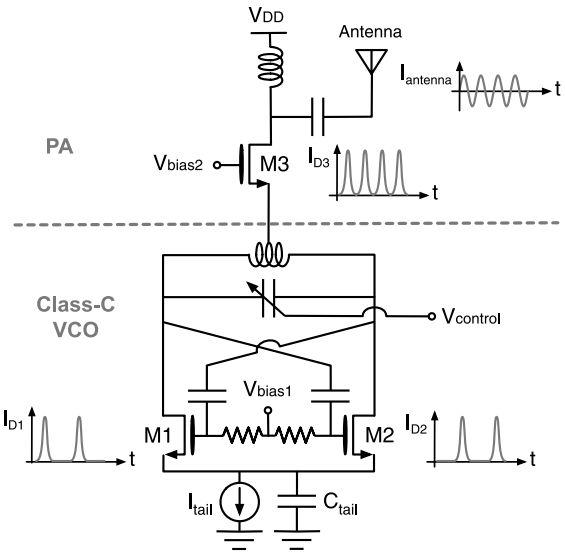

Fig. 3. Class-C VCO and PA stacking.

II. Stacking Class-C VCO and PA

The Class-C VCO is an oscillator topology originally proposed by [9], where the cross-coupled pair in the VCO operates in Class-C in order to maximize the amplitude of the current injected into the *LC*-tank at the oscillation frequency. According to the original design proposed by [9], two key elements are required to maintain the VCO in Class-C operation: a capacitor C_{tail} in parallel with the VCO's biasing current source I_{tail}, and a proper bias scheme to keep the cross-coupled pair M1-M2 in the saturation region during the conducting phase (Fig. 3) [9], [10].

A. Class-C VCO as a Frequency Doubler

In a Class-C oscillator topology, each transistor of the cross-coupled pair (M1-M2) generates a train of pulses that feeds an *LC* tank (used to amplify the differential component at f_{LO} by sustaining the oscillation). If the tank resonates only for differential components, as in the case shown in Fig. 3, common-mode signals are collected at the center tap of the inductor. The two trains of pulses collected at the center tap of the inductor form a train of pulses at $2 \cdot f_{LO}$, making the Class-C oscillator a frequency doubler. By feeding the pulse train to a common-gate PA as shown in Fig. 3, a complete transmitter front-end can be realized. In this structure, the oscillator operates at half of the carrier frequency of the transmitted signals, saving power in frequency generation and the dividers. Furthermore, a differential to single-end conversion is intrinsically performed simplifying the interface between the PA and the antenna. In addition to that, the VCO bias current is reused by the PA and no buffers are required to drive the PA avoiding loading the *LC* tank.

In WSN transceiver, the RX and the TX typically share the same VCO. This could be a problem for the proposed structure where the VCO operates at half of the carrier frequency. A possible solution is proposed in [11], where a receiver is

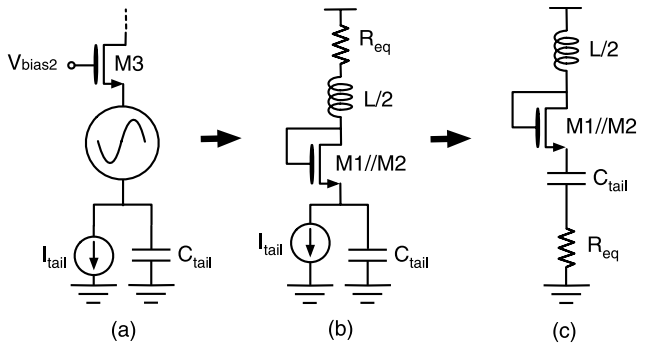

Fig. 4. PA-VCO stack equivalent circuits at $2 \cdot \omega_{\mathrm{LO}}$. , (a) PA-VCO stack. (b) Common-mode equivalent impedance R_{eq} at $2 \cdot \omega_{\mathrm{LO}}$. (c) Transformation of R_{eq}.

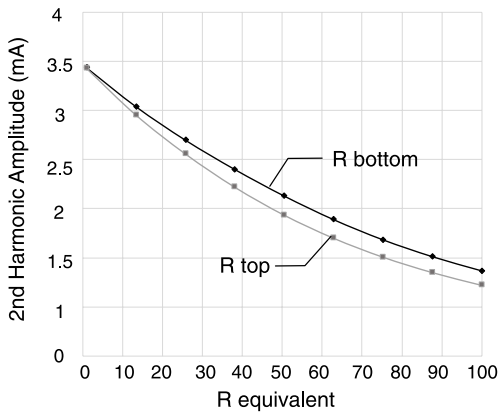

Fig. 5. Effects of having R_{eq} at the top and bottom of the stack.

realized by using a VCO also operating at half of the carrier frequency exploiting injection-locking properties.

B. Stacking the PA and the VCO

The common-gate stage M3 in Fig. 3 intrinsically operates in Class-C since it is fed by a train of narrow pulses. A resonant *LC* matching network is applied at the output of the M3 to provide a DC path to filter out higher order harmonics and to maximize the efficiency for a targeted output power, by scaling the impedance of the antenna.

Stacking of the PA with the Class-C VCO is less trivial than it appears since a high input impedance provided by the PA tends to compromise the Class-C operation of the VCO. The study of this phenomenon is complex since the PA operates in Class-C and a simple time-invariant linear model cannot be used. However, the same approach used in [9] to study the Class-C oscillator was adopted. According to [9], the time-variant transconductance of M3 can be described by the following Fourier series:

$$g_m(\omega_{\mathrm{LO}}t) = \sum_{\mathrm{p}} g_{\mathrm{p}} \cdot \cos(p \cdot \omega_{\mathrm{LO}}t) \tag{6}$$

where $\omega_{\mathrm{LO}} = 2\pi \cdot \mathrm{f_{LO}}$ and the coefficient $\mathrm{g_p}$ in the Fourier series can be determined by the large-signal regime and the MOSFET device parameters [9]. Notice that g_{p} are different from the coefficients of the classic Taylor expansion around a DC bias point. For example, g_0 is the transistor transconductance averaged in an oscillation period that would resemble the small-signal transconductance g_m in a time-invariant situation. Since the PA works as a common-gate stage, its input resistance at $2 \cdot \mathrm{f_{LO}}$ can be found by solving the following equation for the components i_{d} at $2 \cdot \omega_{\mathrm{LO}}$:

$$i_{\mathrm{d}}(t) = g_m(t) \cdot V_x \cdot \cos(2 \cdot \omega_{\mathrm{LO}}t) \tag{7}$$

where $i_{\mathrm{d}}(t)$ is the current absorbed by the transistor in the presence of a sinusoidal voltage source V_x at its input. By substituting $i_{\mathrm{d}}(t) = I_x \cdot \cos(2 \cdot \omega_{\mathrm{LO}}t)$ in (7), the input impedance at $2 \cdot \omega_{\mathrm{LO}}$ can be expressed as

$$R_{\mathrm{eq}} = \frac{V_x}{I_x} = \frac{1}{\left(g_0 + \frac{g_4}{2}\right)}. \tag{8}$$

As shown in Fig. 4, for the signal at $2 \cdot \mathrm{f_{LO}}$, this input impedance appears in series with the capacitor C_{tail} because the current source I_{tail} behaves as an open circuit for such component. Although in general it is wrong to move a resistor from drain to source of a transistor, in this case the transformation is possible because for common-mode components, the transistors M1 and M2 are diode connected [Fig. 4(b)]. The role of the capacitor C_{tail} in a Class-C oscillator is to provide a low-impedance path for the current when both transistors in the switching pair are off. An increment of such R_{eq} reduces the capability of the oscillator to operate in Class-C by decreasing the efficiency of the oscillator and the extraction of the second harmonic as shown by the simulation in Fig. 5. To prove the correctness of the transformation performed in Fig. 4, Fig. 5 shows the effect of having R_{eq} at the top and bottom of the stack. The slight difference between the two curves derives from the presence of parasitic capacitance of the transistors that mitigate the effect of an increment of R_{eq} when it is placed in series to C_{tail}.

In order to keep the VCO in Class-C operation, the input impedance of the PA must be lower than $\mathrm{C_{tail}}$, leading to the following condition:

$$R_{\mathrm{eq}} \ll \frac{1}{2 \cdot \omega_{\mathrm{LO}} \cdot C_{\mathrm{tail}}}. \tag{9}$$

Once condition (9) is satisfied, another critical element for the stack design is the subdivision of the supply voltage (V_{DD}) between the VCO ($V_{\mathrm{DD,VCO}}$) and the PA ($V_{\mathrm{DD,PA}}$). The overall efficiency (η_{STACK}) can be expressed as follows:

$$\eta_{\mathrm{STACK}} = \frac{P_{\mathrm{RF}}}{P_{\mathrm{DC,STACK}}} \tag{10}$$

where $P_{\mathrm{DC,STACK}}$ is the power consumed by the overall stack. Equation (10) can be rewritten as a function of the PA efficiency (η_{PA}) as

$$\eta_{\mathrm{STACK}} = \eta_{\mathrm{PA}} \cdot \frac{V_{\mathrm{DD,PA}}}{V_{\mathrm{DD}}}. \tag{11}$$

For a given η_{PA}, increasing $\mathrm{V_{DD,PA}}$ improves the efficiency of the stack. However, when the losses of the matching network are also considered, (11) can be rewritten as:

$$\begin{aligned}\eta_{\mathrm{STACK}} &= \eta_{\mathrm{PA,ideal}} \cdot \eta_M \frac{V_{\mathrm{DD,PA}}}{V_{\mathrm{DD}}} \\ &= \eta_{\mathrm{PA,ideal}} \cdot \frac{V_{\mathrm{DD,PA}}}{V_{\mathrm{DD}}} \cdot \left(1 - \frac{\sqrt{\frac{\mathrm{V_{DD,PA}^2}}{\mathrm{V_{RF}^2}} - 1}}{\mathrm{Q_L}}\right).\end{aligned} \tag{12}$$

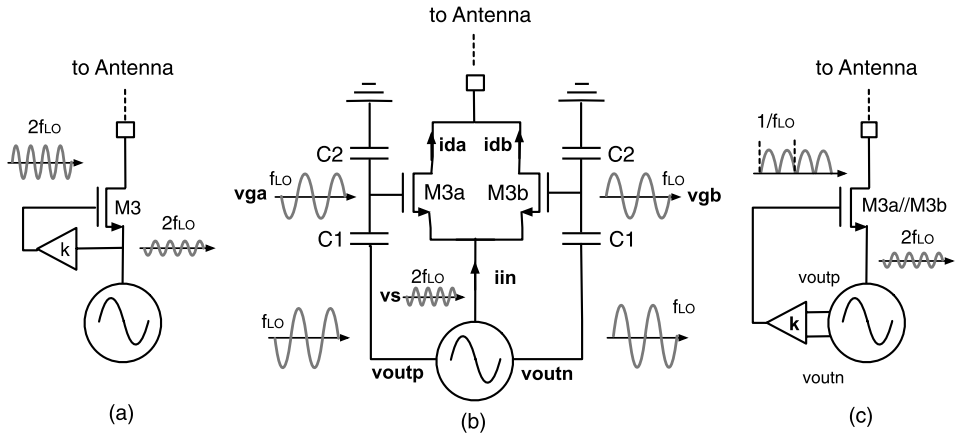

Fig. 6. Boosted common-gate stage: (a) active implementation, (b) proposed solution, and (c) equivalent model.

In this case, it is possible to verify that higher $V_{DD,PA}$ leads to more losses in the matching network, making (12) nonmonotonic. A more intuitive explanation of the behavior of (12) is that, for small $V_{DD,PA}$, the overall efficiency diminishes because the majority of the power is used in the VCO, while for very large $V_{DD,PA}$ the efficiency is limited since some power is dissipated in the matching network. The optimum value of $V_{DD,PA}$ depends on many constraints such as Q_L, V_{DD}, V_{RF}, and the power required by the VCO to satisfy a certain PN spec. The flexible subdivision of the supply voltage between the VCO and the PA offers an additional degree of freedom for the design optimization without the need for any DC–DC converters. In fact, the optimization can be done by simply controlling the DC bias voltage at the gate of transistor M3, which, for low frequency components, operates as a voltage regulator for the VCO.

When a low PN is needed, as targeted in the presented prototype to achieve a small carrier-frequency drift and FSK error, more power must be consumed by the VCO requiring a $V_{DD,VCO}$ larger than $V_{DD,PA}$. Although in this case η_{STACK} is inevitably reduced, the PA can be more efficient since it is less sensitive to the parasitic elements, as shown by (4) and (12). On the other hand, if the PN spec is relaxed, the subdivision of the supply between the VCO and the PA can be optimized as a function of the delivery output power and the overall efficiency of the stack.

III. Boosted Common-Gate PA

As shown in the previous section, a low input impedance of the common-gate PA at the second harmonic of the oscillation frequency is fundamental to maintain the oscillator in Class-C operation. When the transmitted power is in the range of mW, a simple common-gate topology as reported in Fig. 3 is not sufficient to satisfy the condition expressed by (9) since the average transistor transconductance (i.e., g_0) becomes too small. In such cases, the input impedance of the common-gate PA can be further decreased by a boosted topology as shown in Fig. 6(a). The main problem of such an approach is the usage of an additional amplifier that would compromise the overall efficiency. An active stage can be avoided by exploiting the large differential signal produced by the VCO at ω_{LO}. As shown in Fig. 6(b), the amplifier is split into two parts and each gate is driven by one of the phases of the differential LO signals produced by the VCO tank. The presence of a train of pulses feeding the PA makes it difficult to develop an analytical expression for the input impedance of the amplifier, which relies on a time-variant nonlinear operation of the transistors. However, the behavior of the proposed structure can be studied by considering the transformation reported in Fig. 6. Since each transistor works only for half of the oscillation period, the structure in Fig. 6(b) resembles the one reported in Fig. 6(c), where a single transistor is driven by a "rectified" sinusoid at ω_{LO}, which also contains the frequency component at $2 \cdot \omega_{LO}$. This component, correlated to the one at the source of M3, is used to boost the transistor transconductance, lowering the input impedance. In order to guarantee a Class-C operation for the PA, the amplitude at the gate of the M3a and M3b must be limited to keep the transistors in the saturation region when turned on. This requires the introduction of a capacitor divider between the VCO tank and the PA that partially loads the VCO tank. However, since the amplitude required to lower the input impedance can be only a fraction of the one developed across the VCO tank, the capacitive divider can be sized to limit the loading effect introduced by the PA.

Simulations of currents and voltages highlighted in Fig. 6 are reported in Fig. 7. The large signals at ω_{LO} provided at the gate turn the transistors on and off such that the input pulses flow alternatively into M3a and M3b. A plot of the input impedance (for $2 \cdot f_{LO}$ components) as a function of the capacitive divider gain k is reported in Fig. 8. For $k = 0$, the structure behaves as a common-gate stage, while an increment of k decreases the level of the input impedance up to a factor 10. For very large values of k, the input impedance rises again since the transistors start to work partially in triode.

When stacking on the top of the VCO, the boosted common-gate PA resembles a frequency doubler, which exploits the nonlinearity of the transistor to generate a second harmonic of output current. However, in the proposed solution, the output current is not set by the voltage driving the gate of the transistor but by the current feeding the source (Fig. 6). In this case, the stage operates as a boosted cascode where the additional voltage presented at the gate only reduces the swing at the source by lowering the input impedance. To work as a frequency doubler, the PA would require a large capacitor at

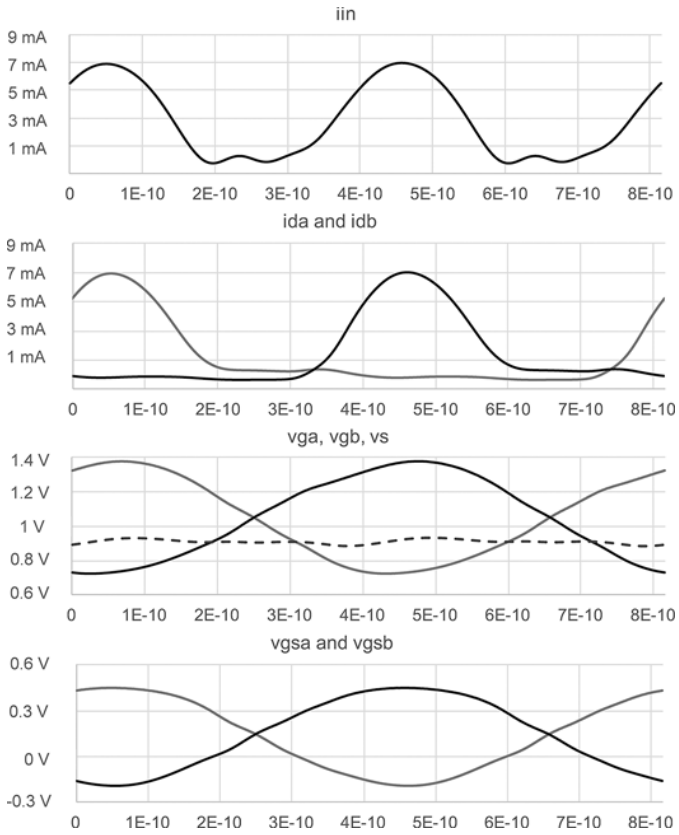

Fig. 7. Simulation results of voltages and currents in the PA.

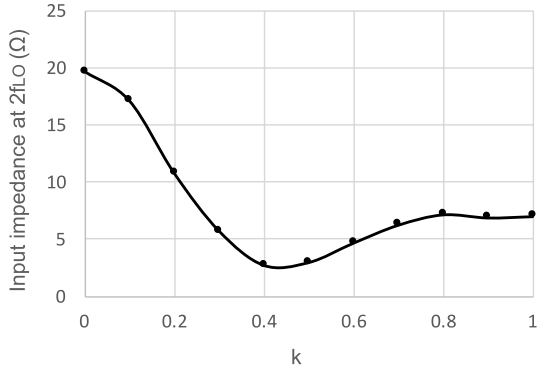

Fig. 8. Input impedance at $2 \cdot f_{LO}$ versus capacitive divider gain k.

its source to act as a common-source stage for the RF signal. The proposed solution, not only avoids the presence of a large decoupling capacitor, but also takes advantage of the fact that a common-gate stage driven by a high impedance introduces less noise and distortion compared to a common-source stage. The reason for this is that the gate and the source tend to follow each other for noise and distortions due to high driving impedance.

IV. Design Methodology

Here, a design methodology to dimension the most important elements in the PA-VCO cell from a given voltage supply, a targeted output power and the PN is demonstrated. Although several strategies can be adopted to obtain an optimized design, this strategy offers a useful start point especially for the design of the PA matching network and the resonant load of the VCO.

In this design methodology, the first step is to set the voltage headroom for the two building blocks. The minimum voltage supply that can be dedicated to the Class-C VCO depends on several elements that can be found in [9] such as start-up constraints, transistor threshold and the PN spec. Once the minimum $V_{DD,VCO}$ is determined, $V_{DD,PA}$ is also obtained. The definition of the voltage headroom for the two building blocks sets an upper bound for the efficiency of the stack defined by (11).

Once $V_{DD,PA}$ is determined, the PA load (R_{load}) that maximizes the efficiency is only a function of the targeted output power P_{RF} and can be found in (3). With R_{load}, the current amplitude at $2 \cdot f_{LO}$ delivered by the PA is also set. By assuming a conversion gain of the Class-C oscillator that is close to one [9], the VCO and the PA bias current (I_{bias}) are determined by $V_{DD,PA}/R_{load}$. Finally, R_{load} also sets the impedance ratio that the matching network has to provide to the antenna (i.e., R_{load}/R_s with R_s typically equal to 50 Ω).

Once the VCO current (I_{bias}) and its voltage headroom ($V_{DD,VCO}$) have been determined, the VCO tank must be designed to maximize the oscillation amplitude at f_{LO}. The maximum peak-to-peak oscillation amplitude allowed for a Class-C VCO not to compromise the PN performance is roughly $1.3 \cdot V_{DD,VCO}$ [12], which leads to a tank resistance at resonance as

$$R_{tank} = \frac{1.3 \cdot V_{DD,VCO}}{2 \cdot I_{bias}}. \quad (13)$$

V. Prototype

The proposed current-reuse PA-VCO stack has been integrated in a fractional PLL to implement an open-loop transmitter tailored to an indoor localization application. The main goals for this prototype were a targeted output power below 0 dBm for the PA, low carrier-frequency drift, and low FSK error. While in a closed-loop architecture, carrier-frequency drift and the FSK error are mainly set by the PN produced in the PLL bandwidth, in an open-loop modulation they are determined only by the VCO. Since, beside the power efficiency, the cost of integration of a single technology node is crucial to allow a high-density of devices in the network, the technology chosen for the integration was 0.13 μm CMOS technology with an ultrathick metal layer. From this point of view, the capability of the VCO to operate at half of the carrier frequency allowed us to limit the power dissipation despite the technology node adopted. The schematic of the integrated prototype is shown in Fig. 9. The PA-VCO stack has been inserted in an analog PLL, which is used for channel selection. An external clock is used as reference and the PLL was designed to achieve a bandwidth of around 1 MHz for a fast settling of the carrier frequency. Once the channel is selected, the PLL is opened and transmission occurs by directly modulating the VCO as proposed in [4]. This prevents the spurs of the PLL from affecting the transmission. A more detailed schematic of the VCO is shown in Fig. 10. The VCO tank is constituted by a fixed capacitor (400 fF), a coarse tuning capacitor bank to compensate process variation (seven elements of 100 fF each), a varactor to close the PLL, and a smaller varactor used for

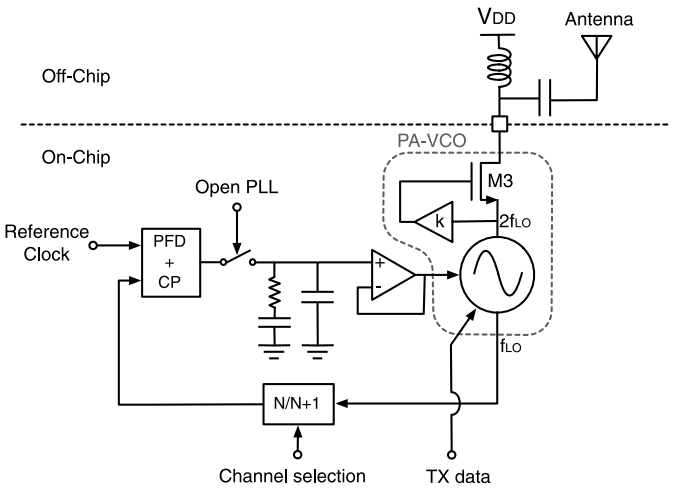

Fig. 9. TX architecture.

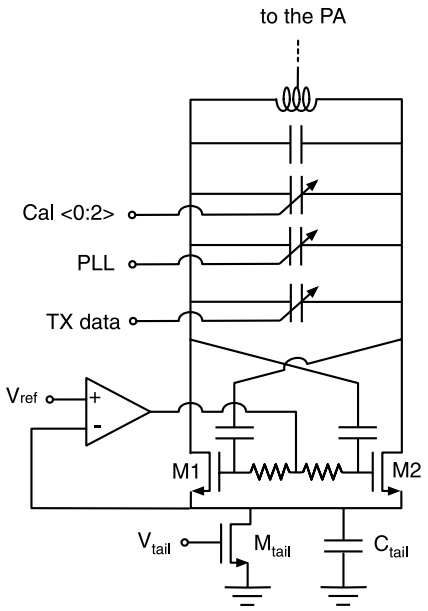

Fig. 10. Class-C VCO and its biasing scheme.

the signal modulation. The varactor used for the modulation is driven by an external operational amplifier, which generates two logic values. This approach, proposed in [4], can shape the pulse in order to mimic a GFSK modulation. The inductor in the VCO LC-tank has a nominal value of 6.9 nH with a simulated quality factor of 15 at half of the carrier frequency (i.e., 1.2 GHz). Each of the VCO cross-coupled transistors has a size of 50 μm/0.12 μm and the tail current source M_{tail} has a size of 600 μm/0.6 μm. The tail capacitor used to maintain Class-C operation C_{tail} has a value of 5 pF.

The PA was implemented as shown in Fig. 6(b). Each of the transistors in the boosted common-gate stage (M3a and M3b in Fig. 6(b)) has a size of 400 μm/0.18 μm. To allow full characterization for a wide range of bias current, the capacitive divider was implemented with 3-bit resolution to adjust the amplitude of the LO signals at the gate of M3a/M3b upon the bias current magnitude. The divider attenuation can be programmed between 2/3 and 1. This flexibility unfortunately cost a degradation of the overall quality factor of the tank when the divider attenuation is 2/3 (i.e., all switches on).

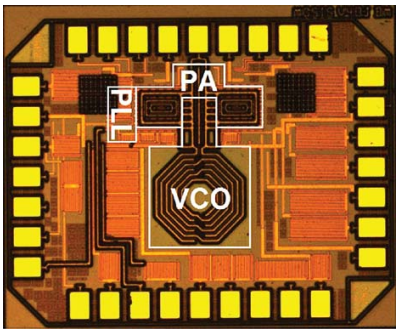

Fig. 11. TX chip micrograph.

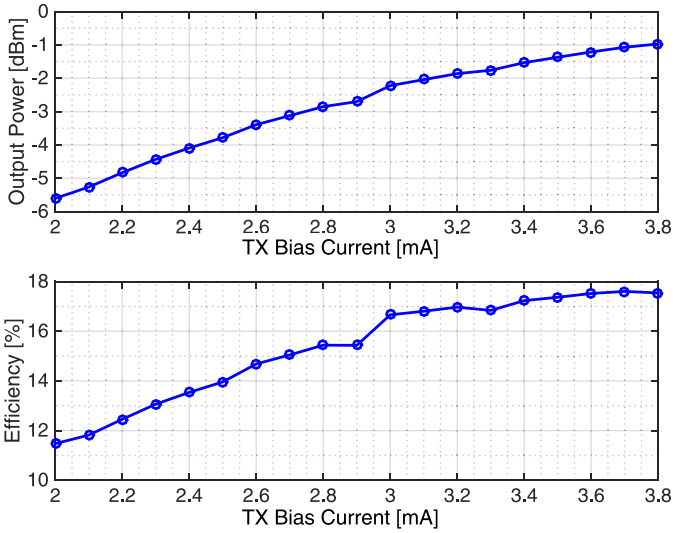

Fig. 12. Transmitted power and TX efficiency versus TX bias current.

The impedance transformation between the PA output and the antenna was realized on the evaluation board to have more flexibility during the testing phase. The L-matching network also provides a DC path for the bias current. The modulated signal is provided externally through an R&S SMA200W Vector Signal Generator while the transmitted signal is sensed by an R&S FSW26 Signal Analyser.

As previously reported, the VCO has to be biased properly to maintain its Class-C operation. The scheme proposed by [10] has been applied, as shown in Fig. 10. An operational amplifier is able to set the DC value at the drain of the current mirror M_{tail}; thus, current flowing through the current mirror will be maintained constant during both start-up and steady state. By applying this solution, oscillation amplitude can be maximized while still keeping oscillation start-up robust.

VI. Measurement Results

The chip micrograph is reported in Fig. 11. The die measures 1.3 mm $\times$ 1.0 mm while the active area of the design is 0.2 mm^2 (dominated by the integrated inductor). The rest of the area is occupied by the pads and decoupling capacitors to better filter interferences coming from the external biases. The supply voltage is 1.2 V for the entire chip. $V_{\text{DD,VCO}}$ was set to 0.9 V to minimize the PN and with it carrier-frequency drift and the FSK error.

The output power and the TX efficiency versus the TX bias current are plotted in Fig. 12. Note that the TX transmission

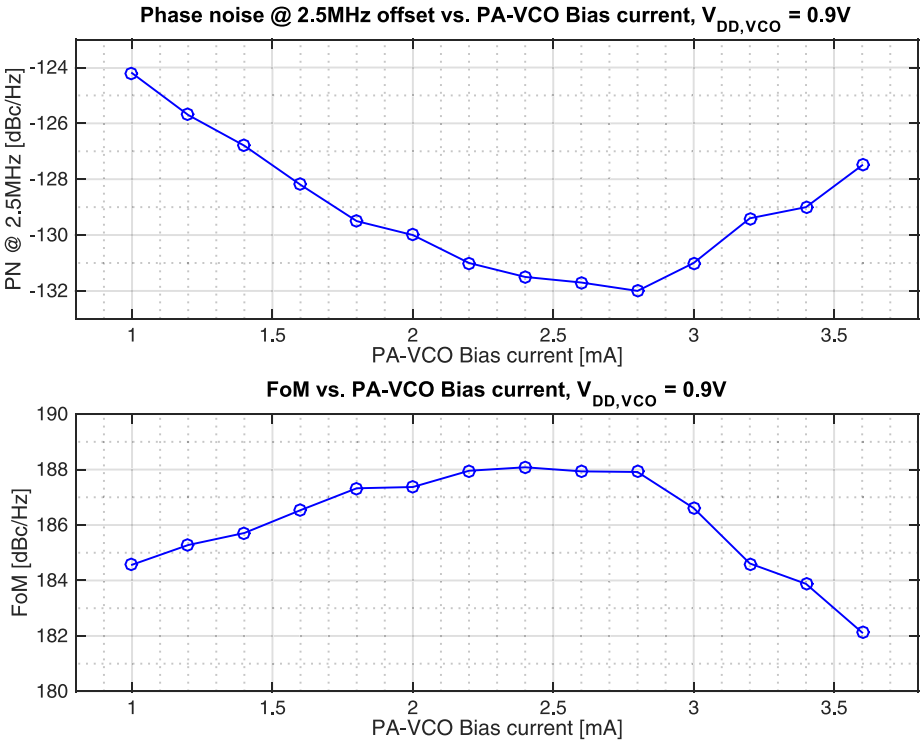

Fig. 13. PN and FoM versus VCO bias current.

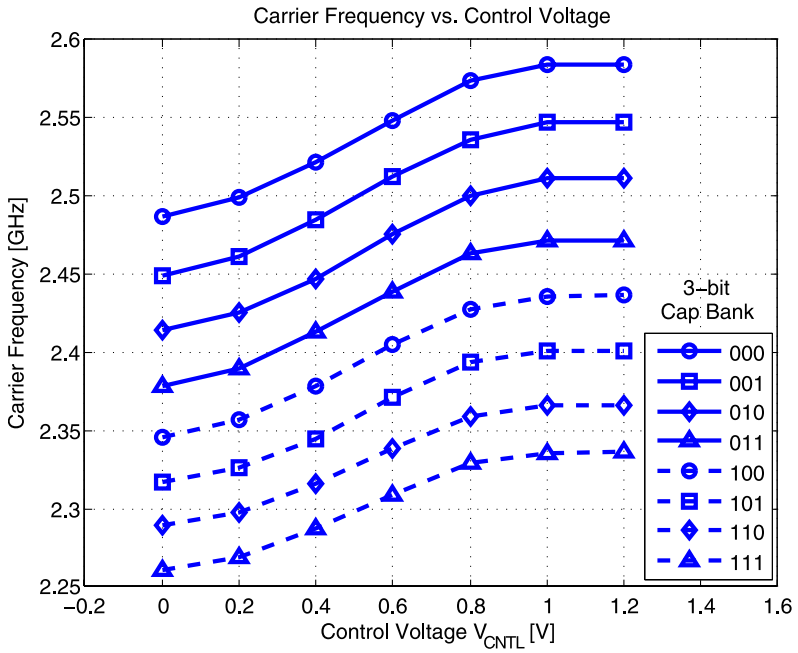

Fig. 14. FTR under capacitive divider setting 100_2.

occurs when the PLL is in open-loop and powered off. Thus, the only excess power consumption other than the PA-VCO stack is two operational amplifiers (one used for Class-C VCO biasing and another used as a buffer in the PLL loop). These op-amps consume 0.2 mA in total. The peak TX efficiency is equal to 17.5% when the TX consumes a total current of 3.8 mA. Since power dissipations of both the VCO and the PA scale during the sweep, the overall efficiency can be kept above 11% in the entire range from 2.0 mA to 3.8 mA. From (11), it is possible to extrapolate the efficiency of the PA to be approximately 70% when delivering an output power of -1 dBm. Notice that, in all of the measurements, the matching network (optimized for an output power around 0 dBm) has been kept constant.

The free running VCO achieves almost constant PN level through the entire ISM band. A plot of the PN and the Figure of Merit (FoM) versus the VCO bias current is reported in Fig. 13. The measurements were taken with a carrier of

TABLE I
CHIP SUMMARY AND COMPARISON WITH STATE OF THE ART

	This work	[14]	[15]	[16]	[17]	[4]	[18]	[19]	[20]
Max. Transmitted Power [dBm]	**-1**	+4	-3	+5	-1	+1.9	+1.6	+3	+1
Peak Efficiency (@ output power [dBm])	**17.5% (@-1)**	9.1% (@0)	9.8% (@-3)	10.5% (@0)	14.7% (@-1)	17.4% (@+1.9)	24.5% (@+1.6)	36% (@+3)	28.6% (@+1)
Modulation Type	**GFSK**	GFSK	GFSK	GFSK	GFSK	GFSK	GFSK	GFSK	GFSK
Data rate [Mb/s]	**1**	1	1	1	1	1	1	1	1
FSK Error [%]	**0.69**	N.A.	N.A.	N.A.	2.8	N.A.	N.A.	N.A.	4.78
Max. Carrier-Frequency Drift [Hz/µs]	**7**	N.A.	N.A.	N.A.	N.A.	20	20	N.A.	57.44
PN [dBc/Hz] @2.5MHz	**-129**	N.A.	-116*	-125	-119*	-118.5	-117	-124*	N.A.
Technology	**130nm CMOS**	90nm CMOS	65nm CMOS	65nm CMOS	90nm CMOS	130nm CMOS	130nm CMOS	28nm CMOS	40nm CMOS
Power dissipation [mW]	**4.56**	11	5.1	9.5	5.4	8.9	5.9	5.5	4.4
Supply Voltage [V]	**1.2**	1.2	1.1	1.3	1.2	1.0	1.0	0.5/1.0	1
Chip Area [mm^2]	**1.3/0.2****	1.95	7.84	0.35**	3.61	1.54	2.1	N.A.	1.3

* PN @2.5MHz was normalized from the one at 1MHz
** Core area

2.45 GHz at 2.5 MHz frequency offset. The minimum PN of -132 dBc/Hz is obtained for a TX bias current equal to 2.8 mA. After this point, the amplitude of the VCO exceeds the one required to operate efficiently in Class-C. The following oscillator FoM has been used in the calculation [13]:

$$\text{FoM} = -L(\Delta f) + 20\cdot\log\left(\frac{f_{\text{osc}}}{\Delta f}\right) - 10\cdot\log\left(\frac{P_{\text{diss}}}{1\text{ mW}}\right) \quad (14)$$

where f_{osc} is center frequency, Δf is the offset frequency from the center, $L(\Delta f)$ is the PN at specific offset, and P_{diss} is the DC power consumed by the VCO. With $V_{\text{DD,VCO}}$ equal to 0.9 V, the peak FoM achieved is 188 dBc/Hz. The VCO frequency tuning range (FTR) is reported in Fig. 14 when the 3-bit capacitive divider is set to binary value 100_2 (typical operative condition). By acting on the 3-bit capacitor bank and the varactor connected to the PLL, the output frequency sweeps from 2.26 GHz to 2.58 GHz, leading to a FTR of 13.2%.

The TX performance was evaluated by employing both FSK and GFSK modulation signals (with a modulation index of 0.5). The modulations were applied by calibrating the amplitude of the signal driving the varactor on-board. The spectrum plot is shown in Fig. 15; the emission mask is respected for both cases with excess margin since low power is transmitted. At a data rate of 1 Mb/s, a maximum carrier-frequency drift of 7 Hz/μs and an FSK error below 0.7% were obtained. A screenshot of the output spectrum between 0.5 GHz and 10 GHz while delivering a single tone at -1 dBm is reported in Fig. 16 (0.6 dB of cable/board losses are not de-embedded). All higher-order harmonics of the LO and the transmitted signal remain below -40 dBm.

A summary of the performance of the proposed design and other GFSK transmitters at 2.4 GHz is reported in Table I.

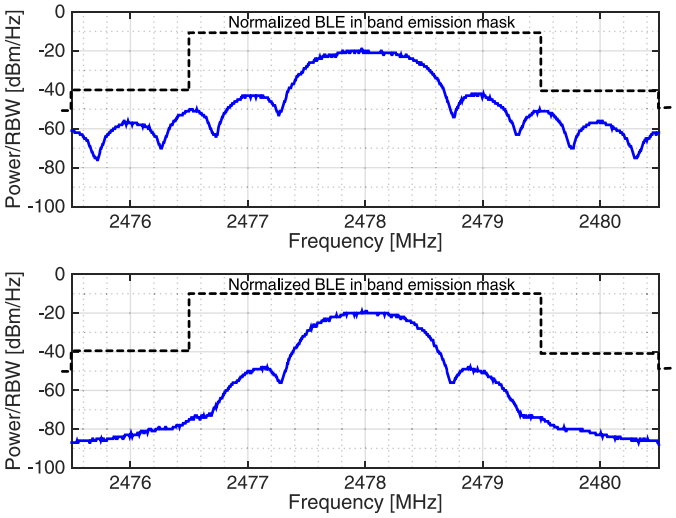

Fig. 15. Transmitted PSD with FSK and GFSK modulation index of 0.5 at 1 Mb/s data rate (5 MHz span and 10 kHz resolution bandwidth).

The comparison with different solutions is not simple since several TXs were designed to maximize their efficiency for P_{RF} higher than 0 dBm, e.g., [16]. Comparing with other sub-mW output power TXs, a significant improvement of carrier-frequency drift and the FSK error was obtained without sacrificing efficiency. Since the TX is in open-loop, the oscillator PN affects not only the out-of-band emission performance but also carrier-frequency drift and the FSK error. Although the VCO burns the majority of the power, a comparable efficiency was obtained due to a higher PA efficiency thanks to the PA operation with a very low voltage supply. Although the prototype has an external matching network for testing purposes (i.e., a high Q inductor), its impact on the overall

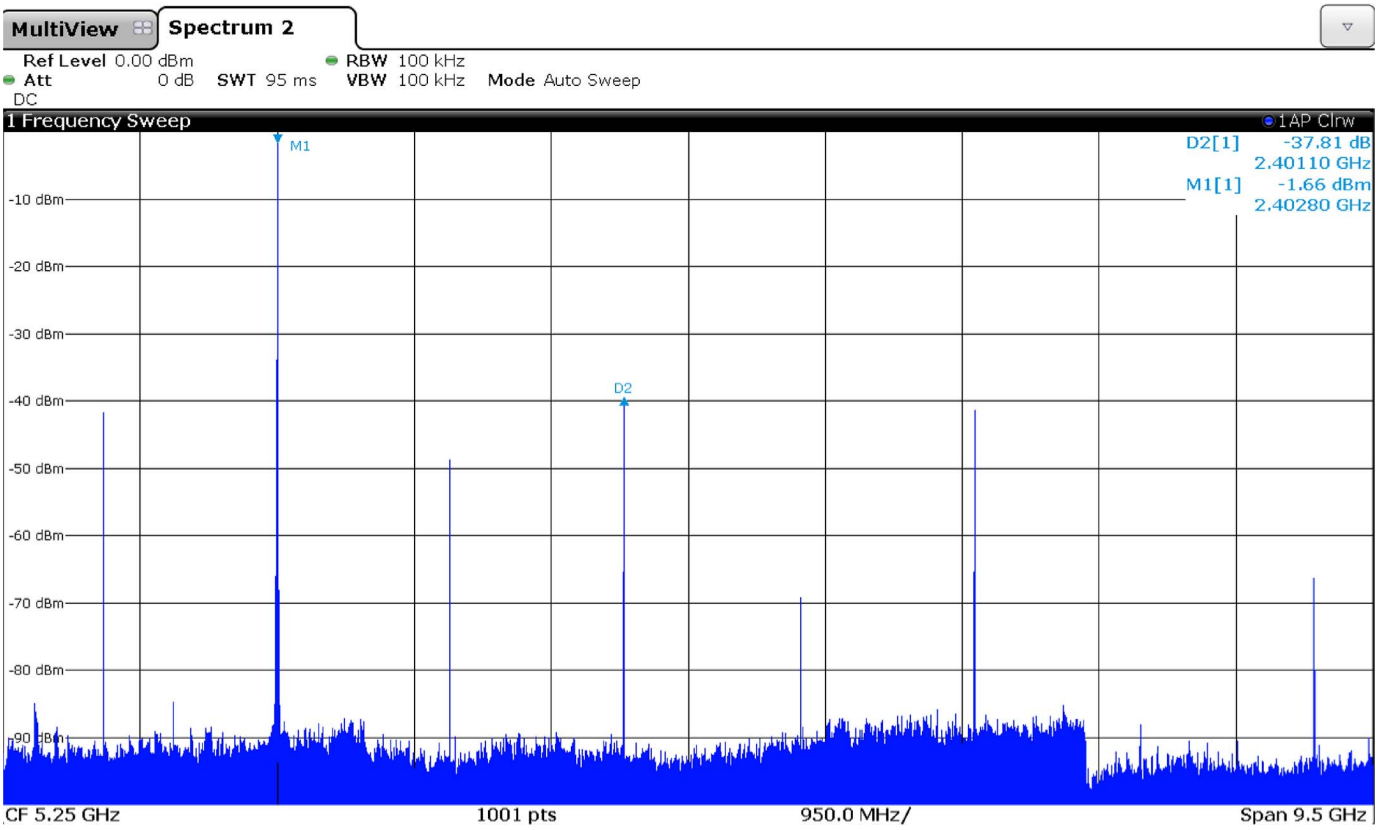

Fig. 16. The 0.5 GHz–10 GHz output spectrum while delivering single tone at −1 dBm (0.6 dB of cable/board losses are not de-embedded).

efficiency is minimal since $V_{DD,PA}$ resembles V_{RF} and, as shown by (4) and (12), in such case η_M is close to one regardless of the Q_L value.

VII. Conclusion

A current-reuse PA-VCO topology for low power FSK/GFSK transmitters has been presented. By stacking a Class-C VCO and a boosted common-gate PA, high TX efficiency at low output power (−1 dBm) was achieved. The proposed design demonstrated low carrier-frequency drift and FSK error without significantly sacrificing the TX efficiency due to the PA operation with a small voltage supply.

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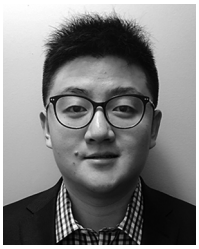

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