A 2.4-GHz 1.3-mW OQPSK RF Front-End TX Based on an Injection-Locked Power Amplifier

Saba Zargham, *Member, IEEE* , Zexi Ji, and Antonio Liscidini, *Senior Member, IEEE*

***Abstract*— An injection locking power amplifier is presented. The proposed solution, tailored to quadrature phase shift keying (QPSK) modulation for IoT has been realized by exploiting the property of an injection-locked frequency divider to work as a phase rotator. Hence, the divider's output is directly coupled to the antenna by a transformer to deliver the desired output power. The combination of these two ideas resulted in a high-efficiency, high-bandwidth QPSK RF front-end for IoT, capable of operating at up to 120 Mbit/s and delivering 1.3-mW output power while burning 3.4 mW.**

***Index Terms*— Injection locked divider, IoT, low power transmitter, offset-quadrature phase shift keying (QPSK) (OQPSK), power amplifier (PA), QPSK, quadrature oscillator, TX.**

I. Introduction

HIGH data-rate wireless protocols have been developed to address the increasing demand for high-speed wireless communications. However, more often than not, available bandwidths are limited in the increasingly crowded spectrum. It is, therefore, much to our advantage to design transmitters that utilize more spectrally efficient modulation schemes. Offset-quadrature phase shift keying (OQPSK) is one such modulation scheme that exhibits high spectral efficiency. With the data being encoded in the signal's phase rather than its amplitude, this quasi-constant-envelope modulation makes it possible to limit the power dissipated in the RF transmitters since non-linear and high-efficiency power amplifiers (PAs) can be used in the transmitter chain [1]–[3]. Furthermore, the PA can simply be fed by a signal coming from a voltage-controlled oscillator (VCO) without requiring any mixers to up-convert the baseband signal.

Traditionally, phase modulation can be generated using both closed-loop (e.g. PLL) and open-loop (e.g. phase multiplexer) architectures [2], [4], [5]. Closed loop solutions are typically less noisy but often with a limited modulation bandwidth. On the other hand, while open loop implementations allow larger bandwidths and potentially higher data rates [3], [6], they suffer from mismatches and non-idealities introduced by the multiplexers.

Manuscript received December 2, 2019; revised June 12, 2020 and December 8, 2020; accepted January 2, 2021. Date of publication January 29, 2021; date of current version April 23, 2021. This article was approved by Associate Editor Kenichi Okada. *(Corresponding author: Saba Zargham.)*

The authors are with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S, Canada (e-mail: saba.zargham@mail.utoronto.ca; zexi.ji@mail.utoronto.ca; antonio.liscidini@utoronto.ca).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3052178.

Digital Object Identifier 10.1109/JSSC.2021.3052178

One technique that has gained popularity for low-power transmitter design is injection locking, where the LC VCO or a ring oscillator in the transmitter chain, is locked to an input reference. This, not only has the benefit of reducing the complexity of the whole system (i.e. by removing the need for multi-phase PLLs [3]) but also improves the output phase noise if a clean reference signal is used [6].

One such transmitter designed using direct modulation is brought forth in [3]. In this article, an injection locking phase generator along with a polarity swap circuit are used to generate OQPSK/QPSK modulation. By changing the self-resonant frequency (SRF) of the VCO, the output phase changes by 90°, creating the two symbols at ±45°. The polarity swap circuit is then used to generate the two remaining symbols of the QPSK constellation. While this transmitter benefits from the aforementioned advantages of injection-locking, changing the SRF could give rise to the error-vector-magnitude (EVM). In other words, this design suffers from systematic constellation errors due to the capacitor bank design. These errors translate directly into phase errors and degrade the EVM. The 6-bit binary cap adopted by this design results in a 10° phase accuracy at the output which in turn affects the phase error and degrades the EVM. An EVM of 11.493% for OQPSK at 50 Mb/s is reported.

Another drawback of open-loop systems is the need to simultaneously generate all the possible output phases at the same time. This can result in power-hungry systems especially in IoT applications, where the power dissipated in the PA can be comparable to the one required for phase generation [7], [8]. When a low power signal is transmitted, the generation of multiple phases simultaneously could lead to a significant increment in the overall power consumption. This in turn consumes more power compared to a system that can generate each phase on demand, thus avoiding the extra power dissipation of the idle phases.

The transmitter proposed in [6] is an example of this approach. This design uses an injection locked ring oscillator (ILRO), and a digital PA embedded with a phase multiplexer for QPSK modulation. Compared to the direct conversion transmitters, this design has many advantages. Namely, employing a subharmonic ILRO offers an improved energy efficiency compared to a PLL-based ring oscillator, as it removes the need for many additional building blocks such as a phase detector, charge pump, loop filter, and divider. Moreover, the constraints on the phase noise performance of the ring oscillator are relaxed as the system benefits

from injection locking and therefore is predominated by the reference phase noise in the vicinity of the locking frequency. However, it does suffer from the mentioned drawbacks of an open-loop structure. In fact, at −9 dBm, the power required for the generation of all possible phases simultaneously is 2.26 mW, which is more than the transmitted power, leading to a significant loss of efficiency.

This article tries to address the above issues outlined for the open-loop transmitters, by the use of a very compact and low power approach where the phase modulator and the PA are merged into a single stage called an injection-locked power amplifier (ILPA) [9]. The presented structure exploits the property of an injection-locked frequency divider (ILFD) that can act as a phase rotator, when the sign of the injected signal toggles between plus and minus (Fig. 1). The proposed solution eliminates the need for a phase multiplexer typically required in open-loop wide-band modulators and does not require multiple phases to be synthesized simultaneously.

Additionally, compared to previous work, where two different dividers—with two different LC tanks—were used to generate the four phases [12], this architecture uses one single injection locked LC divider to generate all four phases of the QPSK, therefore minimizing the output phase mismatches. It is worth mentioning that, as this design does not include the LO generation block, if not designed properly, this could negatively affect the output phase noise. Whether fed externally or ON-chip, as long as the input exhibits a reasonable phase noise around the carrier, the output EVM and spectrum will not be deteriorated. With proper ON-chip LO however, one main contributor to the output phase error would be the mismatch in the MUX used to toggle between the two antiphase inputs. In this article, it will be shown how the presented solution can offer a large modulation bandwidth, a low EVM, and a relatively high power efficiency.

This article is structured as follows. Section II focuses on quadrature generation based on an ILFD. Section III discusses the limitations of such a system when used as a phase modulator, Section IV further explains the whole system integrated with the PA, Section V describes the characteristics of the proposed prototype, and Sections VI and VII summarize the measurement results and conclusions.

II. ILFD for Quadrature Generation

A. Injection-Locked Frequency Dividers

The working principle of the injection-locked LC divider has been extensively studied [10], [11]. It can also be easily understood by considering the cross-coupled pair as a mixer in feedback that down-converts the input signal [12] as shown in Fig. 2(a).

The input signal in this case is the input current consisting of the biasing term plus a current running at $\omega_{\text{inj}} = 2\omega_{\text{out}}$, injected at the common source node of the cross-coupled pair. The injection prompts the tank to introduce a phase shift, $\beta(\omega)$, between the output voltage and input current. This phase shift ranges from $\pi/2$ to $-\pi/2$ and is a function of $\Delta\omega = \omega_{\text{out}} - \omega_o$ [12]. This leads to a deviation in the oscillation frequency. The reason is that now the tank's natural frequency

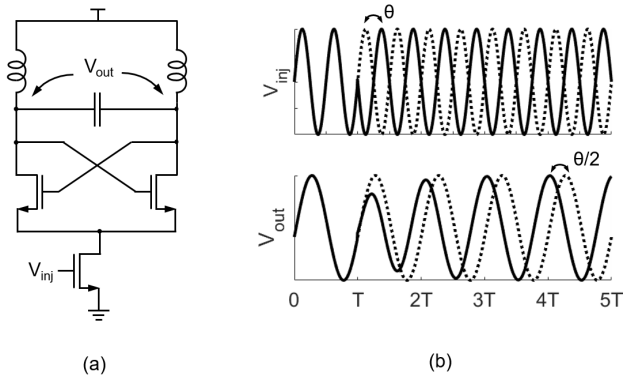


Fig. 1. (a) Injection-locked LC frequency divider with tail injection. (b) Injected signal and corresponding output voltage for an unmodulated (dotted line) and modulated (solid line) input [9].

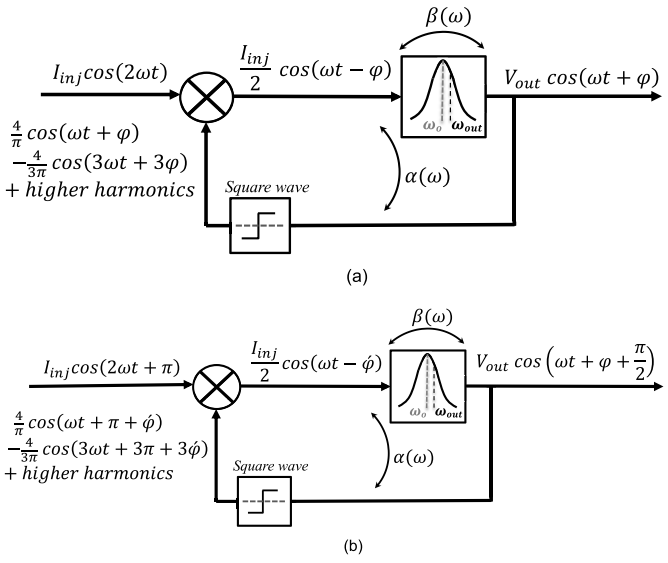


Fig. 2. Simple behavioral model for the ILFD. (a) No input phase shift [12], (b) With 180° input phase shift.

of resonance, ω_o, no longer satisfies the oscillation condition for phase. In order for the loop to sustain oscillation, the net phase shift around the loop should remain 0. To maintain oscillations under injection, the mixer introduces a phase shift of α, such that

$$\alpha + \beta = 0. \tag{1}$$

From Fig. 2(a), if we take the output phase equal to φ, we have

$$\alpha = -2\varphi \tag{2}$$

$$\beta = 2\varphi. \tag{3}$$

Thus, the system is able to lock to the input and oscillate at $\omega_{\text{out}} = (\omega_{\text{inj}}/2)$. Note that the input current driving the mixer is not a pure sine wave but rather, due to the hard limiting operation of the switches, a square wave. When this current is mixed with the output voltage of the LC tank resonating at ω_{out}, mixing components at the sum and difference of the two frequencies are produced. The high-frequency component at

$3\omega_{\text{out}}$ is attenuated by the inherent filtering of the tank tuned at ω_o. As a result, the divider is locked to the input LO signal and oscillates at ω_{out}.

It is worth mentioning that this locking occurs within a certain lock range, ω_L, around the resonant frequency. Assuming square wave mixing and a total zero phase shift around the loop, an expression for the locking range can be derived [12]. From (4) it is clear that ω_L is proportional to the injection ratio and inversely proportional to the quality factor of the tank

$$\omega_L = \frac{2}{3}\frac{\omega_o}{Q} \cdot \frac{I_{\text{inj}}}{I_{\text{dc}}}. \tag{4}$$

A similar expression for the LR is derived in [14] and [15], as well.

B. ILFD as a Phase Rotator

The key to using the ILFD for quadrature generation, is utilizing it as a phase divider, as well as a frequency divider. Consider the block diagram of Fig. 2(b), where now an input phase shift of 180° or π (rad) is incorporated in the phase of the injected current. This figure illustrates the idea behind using a single injection-locked oscillator for quadrature generation.

Similar to Fig. 2(a), the output phase of the mixer, φ', experiences the phase shift of the LC tank, β

$$\omega t - \varphi' + \beta = \omega t + \varphi' + \pi \tag{5}$$

$$\varphi' = \frac{\beta - \pi}{2}. \tag{6}$$

Recall from (3), the output phase in the absence of any input phase shift was

$$\varphi = \beta/2. \tag{7}$$

Therefore, the total phase shift at the output compared to Fig. 2(a) is

$$\varphi' + \pi - \varphi = \frac{\pi}{2} = 90°. \tag{8}$$

The injection-locked divider can also be studied by treating the divider as a time-invariant system where an input $x_1 = \cos(2\omega t)$ corresponds to an output $y_1 = \cos(\omega t + \theta_{\text{initial}})$. Assume a phase shift is then introduced at the input of the divider, holding

$$x_2 = \cos(2\omega t + \phi_{\text{in}}) = x_1\left(t + \frac{\phi_{\text{in}}}{2\omega}\right). \tag{9}$$

Due to the time-invariance property of the system and the divide-by-2 operation, the resulting output is equal to

$$y_2 = y_1\left(t + \frac{\phi_{\text{in}}}{2\omega}\right) = \cos\left(\omega\left(t + \frac{\phi_{\text{in}}}{2\omega}\right) + \theta_{\text{initial}}\right). \tag{10}$$

Eventually, the output locks to a signal that is half of the input, in both phase and frequency

$$y_2 = \cos\left(\omega t + \frac{\phi_{\text{in}}}{2} + \theta_{\text{initial}}\right). \tag{11}$$

Based on the analysis above, a polarity flip (i.e. 180° phase shift) at the input would correspond to a 90° phase shift at the output, thereby making the ILFD a suitable candidate to generate OQPSK modulation directly and efficiently.

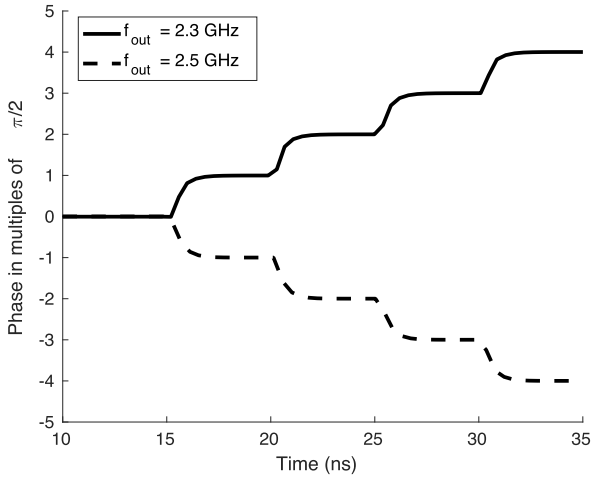


Fig. 3. Transient phase response for two output frequencies f_{out} of 2.3 and 2.5 GHz, on opposite sides of the resonant frequency $f_o = 2.4$ GHz. The input polarity is flipped every 5 ns.

Mazzanti *et al.* [13] have shown that two injection locked frequency dividers can be used to generate quadrature modulation, given that they are driven by antiphase inputs. In this method, however, any mismatch between the two dividers would lead to quadrature error [13]. In the following section, it will be shown that through a dynamic flip of the polarity of the input signal, even a single ILFD can be used as a PSK modulator by producing an output whose phase, can rotate by arbitrary increments of 90° as a function of the phase of the input signal. (Fig. 3).

III. Theoretical Analysis

A. Phase Shift Direction

A polarity flip corresponds to either 180° or −180° phase shift. While these are indistinguishable at the input, they can lead to different phase shifts at the output (i.e. 90° and −90°). This indicates that the output phase can either advance or lag in response to the input trigger. In the case of an LC injection locking divider, the direction of the phase shift depends on the relative position of the output frequency (ω_{out}) with respect to the resonant frequency of the tank (ω_o). Particularly, if $\omega_{\text{out}} < \omega_o$, the output phase will advance by 90° each time the input polarity is flipped, and if $\omega_{\text{out}} > \omega_o$, the output phase will lag by 90° (Fig. 3).

This behavior can be explained intuitively considering the fact that an injection locked oscillator, once unlocked, will tend to its intrinsic resonant frequency, ω_o. When the input polarity changes, the system is temporarily unlocked from steady state and tends to maintain its oscillations now at ω_o. The loop, therefore, compensates for this frequency difference by *leading* or *lagging* the output phase depending on the difference between the steady state output frequency, ω_{out}, and ω_o, until a new steady-state output frequency is reached. During this time, if $\omega_{\text{out}} - \omega_o$ is negative the output phase will increase, if the difference is positive the output phase will start

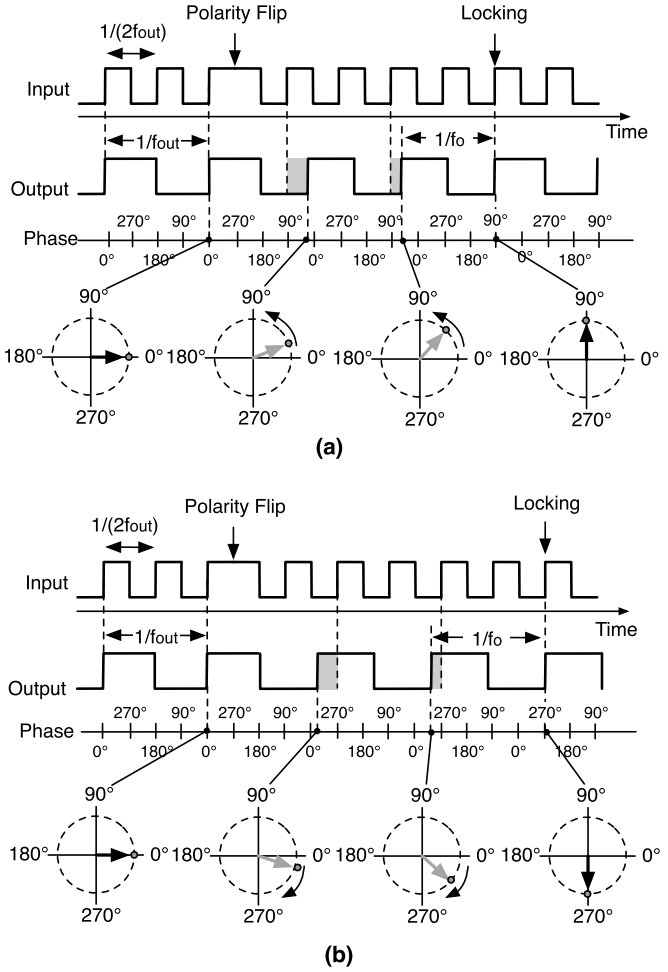


Fig. 4. Phase change due to an input polarity flip. (a) When f_o is greater than f_{out} (e.g. $f_o = 2.4$ GHz $f_{\text{out}} = 2.3$ GHz). (b) When f_o is smaller than f_{out} (e.g. $f_o = 2.4$ GHz $f_{\text{out}} = 2.5$ GHz).

to decrease. In this process, not only the sign of the frequency difference is important but also its magnitude. In fact, it will be shown analytically in this article that the phase variation per cycle is proportional to $|\omega_{\text{out}} - \omega_o|$ by determining the settling time between two steady-states.

To provide a better understanding of the system's operation, the input (injection) and output signals have been plotted for two different output frequencies in Fig. 4 along with a reference phase. Initially, the output is locked to the input reference. The corresponding edges are synchronized each period, maintaining an oscillation at f_{out}. Once a polarity flip occurs and the input phase shifts by 180°, the divider is temporarily unlocked. It will then try to revert to its intrinsic frequency of resonance by speeding up if $f_o > f_{\text{out}}$ [e.g. Fig. 4(a)] or slowing down if $f_o < f_{\text{out}}$ [e.g. Fig. 4(b)], until it can once again lock to the proper edge of the input resuming oscillations at f_{out}. As a result, this chain of events will have shifted the output phase by 90°. As shown in Fig. 4(a) and (b), such behavior corresponds to a phasor that rotates clockwise or counterclockwise upon the relationship between f_o and f_{out}.

While this behavior might imply a limitation of the system, the *unilateral* nature of the output phase shifts is in fact what enables us to perform quadrature modulation in the first place. Each time the input polarity is flipped, rather than jumping back and forth, the cumulative phase jumps make it possible to traverse the full QPSK constellation circle in three steps. Note that the output phase jumps are confined to 90° at a time, similar to an OQPSK modulation. This has the benefit of avoiding sharp 180° phase jumps at the output and minimizing variations in the signal's envelope.

This qualitative analysis is suggestive of the presence of some tradeoffs in using an injection locked divider as a phase modulator. Mainly, for a given output frequency the output phase can rotate only in one direction. This means that in order to move arbitrarily between the four symbols of a QPSK constellation, up to three polarity flips—in the worst case—are needed at the input. This corresponds to three 90° phase shifts at the output to reach the farthest symbol. If the intermediate phase shifts, however, occur at the maximum possible speed, the transition times between symbols become negligible compared to the symbol period itself. In this case, the modulation bandwidth is no longer limited to the intermediate transition times between the QPSK symbols. In other words, oversampling the system enables us to achieve higher modulation bandwidths. What sets the lower bound of the inter-symbol transition times and how the transition period affects the output spectrum is further explored in the following sections.

B. Settling Time

As previously discussed, the output phase does not have an instantaneous response to a change in the input phase. As shown in Appendix A, an expression for the characteristic time constant (τ) of the settling time can be derived, by assuming a class B operation for the input transistor

$$\tau = \frac{2Q}{\omega_o} \frac{1}{1 + \left(2Q \frac{\Delta\omega}{\omega_o}\right)^2} \tag{12}$$

where Q is the quality factor of the tank, ω_o is the resonant frequency and $\Delta\omega = \omega_{\text{out}} - \omega_o$ is the deviation from the resonant frequency. A first order approximation of the time constant is thereby [16]

$$\tau = \frac{2Q}{\omega_o}. \tag{13}$$

From (13), it can be deduced that decreasing Q would lead to a lower settling time. Although typically having a low quality factor is not desirable, it will be shown that in the case of an injection locking PA, such condition is automatically obtained to ensure that the majority of the power from the tank is transferred to the output load (i.e. the antenna).

The behavior expressed by (12) can be intuitively understood considering that a greater quality factor, leads to a lower energy loss, and, therefore, less current is required to sustain/lock the oscillation. Furthermore, since the settling of the output phase depends on how quickly the divider locks to the input current signal, less current injected into the tank would require more cycles to change the frequency, leading to a longer settling time. The linear dependence of

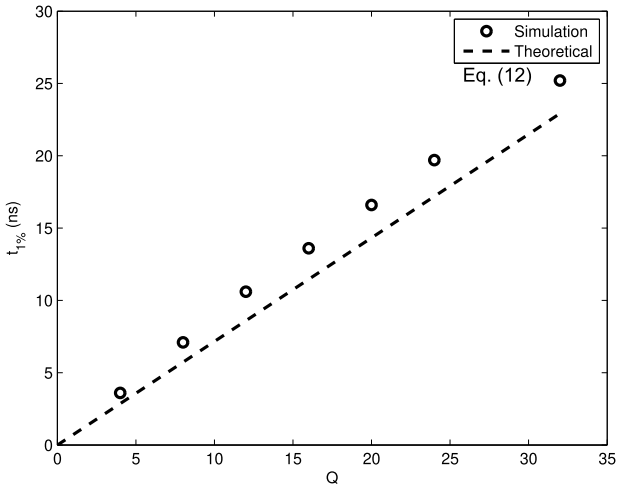


Fig. 5. 1% Settling time versus quality factor for both theoretical and simulated values. Theoretical data plotted using (12).

the quality factor and settling time expressed by (12) has been verified through simulations reported in Fig. 5, where the expected linear relationship has been obtained. Our main interest, however, is to measure the time it takes for the phase to settle within 1% of its final value. This corresponds to around 4.5τ. Fig. 7 plots the 1% settling time normalized to the resonant frequency for different frequency offsets, where simulated and theoretical values fairly match. Furthermore, (12) also confirms the intuition that the time constant decreases as you operate further away from the resonant frequency. This is related to the fact that the slope of the phase shift due to the LC tank decreases as you move away from the resonant frequency.

It is worth noting that as long as the divider remains locked, the output phase will always shift by exactly 90° with each input polarity flip—180° divided by two—independent of $\Delta\omega$. This is advantageous in the sense that it makes the output phase shifts independent of any potential drift in the resonant frequency of the tank and contribute to a more robust design. A drift in the intrinsic resonant frequency could, however, slightly change the settling time according to (12). From both Fig. 7 and (12), it can be seen that this variation farther away from the carrier (i.e. typical case for larger bandwidth and smaller settling times) decreases. The relatively wide locking range provided by the low quality factor of the LC tank, also ensures this.

C. Minimum Switching Time

In addition to settling time, the minimum switching time, $t_{\min}$, is another important parameter limiting the modulation bandwidth. This refers to how quickly the polarity of the input signal can be flipped multiple times such that the output phase continues to shift in the same direction. As will be shown, in order to shift the phase more than 90°, it does not need to settle every step, thus reducing significantly the time required for multiple phase jumps. As shown in the example in Fig. 6, in response to a flip of the input signal, the divider is unlocked and the instantaneous output frequency ω_{inst} experiences a jump changing its relative position

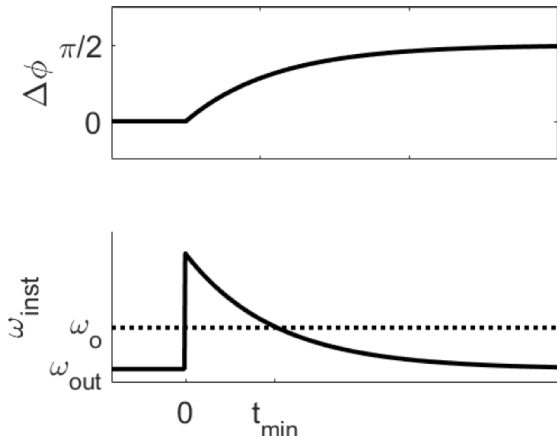


Fig. 6. Conceptual diagram demonstrating the phase and frequency transition after one polarity flip.

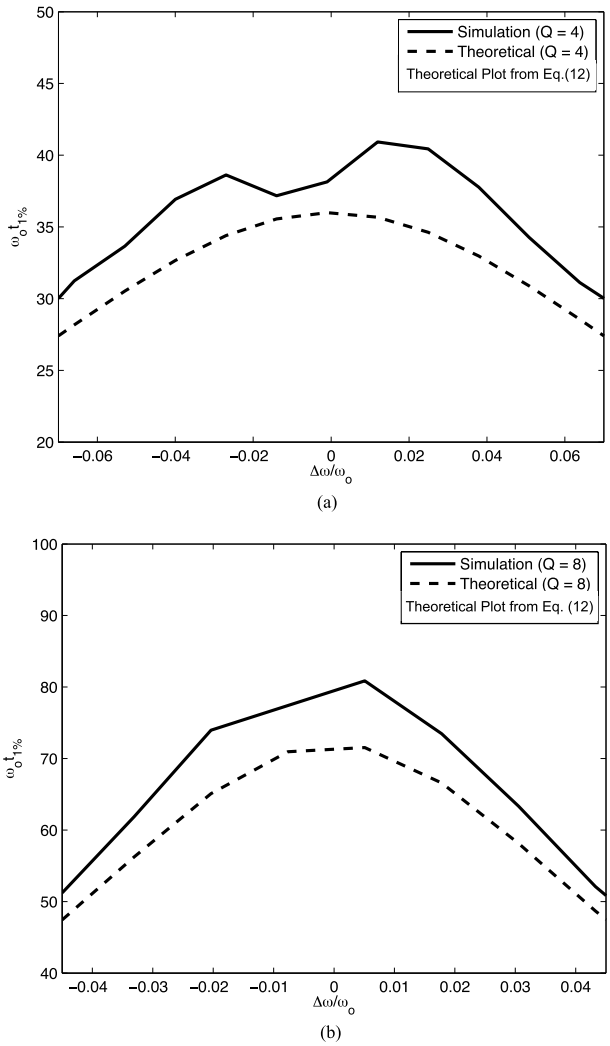


Fig. 7. Normalized 1% settling time versus fractional deviation from the resonant frequency, theoretical ((12)) versus simulated values. (a) $Q = 4$. (b) $Q = 8$.

about ω_o. Since the direction of the phase shift depends on the sign of $\omega_{\text{out}} - \omega_o$, if the input is flipped once more before the minimum switching time $t_{\min}$, the output

phase will start to decrease by settling back to its original value.

Assuming exponential settling for the output phase (i.e. first order response), results in the following expression for $t_{\min}$

$$\phi(t) = \phi_i + \frac{\Delta\phi_{\text{in}}}{2}\left(1 - e^{-\frac{t}{\tau}}\right) \tag{14}$$

where ϕ_i is the initial output phase in steady state, $\Delta\phi_{\text{in}}$ is the phase shift introduced at the input, and τ is the time constant previously discussed. The instantaneous frequency, ω_i, at the output is equivalent to

$$\omega_i = \omega_{\text{out}} + \frac{d\phi}{dt}. \tag{15}$$

In order for the phase to continue to shift in the same direction, the instantaneous frequency must lie on the same side of the resonant frequency as it was during steady-state. This results in the following constraint:

$$\left|\frac{d\phi}{dt}\right| \leq |\Delta\omega| \tag{16}$$

which would then lead to the expression below for the minimum switching time

$$t_{\min} = \tau \ln\left|\frac{\Delta\phi_{\text{in}}/2}{\Delta\omega \cdot \tau}\right|. \tag{17}$$

Substituting for $\tau = 2Q/\omega_o$ (The dependence of τ on $\Delta\omega$ is neglected for simplicity) and $\Delta\phi_{\text{in}} = \pi$, equivalent to one polarity flip

$$\omega_o t_{\min} = 2Q \ln\left|\frac{\pi}{4Q\frac{\Delta\omega}{\omega_o}}\right|. \tag{18}$$

Theoretical and simulated values for $t_{\min}$ are plotted in Fig. 8, indicating the minimum switching time is significantly higher when operating near the resonant frequency. Evidently, for faster performance, the desired output frequency should not be too close to the selected resonant frequency. It must, however, still lie within the locking range of the oscillator. Moreover, operating close to the edge of the locking range results in an attenuated output amplitude.

D. Modulation Bandwidth

Ultimately, the modulation bandwidth of the ILFD is predominantly limited by the settling time of the output phase and the minimum switching time. From (13), considering the first-order approximation for the time constant associated with the output phase change and taking $Q = 4$, at $\omega_o = 2.4$ GHz the resulting 1% settling time is around 2.3 ns. This means that we can have single transitions between consecutive symbols at roughly 400 MHz. An estimate of the minimum switching time at 4% deviation from the resonant frequency is roughly 0.9 ns. As previously noted, it would require a maximum of three transitions to move between any two arbitrary QPSK symbols. The first two transitions can occur at the minimum switching time, while the final transition should be given enough time to fully settle (i.e. within 1%). The minimum symbol period is therefore around 4.1 ns, equivalent to a theoretical maximum data rate of 240 Msymbol/s corresponding to 480 Mbit/s. This, however, neglects other factors that may limit the speed.

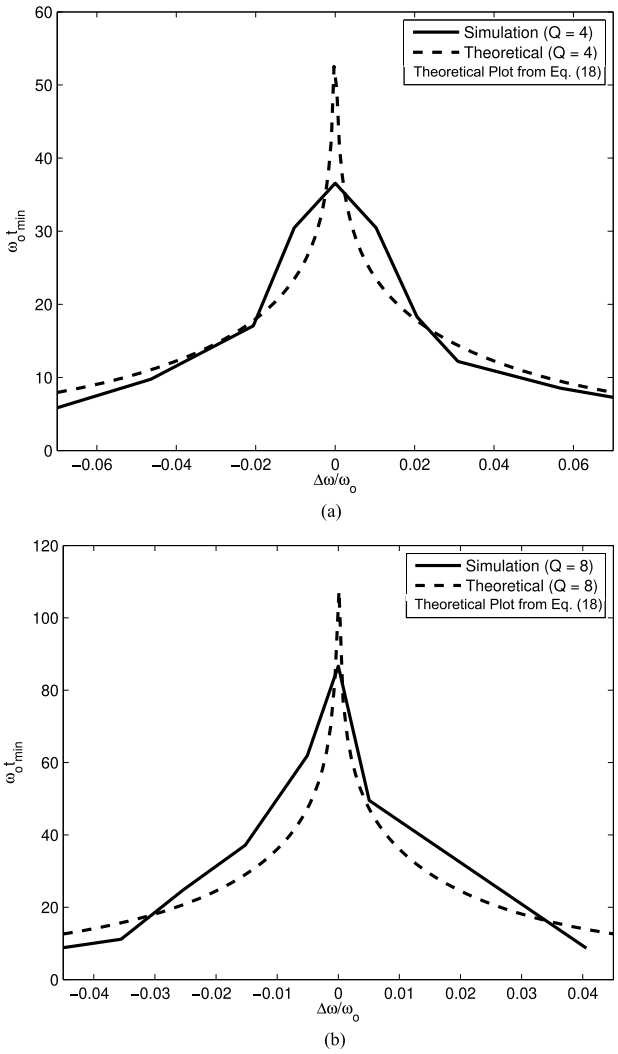


Fig. 8. Normalized minimum switching time versus fractional deviation from the resonant frequency, theoretical ((18)) versus simulated values. (a) $Q = 4$. (b) $Q = 8$.

E. Impact on the Spectrum

In an Offset-QPSK modulation scheme, the direct transition between non-consecutive symbols is nonviable. Furthermore, as previously discussed, for a given ω_{inj} and ω_o, the direction of the phase shift remains constant for the injection-locked modulator. Consequently, a certain asymmetry in the output spectrum can be expected. This is due to the fact that the shifting direction dictates the number of flips needed to move from any arbitrary symbol to the next. Operating at low data rates has the benefit of the inter-symbol transition times becoming negligible compared to the symbol period. In other words, oversampling the system addresses the asymmetry and the spectrum thus becomes analogous to that of an ideal QPSK as shown in Fig. 9. At higher data rates, however, the sidelobes are pushed farther out toward higher frequencies and therefore are more effectively attenuated by the filtering of the LC tank. Fig. 10 shows the output spectrum for three different symbol rates. Moreover, compared to the conventional QPSK, the OQPSK modulator has the benefit of a reduced peak-to-average power ratio, as sharp discontinuities in the output

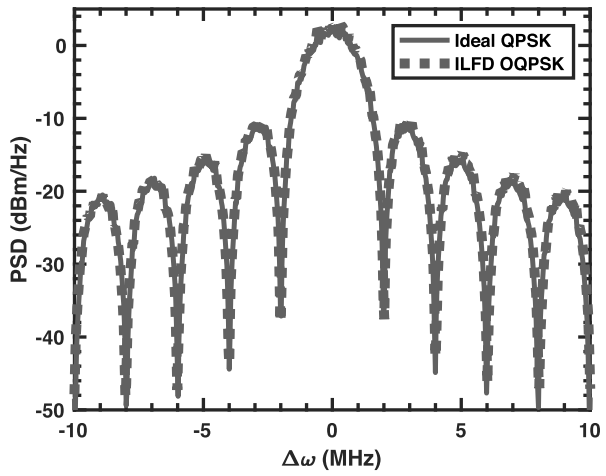


Fig. 9. Simulated output spectrum compared to an ideal QPSK at 2-MHz symbol rate.

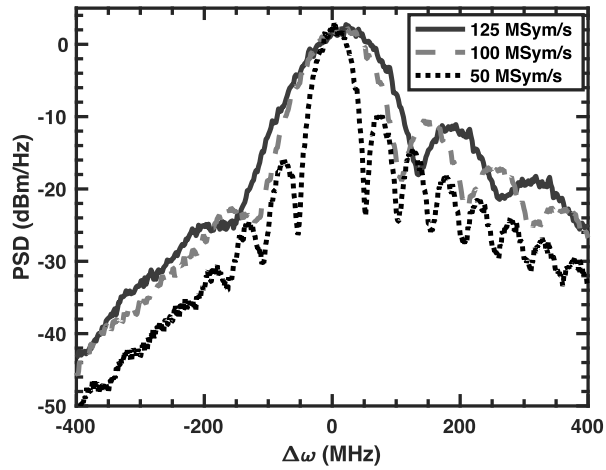


Fig. 10. Simulated output spectra for three different symbol rates.

phase are avoided, the inter-symbol transitions are smoother and the variation of the signal envelope is thereby smaller [7].

IV. Injection Locked PA

A transmitter chain commonly includes the power amplifier and matching network as its last components with the role of delivering the signal to the antenna at the desired power level. Nonetheless, it would be much more area efficient if the divider itself was regarded as a nonlinear PA. The cross coupled pair can be viewed as an amplifier fed by a modulated signal at $2\omega_{\text{out}}$. The amplifier is then coupled to the antenna through an integrated transformer resonating around the desired output frequency. This solution merges the phase generator and the PA into a single block called the injection-locked PA. Moreover, the transformer performs differential to single-ended conversion as well.

A. Q Factor and Efficiency

The efficiency of the ILFD can be determined as follows:

$$\eta = \frac{P_{\text{RF}}}{P_{\text{dc}}} = \eta_{\max}\frac{V_p}{V_{\text{DD}}} \tag{19}$$

where P_{RF} is the power delivered to the load of the oscillator, P_{dc} is the total power consumption, $\eta_{\max}$ is the maximum achievable efficiency and is dependent on the injection scheme, V_p is the amplitude of oscillations (rms) at the output, and V_{DD} is the supply voltage. Assuming class-B biasing of the input transistor and injecting a 50% duty cycle square wave current into the divider, leads to the first harmonic of the output current as $I_0 = (4/\pi)I_{\text{dc}}$, due to square wave mixing. Taking the rms value of this current into account, we have $\eta_{\max} = 2\sqrt{2}/\pi \approx 0.9$. Realistically, however, V_p is limited by the voltage headroom required to keep all the transistors in saturation. This corresponds to $V_p \approx 0.6\ V_{\text{DD}}$. The total efficiency is obtained by multiplying η by the efficiency of the matching network, given by Han and Perreault [17] as

$$\eta_m = 1 - \frac{Q_t}{Q_L} \tag{20}$$

where Q_t is the quality factor associated with the transformation, equivalent to the quality factor of the tank after accounting for the transformed impedance—the 50-*Omega* output load. Q_L is the quality factor of the inductor in the LC tank. In order to increase the efficiency of the matching network, it is advantageous to lower Q_t. In other words, lowering the quality factor of the overall network is advantageous since the overall losses are due to the power transmitted to the load. Recall from subsection C that a lower Q decreases the minimum switching time as well, permitting higher data rates. If Q_t is decreased too much however, it may lead to excessively large currents needed to obtain the maximum efficiency, requiring large transistors whose parasitics would degrade the overall performance of the transmitter. Typical values of $Q_t = 4$ and $Q_L = 12$ result in $\eta_m = 0.67$. All in all, an efficiency of around 30% to 40% is expected.

V. Circuit Design

The schematic of the ILPA is shown in Fig. 11. Designed in 65-nm CMOS technology with an ON-chip transformer, the transmitter is optimized to deliver around 1.5 mW to a 50-Ω load. The cross-coupled pair, M_3 and M_4 use a length of 60 nm and a width of 48 μm—large enough to ensure that the loop gain is sufficiently higher than 1 so that oscillations would start and to keep the voltage drop across them low, but also not so large that the parasitic gate capacitances significantly affect the resonant frequency.

The core of the ILPA is driven by a pair of complementary external LO signals, with the aid of a multiplexer selecting between the in phase or differential LO signal. The output of the multiplexer is connected to the switch M_2 in series with the current source M_1 and controls the injected current. In other words, the tail dc current is sampled at a rate equal to LO_P or LO_N. The MUX itself is driven by a pre-processed input (a control signal generated OFF-chip) corresponding to the number of polarity flips required to generate each symbol that would eventually result in the desired pattern at the output.

The injected current is a square wave with a 50% duty cycle alternating between 0 and 10 mA. This was implemented using a current source (M_1) in series with a switch (M_2). The current source transistor has a length of 100 nm to increase

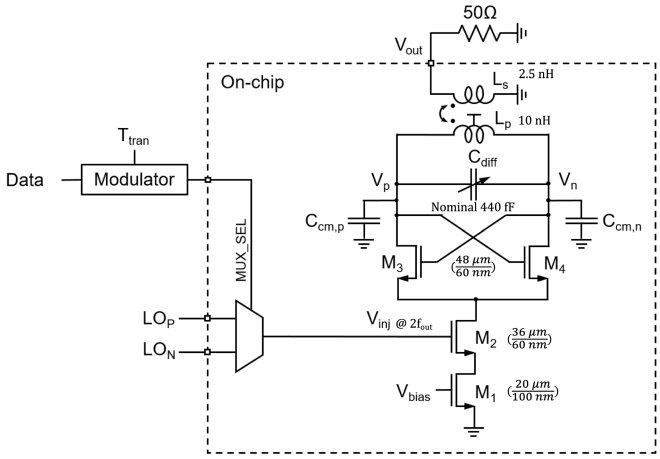


Fig. 11. Schematic of the proposed transmitter. The multiplexer and injection-locked power amplifier are ON-chip. The multiplexer selection signal is generated in software. External LOs are used as inputs.

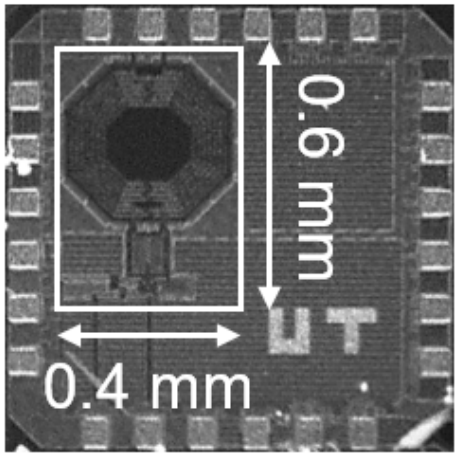


Fig. 12. Chip micrograph.

its output resistance, and a V_{eff} of 150 mV, leading to a width of 20 μm. The switch used a length of 60 nm and a width of 36 μm for a maximum V_{DS} of around 100 mV. To minimize the V_{DS} across the switch, a low-V_T device was used and the body was tied to the source to eliminate the body effect and minimize the threshold voltage. This allowed for larger voltage swing at the output for increased efficiency. The gate capacitance of the switch is driven by a 4.8-GHz signal and therefore is a significant source of power consumption in the circuit. With the current sizing, the gate capacitance is around 30 fF.

For the LC tank, a tunable digitally controlled capacitor bank was designed to target a capacitance 260 and 520 fF, with a nominal value of 440 fF for the resonant frequency of 2.4 GHz. A combination of differential and common-mode capacitors were used to shift the peak of the common-mode response away from the input frequency so that the output swing would not be too degraded.

The ON-chip transformer is a concentric transformer with an ultra-thick metal layer. The inductance of the primary (L_p) is 10 nH, while the inductance of the secondary (L_s) is 2.5 nH. The quality factors of the primary and secondary around 2.4 GHz are 12 and 4, respectively. The coupling factor between the two is 0.7.

VI. Measurements

The chip micrograph is shown in Fig. 12. The die has an area of 1 mm^2 while the active area is only 0.24 mm^2. Evidently, the majority of the active area is taken up by the transformer.

In order to obtain more practical results compared to the previous publication and better emulate an ON-chip LO, the enhanced noise generation option of the signal generator—R&S SMW200A— was used, which enabled us to generate a customized phase noise profile for the input signal. As a result, not only the corresponding output phase noise was re-measured, but also the effect of the input phase noise on the EVM and phase error were observed. A more detailed explanation of the results is given in Sections VI-A and VI-C.

The measured tuning range of the LC tank was 490 MHz (2.15–2.64 GHz) with a locking range (LR) of around 300 MHz for each resonant frequency. This value can be compared to the theoretical locking range calculated from (4). At 254 MHz, the theoretical LR is 15% less than that obtained from measurements.

To test the maximum modulation bandwidth, an Analog Signal Generator from Agilent MXG (N5183A) was used, generating a sine wave at various frequencies to flip the polarity at the input. Clearly, this does not allow for arbitrary input data sequences, as the output can only cycle from one QPSK symbol to the next. Nonetheless, it still allows for a rough estimate of the maximum data rate that could be supported. The limited bandwidth of the vector signal generator meant that it could only output a bit-stream at 50 Msym/s. Due to the oversampling required by our design, this would only allow us to test at data rates that are a fraction of this value and consequently underestimate the maximum bandwidth. Another Major drawback to shifting between consecutive symbols is the need to give each symbol enough time to fully settle. This results in a lower measured modulation bandwidth than expected.

For measurement purposes, the resonant frequency of the tank was set to 2.4 GHz and the injected signal was set to 4.4 GHz for an output frequency of 2.2 GHz.

A. Maximum Modulation Bandwidth and EVM

The modulator maintained functionality with polarity flips at a frequency of up to 360 MHz (Fig. 13), equivalent to a period of 2.8 ns, which is close to the predicted 1% settling time. At polarity flips as high as 180 MHz however, the system sustained a reasonable EVM of 5% and under. Since up to three flips at the input are required to transition between two QPSK symbols, a conservative estimate of the maximum modulation bandwidth would be (180 MHz)/3 = 60 Msymbols/s or 120 Mbit/s. It is worth mentioning that the actual upper bound on the modulation bandwidth could be higher if only the final transition needed to fully settle.

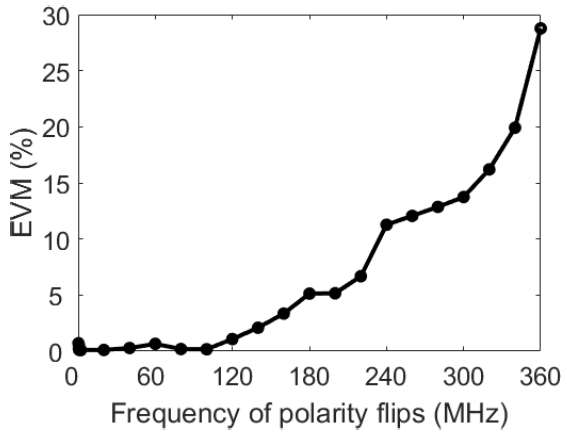
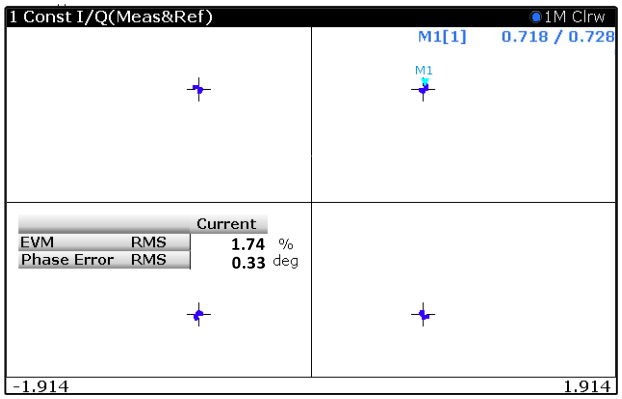
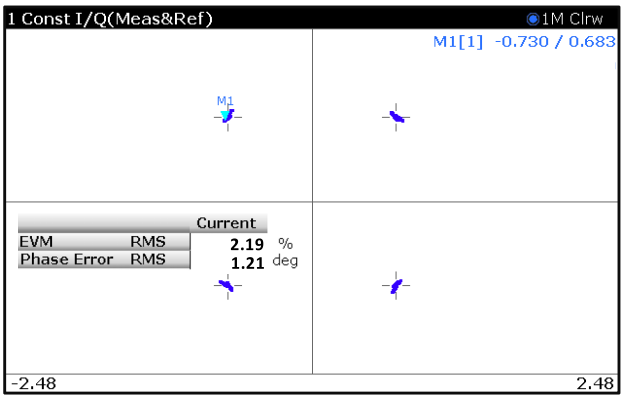


Fig. 13. EVM versus Frequency of polarity flips.



(a)



(b)

Fig. 14. Constellation diagram with polarity flips at 150 MHz using an injection source with (a) low phase noise as in [9] and (b) added phase noise of −105 dBc/Hz at 1-MHz offset.

For an ideal LO source—low phase noise as in [9]—the constellation for polarity flips at 150 MHz corresponding to an equivalent data rate of 100 Mbit/s, is shown in Fig. 14(a). The EVM at this data rate was measured to be 1.74% with 0.33° phase error.

Fig. 14(b) demonstrates the output constellation and its corresponding EVM and phase error in the presence of an added input phase noise of −105 dBc/Hz at 1-MHz offset from the carrier. The resulting EVM is 2.19% with a phase error of 1.21°.

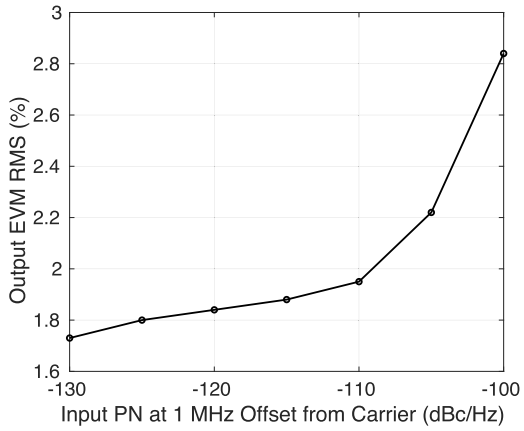


Fig. 15. Output EVM for different input phase noise profiles.

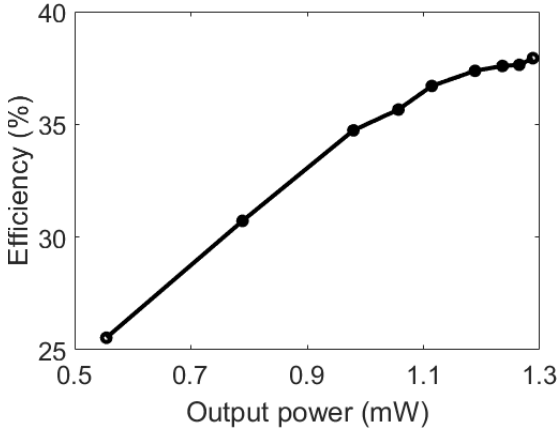


Fig. 16. Efficiency versus Output power.

The output EVM was also measured for different input phase noise profiles. At an equivalent data rate of 100 Mbit/s, in Fig. 15 the EVM is plotted against different values of the input phase noise at 1-MHz offset from the carrier. As is evident from the measurement results, an input phase noise within a reasonable range and comparable to that of similar work does not drastically deteriorate the EVM and phase error.

B. Efficiency

The ILPA achieved a maximum efficiency of 38% while delivering 1.3 mW to the load. Fig. 16 demonstrates the efficiency of the ILPA versus its output power. The divider itself consumed 3 mW, while the digital power consumption—multiplexer, input buffer—was 0.4 mW. Note that this does not include the LO generation power as it was fed from an external source.

It is worth noting, however, that a conservative estimate for the FoM[1] of the ON-chip LO, assuming an LO generation power similar to [22] and a phase noise of −105 dBc/Hz at 1-MHZ offset, is equal to 178.23 dBc/Hz. Nonetheless, the

[1]from [23].

TABLE I
COMPARISON TABLE

		[4]	[19]	[20]	[6]	[21]	[18]	This work
Frequency (GHz)		2.9-4.0	2.4	0.401-0.406	0.9	2.4	0.401-0.428	2.4
Modulation		QPSK	HS-OQPSK	QPSK	QPSK/ 16-QAM	GMFSK	QPSK	QPSK
Technology		65 nm	65 nm	180 nm	65 nm	65 nm	130 nm	65 nm
Active Area (mm^2)		0.52	0.39	0.04	0.08	0.85	0.643	0.24
Supply (V)		1.2	0.3-0.7	1.2	1.2/0.77	1.0	1.0	1.2
Output power (dBm)		N/A	0 / 6	-10.8	-9 / -15	-6	-13	+1
Power (mw)	PA	Total: 5	Total: 4.4 @ 0dBm	Total: 0.425	Total: 2/1.3 (w/o BS)	1.6	0.77	3.4
	LO					1	2.88	-
	Driver					0.2	0.43	0.4
Data rate (Mbit/s)		20	N/A	0.06	50 / 100	N/A	11	100
Energy/bit (nJ/bit)		0.25	N/A	7.01	0.02 (w/o BS) 0.033 (w/ BS)	N/A	0.37	0.045*
EVM (%)		1.58	2.29	N/A	5.28	N/A	4.9	2.22**
Phase noise at 1 MHz offset (dBc/Hz)		-110	-117	-95	-100	N/A	-100 (SIL)/ -91 ($\Delta\Sigma$IL)	-111**

* Assuming an LO generation power of 1.1 mW as [22].
** Measured with an input phase noise of -105 dBc/Hz at 1 MHz offset from the carrier.

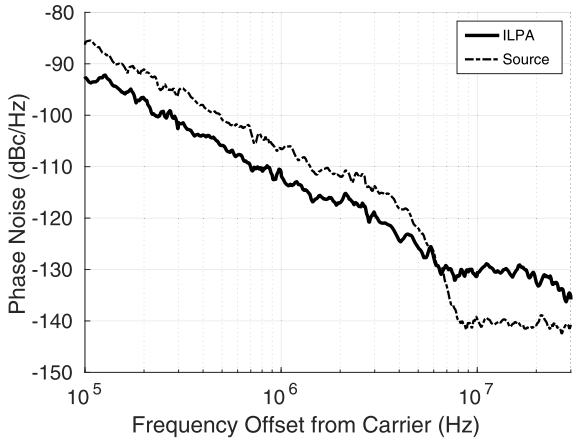


Fig. 17. Phase noise of the ILPA (locked at 2.42 GHz) and the injection source (at 4.84 GHz). Intrinsic frequency of the ILPA is 2.4 GHz.

measurement results below, still demonstrate low EVM and high efficiency amid a less than perfect 178 dBc/Hz FoM.

C. Phase Noise

One of the advantages of an injection locked system is its phase noise performance. Under locked conditions, the output phase noise is mainly determined by the phase noise of the injection signal.

In the case of an injection-locked frequency divider and for a divide-by-two operation, at frequencies close to the carrier the output phase noise follows that of the locking source by 6 dB [24].

Using the enhanced noise generation option of the signal generator, several phase noise profiles were created, one of which is plotted in Fig. 17 with its corresponding output phase noise. The output phase noise follows 6 dB below that of the injection source up to 5 MHz offset from the carrier, where the input phase noise starts to drop due to the limited bandwidth of the noise source generator. Above 5 MHz, the output phase noise of ILPA eventually flattens due to the presence of other noise sources (e.g. jitter introduced by the clock buffers and the output load)."

VII. CONCLUSION

In this article, an OQPSK RF front-end TX based on an injection-locked power amplifier was presented. The circuit was designed in 65-nm CMOS technology. The PA was merged with an injection-locked LC divider by using an integrated transformer to couple to the antenna. The measurement results are summarized in Table I. Compared to the state of the art, this design attains higher data rates, while also consuming significantly lower power and achieving low EVM. Centered around 2.4 GHz, it delivered up to 1.3 mW of output power with a maximum data rate of 120 Mbit/s. The EVM was 2.22% at an equivalent data rate of 100 Mbit/s.

APPENDIX

A. Settling Time Derivation

Let ϕ_{in} be the phase offset of the input signal and ϕ the phase offset of the output signal at steady state. Let us show that taking the derivative of the phase difference between input and output at steady-state as a function of frequency would lead to an approximate value for the characteristic time constant of the phase settling. Let $v_{\text{in}}(t) = \cos(2\omega t + \phi_{\text{in}})$ and $v_{\text{out}}(t) = \cos(\omega t + \phi)$. When the input phase is zero at time instance $t = -\phi_{\text{in}}/2\omega$, the output phase is at $\phi - \phi_{\text{in}}/2$. Thus, $\phi_o = \phi - \phi_{\text{in}}/2$ is the steady-state phase difference between the input and output, describing the phase required at the output according to Barkhausen's criteria to maintain oscillations. For a given phase difference, the output instantaneous frequency

that would sustain oscillations can also be found

$$\phi_o(\omega_i(t)) = \phi(t) - \frac{\phi_{\text{in}}(t)}{2} \tag{21}$$

$$\phi_o\left(\omega_{\text{out}} + \frac{d\phi}{dt}\right) = \phi(t) - \frac{\phi_{\text{in}}(t)}{2}. \tag{22}$$

By linearizing ϕ_o about ω_{out}, we have

$$\phi_o(\omega_{\text{out}}) + \left(\frac{d\phi_o}{d\omega}\bigg|_{\omega=\omega_{\text{out}}}\right)\frac{d\phi}{dt} = \phi_{\text{out}}(t) - \frac{\phi_{\text{in}}(t)}{2}. \tag{23}$$

Let the difference between the output phase and its steady state be $\Delta\phi(t) = \phi(t) - \phi_o(\omega_{\text{out}})$. Since $\phi_o(\omega_{\text{out}})$ does not depend on time, we can assume $(d\Delta\phi/dt) = (d\phi/dt)$. The former expression can be written as

$$\frac{d\Delta\phi}{dt} = -\frac{1}{\tau}\left(\Delta\phi_t - \frac{\phi_{\text{in}}(t)}{2}\right) \tag{24}$$

where

$$\tau = -\frac{d\phi_o}{d\omega} \tag{25}$$

is the characteristic time constant of the settling. Class B biasing of the input transistor, leads to an output phase equal to the phase shift introduced by the LC tank if it is between $-45°$ and $+45°$, assuming hard mixing. This is because if the output phase satisfies this condition, the current entering the tank will be in phase with the injected current

$$\phi_o(\omega) = \beta(\omega) = -\tan^{-1}\left(2Q\frac{\omega-\omega_o}{\omega_o}\right) = -\tan^{-1}\left(2Q\frac{\Delta\omega}{\omega_o}\right). \tag{26}$$

Therefore, by applying previous results, the final expression for the time constant is the following:

$$\tau = \frac{2Q}{\omega_o}\frac{1}{1+\left(2Q\frac{\Delta\omega}{\omega_o}\right)^2} \tag{27}$$

REFERENCES

[1] S. Pasupathy, "Minimum shift keying: A spectrally efficient modulation," *IEEE Commun. Mag.*, vol. 17, no. 4, pp. 14–22, Jul. 1979.

[2] Y.-H. Liu, C.-L. Li, and T.-H. Lin, "A 200-pJ/b MUX-based RF transmitter for implantable multichannel neural recording," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 10, pp. 2533–2541, Oct. 2009.

[3] S. Diao *et al.*, "A 50-Mb/s CMOS QPSK/O-QPSK transmitter employing injection locking for direct modulation," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 120–130, Jan. 2012.

[4] G. Marzin, S. Levantino, C. Samori, and A. L. Lacaita, "A 20 Mb/s phase modulator based on a 3.6 GHz digital PLL with-36 dB EVM at 5 mW power," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 2974–2988, Dec. 2012.

[5] H. A. Shawkey, G. H. Ibrahim, M. A. Elmala, and D. A. El-Dib, "Low power QPSK RF transmitter for 405–406 MHz MEDS band," *Int. J. Elect. Comput. Sci.*, vol. 14, no. 3, pp. 36–41, Jun. 2014.

[6] X. Liu, M. M. Izad, L. Yao, and C.-H. Heng, "A 13 pJ/bit 900 MHz QPSK/16-QAM band shaped transmitter based on injection locking and digital PA for biomedical applications," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2408–2421, Nov. 2014.

[7] Y.-H. Liu and T.-H. Lin, "A 3.5-mW 15-mbps O-QPSK transmitter for real-time wireless medical imaging applications," in *Proc. IEEE Custom Integr. Circuits Conf.*, Sep. 2008, pp. 599–602.

[8] K.-H. Teng, T. Wu, X. Liu, Z. Yang, and C.-H. Heng, "A 400 MHz wireless neural signal processing IC with 625×on-chip data reduction and reconfigurable BFSK/QPSK transmitter based on sequential injection locking," *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 3, pp. 547–557, Jun. 2017.

[9] Z. Ji, S. Zargham, and A. Liscidini, "Low-power QPSK transmitter based on an injection-locked power amplifier," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp. 134–137.

[10] B. Hong and A. Hajimiri, "A general theory of injection locking and pulling in electrical oscillators—Part I: Time-synchronous modeling and injection waveform design," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2109–2121, Aug. 2019.

[11] B. Hong and A. Hajimiri, "A general theory of injection locking and pulling in electrical oscillators—Part II: Amplitude modulation in *LC* oscillators, transient behavior, and frequency division," *IEEE J. Solid-State Circuits*, vol. 54, no. 8, pp. 2122–2139, Aug. 2019.

[12] A. Mazzanti, P. Uggetti, and F. Svelto, "Analysis and design of injection-locked LC dividers for quadrature generation," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1425–1433, Sep. 2004.

[13] S. L. J. Gierkink, S. Levantino, R. C. Frye, C. Samori, and V. Boccuzzi, "A low-phase-noise 5-GHz CMOS quadrature VCO using super-harmonic coupling," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1148–1154, Jul. 2003.

[14] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[15] R. Adler, "A study of locking phenomena in oscillators," *Proc. IEEE*, vol. 61, no. 10, pp. 1380–1385, Oct. 1973.

[16] A. Mirzaei, M. E. Heidari, R. Bagheri, S. Chehrazi, and A. A. Abidi, "The quadrature LC oscillator: A complete portrait based on injection locking," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1916–1932, Sep. 2007.

[17] Y. Han and D. J. Perreault, "Analysis and design of high efficiency matching networks," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1484–1491, Sep. 2006.

[18] K.-H. Teng and C.-H. Heng, "A 370-pJ/b multichannel BFSK/QPSK transmitter using injection-locked fractional-N synthesizer for wireless biotelemetry devices," *IEEE J. Solid-State Circuits*, vol. 52, no. 3, pp. 867–880, Mar. 2017.

[19] X. Peng, J. Yin, P.-I. Mak, W.-H. Yu, and R. P. Martins, "A 2.4-GHz ZigBee transmitter using a function-reuse class-F DCO-PA and an ADPLL achieving 22.6% (14.5%) system efficiency at 6-dBm (0-dBm) P_{out}," *IEEE J. Solid-State Circuits*, vol. 52, no. 6, pp. 1495–1508, Jun. 2017.

[20] A. R. Gundla and T. Chen, "An efficient multi channel, 425 μW QPSK transmitter with tuning for process variation in the medical implantable communications service (MICS) band of 402–405 MHz," in *Proc. IFIP/IEEE Int. Conf. Very Large Scale Integr. (VLSI-SoC)*, Tallinn, Estonia, Sep. 2016, pp. 1–5.

[21] Z. Sun *et al.*, "A 0.85 mm^2 BLE transceiver with embedded T/R switch, 2.6 mW fully-passive harmonic suppressed transmitter and 2.3 mW hybrid-loop receiver," in *Proc. IEEE 44th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2018, pp. 310–313.

[22] J. Prummel *et al.*, "A 10 mW Bluetooth low-energy transceiver with on-chip matching," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 3077–3088, Dec. 2015.

[23] M. Garampazzi *et al.*, "An intuitive analysis of phase noise fundamental limits suitable for benchmarking LC oscillators," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 635–645, Mar. 2014.

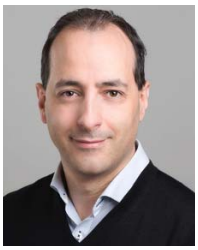
[24] J. Lee and H. Wang, "Study of subharmonically injection-locked PLLs," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

Saba Zargham (Member, IEEE) was born in Toronto, ON, Canada, in 1992. She received the B.Sc. degree in electrical engineering from the Sharif University of Technology, in 2016, and the M.A.Sc. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2020.

Her research was mainly focused on CMOS RF integrated circuits for wireless communications and RF front-end design with a particular interest in using injection locked dividers for phase modulation and low-power wireless transmitters. She is currently an Analog Design Engineer with Synopsys.

Ms. Zargham was the recipient of the Best Student Paper Award in IEEE ESSCIRC, 2018.

Zexi Ji received the B.A.Sc. degree in engineering science (major in electrical and computer engineering) from the University of Toronto, Toronto, ON, Canada, in 2016, and the M.S. degree in electrical engineering and computer science from MIT, in 2018, where he is currently pursuing the Ph.D. degree in electrical engineering and computer science, with a focus on hardware accelerators for machine learning applications.



Antonio Liscidini (Senior Member, IEEE) was born in Tirano, Italy, in 1977. He received the Laurea *(summa cum laude)* and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was a summer Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, studying poly phase filters and CMOS low-noise amplifiers. From 2008 to 2012, he was an Assistant Professor with the University of Pavia, and a Consultant with Marvell Semiconductors, Pavia, in the area of integrated circuit design. In 2012, he moved to the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently an Associate professor. In 2019, he has become Consultant for Huawei Technology Group in the area of RFIC for optical communication. His research interests are focused on analog mixed signal interfaces with particular emphasis on the implementations of transceivers and frequency synthesizers for wireless-wireline communication and ultralow power applications.

Dr. Liscidini has been a member of the ISSCC TPC from 2012 to 2017, the ESSCIRC TPC from 2010 to 2018, and the CICC TPC from 2019 to currently. He was a recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits, and a co-recipient of the Best Invited Paper Award at the 2011 IEEE CICC and the Best Student Paper Award at the 2018 IEEE ESSCIRC. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2008 to 2011 and from 2017 to 2018 and as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2013 and 2016 and a Guest Editor of the IEEE RFIC VIRTUAL JOURNAL in 2018. From 2016 to 2018, he has been a Distinguished Lecturer of the IEEE Solid-State Circuits Society.