A Digital Filtering ADC With Programmable Blocker Cancellation for Wireless Receivers

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***Abstract*— This paper presents a long-term evolution (LTE) receiver (RX) front end with a digital filtering analog to digital converter (ADC) in the baseband to perform multi-band blocker cancellation. The digital filtering ADC has a digitally defined transfer function that is highly reconfigurable and insensitive to PVT variations. The dynamic range requirement of the blocker cancellation feedback digital to analog converter (DAC) is relaxed with a trivial uncalibrated first-order passive high-pass filter. The programmable digital filter provides 34.9-dB attenuation of transmitter leakage and variable attenuation of an additional blocker anywhere in the frequency range 17.5–107.5 MHz. A blocker detection algorithm for this RX is presented and takes approximately 26 μs to converge. The RX front end operates at 1.8 GHz with a noise figure of 3.9 dB and IIP3 of −5 dBm, and consumes only 20.4–37.5 mW, the lowest among the state-of-the-art designs.**

***Index Terms*— Analog to digital converter (ADC), baseband, blocker, digital, digital to analog converter (DAC), filtering, long-term evolution (LTE), reconfigurable, wireless receiver (RX).**

I. Introduction and Background

LOW supply voltages and analog gain in nanoscale CMOS make the design of a RF receiver (RX) very challenging. One of the most difficult requirements is to reject signals in frequency bands adjacent to the channel of interest (blockers), whose amplitude is much larger than the in-band signal.

Traditionally, an analog low pass filter (LPF) is used before the analog to digital converter (ADC) in the baseband to provide blocker filtering, as shown in Fig. 1. To improve power efficiency, the LPF and ADC can be combined into a global feedback loop thus creating an analog filtering ADC. There are two approaches to designing an analog filtering ADC. The first embeds the analog filter inside the feedback loop of the ADC, thus relaxing the filter's noise and distortion requirements [1], [2]. The second approach moves the ADC inside the feedback loop of the analog filter, relaxing the ADC thermal and quantization noise requirements [3]–[6].

Seeking the benefits of a more digital implementation, ADCs with digitally improved blocker rejection were proposed in [7] and [8], where a digital filter is incorporated within a feedback loop around the ADC to enhance the signal transfer function (STF) roll-off of a third-order continuous-time $\Delta\Sigma$ modulator (CTDSM). The inclusion of the digital filter increased the blocker attenuation by 6 dB and also reduced the requirements on the first integrator. Although this approach gives the impression of a more digital and flexible implementation, the filter transfer function is still determined by the poles of the analog circuitry hence limiting filter selectivity and requiring accurate calibration and PVT correction.

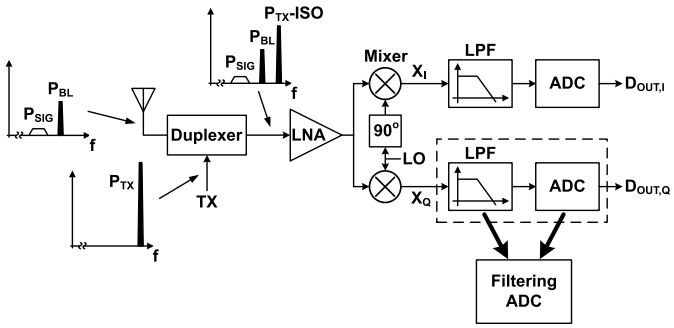

Fig. 1. Block diagram of a typical wireless RX, with a TX and a duplexer to illustrate the blocker profile.

This paper presents a digital filtering ADC, which has a digitally defined transfer function that is highly reconfigurable and completely insensitive to PVT variations [9]. The digital blocker cancellation path provides a maximum blocker attenuation of 34.9 dB. Noise and distortion introduced in the blocker cancellation feedback digital to analog converter (DAC) are high-pass filtered with a trivial uncalibrated first-order passive network. As a result, the analog baseband circuitry consists only of the first-order CTDSM, a feedback DAC with relaxed specifications, plus a few passive components that do not require tuning. The resulting RX is low-power and well-suited for implementation in CMOS technologies at 28 nm and beyond.

II. Baseband Digital Filtering ADC

The specification of a wireless RX based on transmitter (TX) leakage and blocker power is shown in Fig. 2. The sensitivity test and blocking test are worst case scenarios for a wireless RX, where the desired signal is very small and the TX leakage and blocker power are high. However, a more common scenario is in the bottom left corner, where the TX leakage and blocker power are moderate. Designing a wireless

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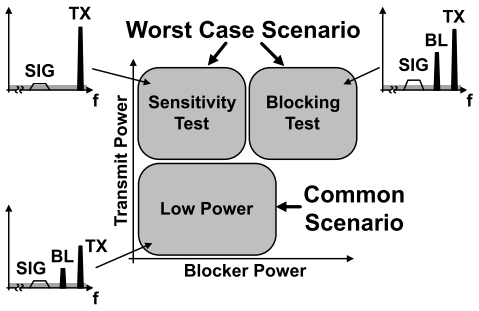

Fig. 2. Specification of a wireless RX, based on TX leakage and blocker power.

RX working in this region is trivial. A typical wireless RX is designed to work in the worst case scenarios. In this paper, we are targeting a highly reconfigurable RX that works in the worst case scenarios, but can also take advantage of the common scenario to save power.

Typically, the biggest blocker comes from the local TX. For example, in the long-term evolution (LTE) standard, TX leakage can be as high as −30 dBm at the RX front end assuming a TX–RX isolation of 57 dB and TX-antenna insertion loss of 2 dB [10]. Fortunately, TX leakage appears at a known frequency offset—a minimum of 41 MHz in band 20. Additionally, one other blocker (or two in an IMD test) may be present, as shown in Fig. 1.

A starting point for the digital filtering ADC is shown in Fig. 3(a), where a digital low-pass filter is placed after the ADC to attenuate the blockers. However, the ADC needs to have a high dynamic range, because it needs to handle the large blocker without saturating. A digital high-pass filter (HPF) in feedback, in combination with a DAC, can be used to reconstruct the blocker and cancel it at the summing node in front of the ADC [see Fig. 3(b)]. As a result, the ADC's dynamic range requirement is reduced. However in this case, at high frequency, the digital filter gain never rolls off, and the phase shift contributed by the ADC and the digital filter becomes significant; hence, the feedback loop becomes unstable. To make the loop stable, high-frequency loop gain can be reduced by replacing the digital HPF with a digital bandpass filter [see Fig. 3(c)]. Blockers are still canceled within the bandwidth of the digital bandpass filter. In the case where more than one blocker is present, multiple bandpass filters can be placed in parallel [see Fig. 3(d)], each responsible for one blocker. The proposed digital filtering ADC is easily reconfigurable, and the digital filters can be turned off when there are no blockers to save power.

A second-order digital bandpass filter in feedback is used which makes the closed loop response a second-order notch filter. The resulting closed-loop magnitude response for notch filters with different center frequencies is plotted in Fig. 4(a). They all have the same Q factor of 24, and the peak attenuation is adjusted such that the gain at the signal band edge, B, is −1 dB. Assuming that there is only one blocker present, and the center frequency of the notch can be placed exactly at the blocker frequency, the effective attenuation of the second-order notch filter is plotted for continuous wave (CW) blockers

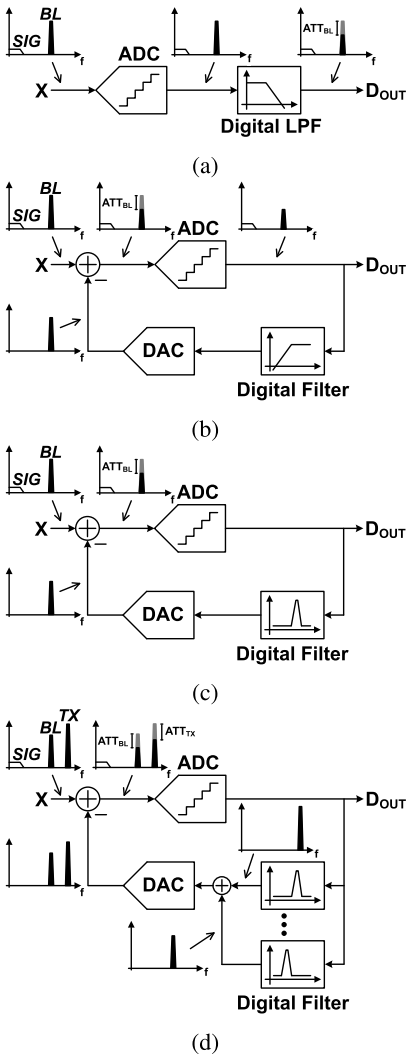

Fig. 3. Block diagram of a digital filtering ADC with (a) low pass filter after the ADC, (b) HPF in feedback, (c) bandpass filter in feedback, and (d) multiple bandpass filters in feedback.

and modulated blockers in Fig. 4(b). The attenuation of the modulated blocker is calculated based on the average attenuation over a bandwidth of $B/2$. It can be seen that the second-order notch filter provides much more attenuation of nearby narrowband CW blockers than a fourth-order Butterworth filter, and an attenuation of modulated blockers similar to a third-order Butterworth filter.

The baseband architecture with digital multi-band blocker cancellation is shown in Fig. 5. The baseband circuitry receives a current-mode signal comprised of the in-band signal (SIG), TX leakage, and an additional blocker (BL). A digital bandpass filter extracts the TX leakage at its known frequency offset, while a programmable digital bandpass filter can be used to track another blocker. The programmable filter can be set to reject blockers at any frequency offset in the range 17.5–107.5 MHz under the control of a blocker detection algorithm. The DAC converts the summed digital filter outputs to an analog current.

The DAC requires sufficient DR to cancel full-scale TX leakage and blockers while contributing minimal noise in

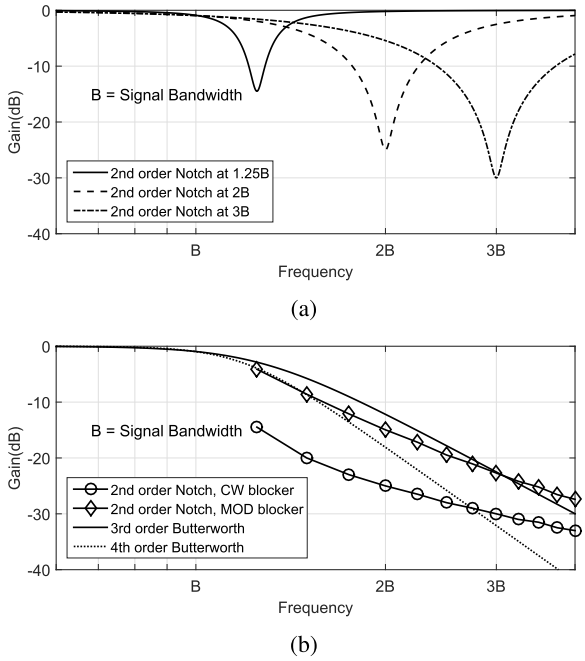

Fig. 4. (a) Simulated transfer function of the second-order notch filters at different center frequencies with $Q = 24$. (b) Attenuation of the second-order notch filters for a CW blocker and a modulated blocker, compared with third- and fourth-order Butterworth filter.

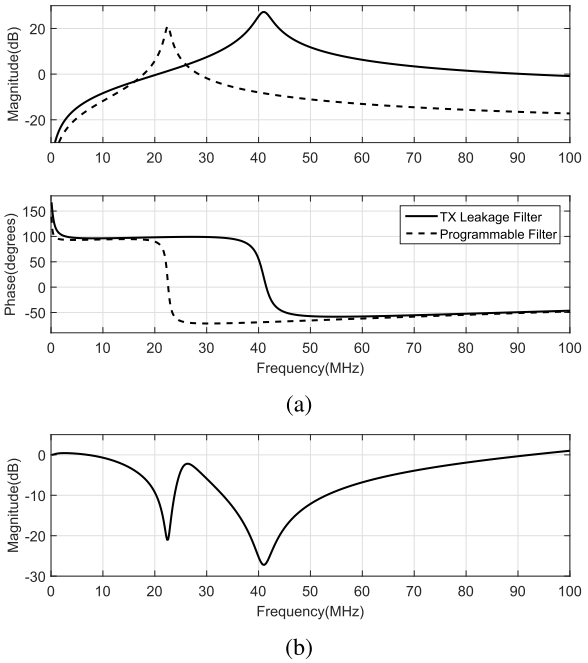

Fig. 6. Simulated transfer function of (a) digital bandpass filters for TX leakage and additional blocker and (b) closed loop transfer function.

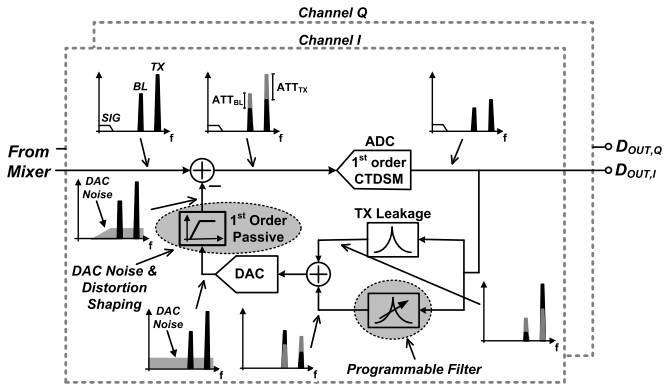

Fig. 5. Baseband signal flow with digital multi-band blocker cancellation.

the signal band. Here, recognizing that the DAC is used to replicate blockers and does not have any signal content in the band of interest, the first-order passive HPF is placed at the DAC output to reduce in-band thermal noise, quantization noise, and distortion from the DAC. Hence, in this paper, a 5-bit DAC provides 34.9-dB blocker attenuation and its DR is not a limiting factor. Only the first-order CTDSM ADC is needed in the main signal path because most of the blocker power is already canceled by the digital path and DAC.

Fig. 6(a) shows the simulated transfer function of the implemented digital bandpass filters programmed to cancel a blocker at 22.5 MHz and the TX leakage at 41 MHz. The closed loop transfer function is shown in Fig. 6(b). The delays from the ADC and the digital logic translate to an increasing phase shift versus frequency. As a result, the loop phase margin will get worse as the center frequency of the digital bandpass filter increases. Therefore, the maximum center frequency of the programmable filter is limited to 107.5 MHz. The center frequency could be increased further by decreasing the filter gain (providing less blocker attenuation) or increasing the filter Q factor.

An architecture similar to Fig. 3(c) was first proposed in [8], with two differences. First, the digital bandpass filter in [8] was used to assist the STF roll-off of a third-order CTDSM and increased blocker suppression by 6 dB. Since the filter transfer function still relies on the poles of the analog path, accurate calibration and PVT correction are needed. In this paper, the filter transfer function depends entirely on the digital bandpass filter which is very accurate. Second, without the first-order passive HPF at the DAC output, the dynamic range required of the DAC in [8] was very high. In addition to the consequently low thermal noise and distortion requirements on the DAC, in the presence of strong blockers, DAC clock jitter in [8] will contribute significant noise in the signal band. Moreover, to mitigate the quantization noise from the DAC, an off-chip reconstruction filter that matches the transfer function of the analog path was needed in [8].

III. Baseband Blocker Detection

In this section, a blocker detection algorithm that tracks the blocker location in real time is proposed allowing the RX to adapt to changing channel conditions. There are two requirements for the blocker detection algorithm. First, the time required for blocker detection must be much smaller than the rate of change in the channel conditions. Second, the blocker frequency needs to be accurately detected as any uncertainty in the blocker frequency will lower the effective blocker attenuation due to the filter's high Q factor.

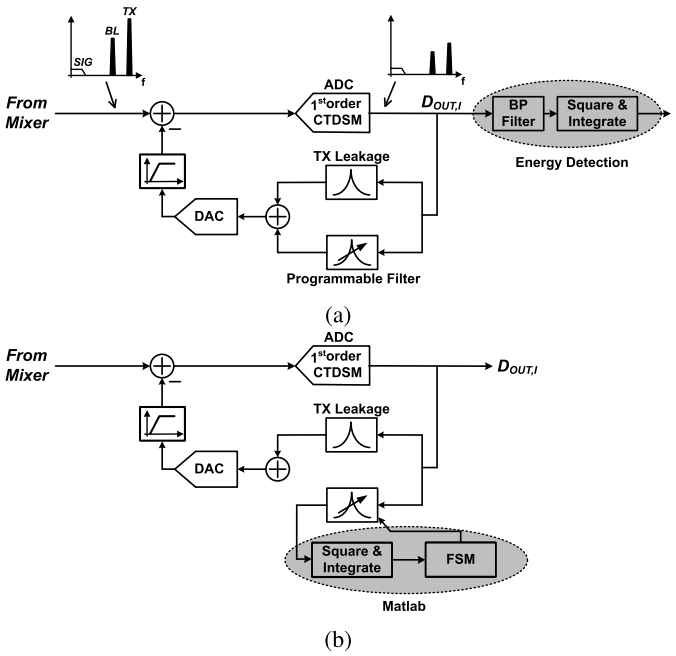

Fig. 7. Block diagram of (a) narrowband spectrum sensing (b) implemented blocker detection with programmable digital filter reused.

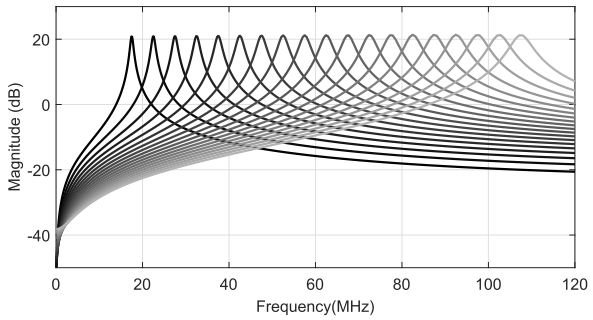

Fig. 8. Simulated magnitude responses for the swept programmable digital bandpass filter.

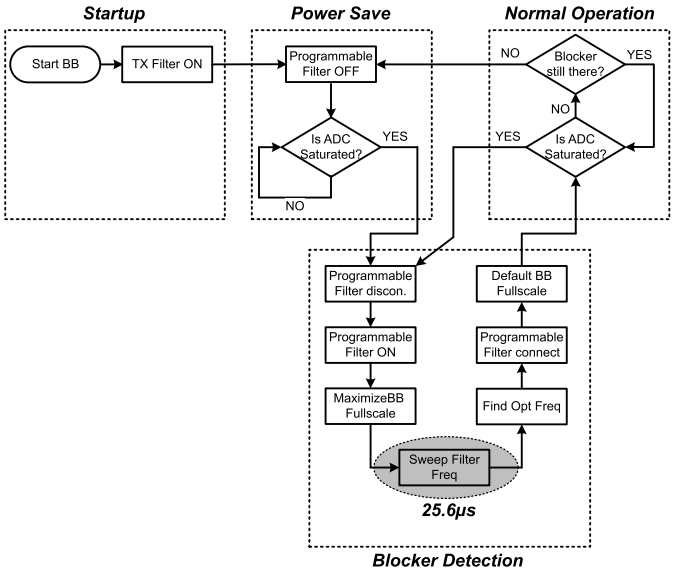

Fig. 9. FSM of the blocker detection algorithm.

To compensate the rapid and significant variations in the channel conditions, the LTE standard provides an automatic repeat request (ARQ) [11]. In an ARQ scheme, for every block of data 1 ms in length, the RX relies on error detection to detect uncorrectable errors. If uncorrectable errors exist, the RX can ask for the TX to retransmit the same information. The block with errors is preserved and combined with the retransmitted block to increase the effective SNR. In this paper, the block length of 1 ms is assumed to be the maximum time allowable for the blocker detection algorithm.

Blocker detection can be considered as a spectrum sensing problem, where the spectrum at the ADC output needs to be sensed and the frequency of the largest blockers needs to be detected. A popular narrowband spectrum sensing algorithm in cognitive radio networks is energy detection [12], as shown in Fig. 7(a). A bandpass filter followed by a square and integrate block is used to calculate the total power in the narrowband that is defined by the bandpass filter. It has the advantage of lower implementation and computational complexity compared to other narrowband spectrum sensing techniques [12]. If the center frequency of the bandpass filter is swept, wideband spectrum sensing is achieved. The block diagram for blocker detection mode is shown in Fig. 7(b) where the programmable digital bandpass filter is disconnected from the main loop and reused for energy detection. Therefore, the only extra hardware is the square and integrate block and the finite state machine (FSM) which is implemented off-chip in MATLAB for this prototype. If implemented on-chip, this additional digital logic will increase the total digital circuit area by 15%.

The programmable digital bandpass filter is swept over the frequency range from 17.5 to 107.5 MHz and the simulated magnitude responses are shown in Fig. 8. The Q factor of the filter is 24. For each frequency setting, the digital filter starts in the reset state, and runs for 400 samples to obtain an accurate power estimate.

The state diagram of the blocker detection algorithm is shown in Fig. 9. The baseband starts in the initial state, where the bandpass filter responsible for the TX leakage is turned on. Note that for LTE, the TX leakage appears at a known frequency offset, and no blocker detection is needed for the TX leakage. The next state is the power save state, where the programmable filter is turned off and the ADC output is continuously monitored to detect saturation from a new blocker. When the ADC is saturated, the probability of the maximum code and minimum code at the quantizer output (for a 17-level quantizer, it would be $+8$ and -8) increases significantly. The ADC saturation criteria are implemented by monitoring the number of $+8$ and -8 outputs from the quantizer within every 400 samples.

In the case where the ADC saturates, it means that a blocker is present and the blocker detection algorithm starts. First, the baseband full scale is maximized to bring the ADC out of saturation, with a small noise penalty. The center frequency of the bandpass filter is swept in 1 MHz increments from 17.5 to 107.5 MHz, taking a total of 36 400 samples which translate

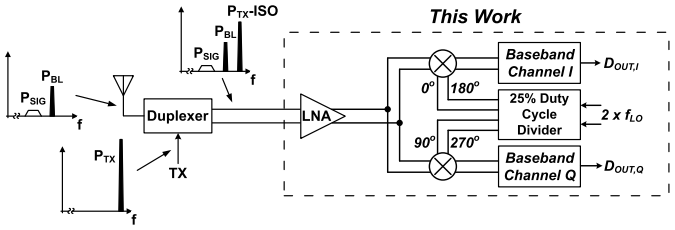

Fig. 10. Top-level block diagram of the proposed wireless RX, with a TX and a duplexer to illustrate the blocker profile.

to 50.6 μs at an ADC sampling frequency of 720 MHz. The algorithm time can be cut in half to 25.6 μs by using both the I and Q channels of the baseband, since they see the same channel conditions. The frequency setting with the most power is the blocker frequency and the programmable digital filter is programmed to that setting and connected to the main feedback loop to cancel the blocker. The total blocker detection algorithm takes approximately 26 μs and it is dominated by the filter frequency sweep time. Note that this time is much less than the transport block size of 1 ms in LTE. After the blocker is detected and canceled, the baseband goes into normal operation, where the ADC output is continuously monitored in case the blocker frequency changes. The blocker power is also monitored at the output of the programmable filter to ensure that the baseband goes into power save mode when the blocker disappears.

IV. Circuit Implementations

The top-level block diagram of the proposed wireless RX prototype is shown in Fig. 10. An RF front end is designed and included to test the blocker cancellation of the baseband in a realistic scenario. The low input-referred noise of this baseband permits a simplified and low-power low-noise amplifier (LNA) design. A common-gate LNA with a differential input impedance of 50 Ω is used, as shown in Fig. 11(a). To improve its transconductance, the NMOS input pair is capacitively cross-coupled [13], and the differential input is also fed into the gate of the PMOS input pair. The LNA output impedance is improved with cascode NMOS and PMOS devices. The off-chip balun, which provides the single-ended to differential conversion, is also used to provide the dc bias current to the LNA input. The I and Q current-mode passive mixers are driven by a 25% duty cycle divider that consists of two latches [14] [see Fig. 11(b)]. The divider outputs 75% duty cycle clock phases which are converted to 25% duty cycle clocks by an inverter. A 50% duty cycle clock at twice the local oscillator (LO) frequency is provided to the divider from off-chip.

Fig. 12 shows the detailed baseband circuit design. Since the mixer outputs a current mode signal, the first-order passive low-pass filter with 20-MHz cutoff frequency is realized simply by R_0 and C_0. The passive low-pass filter acts as an anti-aliasing filter and also provides some attenuation of out-of-band blockers. The voltage swings at the mixer output $I_{\mathrm{IN},I}$ and $I_{\mathrm{IN},Q}$ are determined by the product of the mixer output current and R_0. Therefore, a small R_0 (100 Ω) is

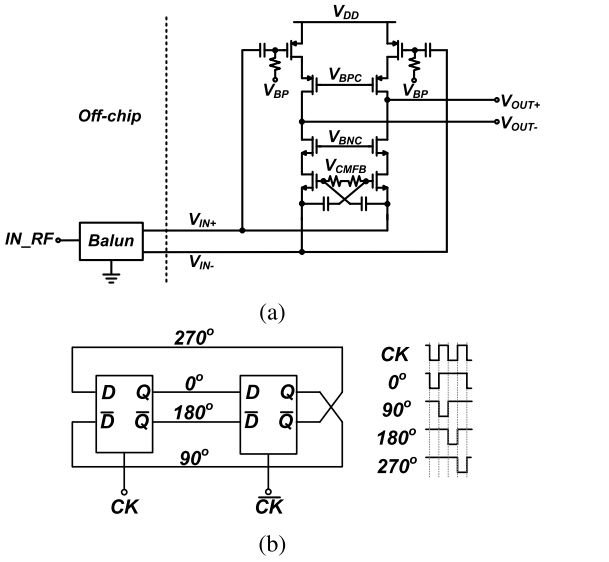

Fig. 11. RF front-end building blocks. (a) LNA implementation. (b) 25% duty cycle divider.

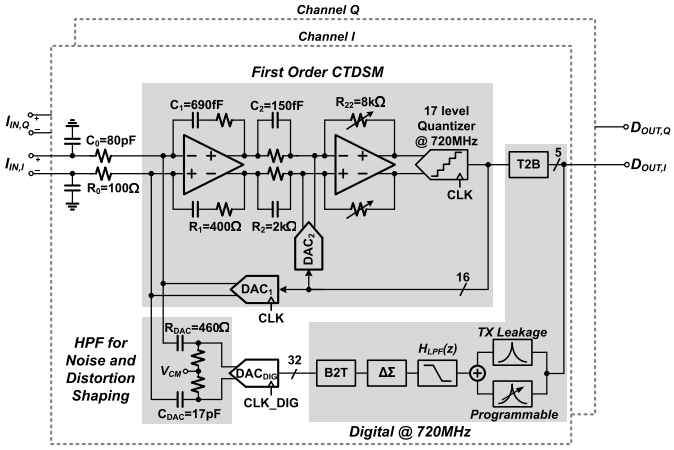

Fig. 12. Baseband circuit design with the first-order CTDSM, digital circuit, and HPF highlighted.

used to improve the mixer linearity. However, the small series impedance formed by R_0 and C_0 increases the noise contribution of the first amplifier. The first operational amplifier is the integrator while the second operational amplifier acts as a variable gain amplifier (VGA) and allows for excess loop delay compensation with DAC_2 [15]. A zero is added by introducing C_2 to extend the bandwidth of the VGA. Otherwise, the phase shift of the VGA will cause peaking in the noise transfer function. The baseband has an input bandwidth of 9 MHz (consistent with LTE20) with the quantizer clocked at 720 MHz yielding an oversampling ratio of 40. The quantizer has 17 levels to ensure acceptable levels of quantization noise and sensitivity to clock jitter. Since this baseband has a relatively few gain stages (2) compared to traditional RX designs, pre-amplifiers precede the quantizer comparators to reduce their input-referred noise and mismatch.

The detailed digital feedback filter implementation running at 720 MHz is shown in Fig. 13. The 16-bit thermometer coded

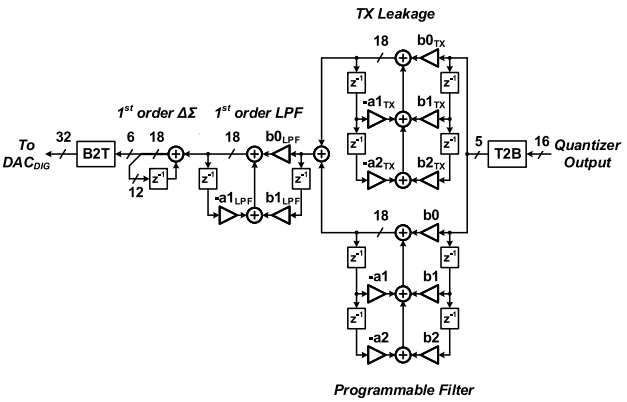

Fig. 13. Detailed digital circuit implementation.

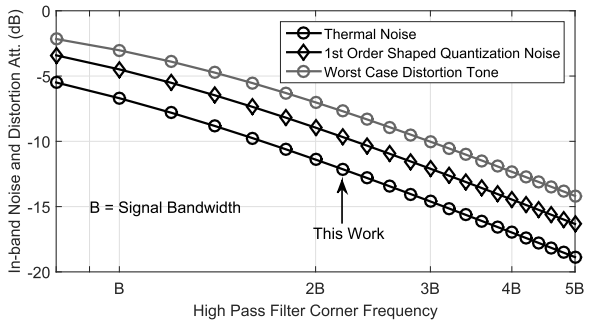

Fig. 14. Simulated DAC in-band noise and distortion suppression as a function of HPF corner frequency.

quantizer output is first converted to a 5-bit binary code with a thermometer to binary decoder (T2B) which is implemented using Wallace tree adders. Two digital second-order infinite impulse response (IIR) filters with 9-bit coefficient resolution detect and cancel TX leakage and one additional blocker. Note that in an intermodulation test, where TX leakage plus two additional blockers are present, canceling the TX leakage and the blocker at lower offset frequency is sufficient to reduce the intermodulation product significantly. The fully programmable coefficients allow accurate adjustment of the filter center frequency, gain, and Q factor to effectively cancel blockers at different frequencies, power levels, and modulation bandwidth. The output of both IIR filters is rounded to 18 bits to achieve a balance between hardware complexity and rounding error. The result is further truncated to 6 bits at the input of the binary to thermometer encoder (B2T) where the resulting quantization noise is shaped by the first-order delay-less digital $\Delta\Sigma$ modulator.

The output noise and distortion from $\mathrm{DAC_{DIG}}$ are shaped further by the first-order passive HPF created by R_{DAC} and C_{DAC}. The value of R_{DAC} is chosen to be much larger than R_0 to minimize the effects of the HPF on the feedback factor of the first amplifier. Fig. 14 shows the simulated DAC in-band noise and distortion suppression as a function of HPF corner frequency. The corner frequency is presented as a function of the signal bandwidth B. The worst case distortion tone attenuation is calculated at the signal band edge where the HPF introduces the least attenuation. The thermal noise,

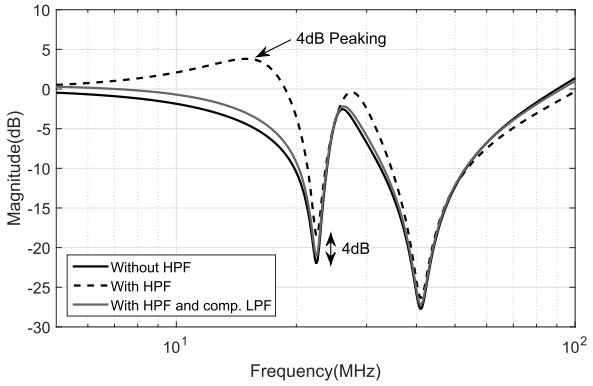

Fig. 15. Simulated closed-loop magnitude response with the LPF used to compensate the HPF.

quantization noise, and worst case distortion suppression with a corner frequency of 2.2 times the signal bandwidth are 12.1, 9.7, and 7.7 dB, respectively.

The first-order passive HPF with transfer function $H_{\mathrm{HPF}}(s)$ modifies the open loop gain of the system and thus introduces 4 dB peaking and 4 dB less blocker attenuation, as shown in Fig. 15. The first-order digital IIR LPF (H_{LPF}(z)) with dc gain of 26 dB, a pole at 1 MHz, and a zero at 20 MHz is added to compensate the HPF. It is designed such that the magnitude of $H_{\mathrm{HPF}}(s) \cdot H_{\mathrm{LPF}}$(z) is approximately unity from 1 to 360 MHz.

The three DACs are designed using a high-speed current-steering architecture [16]. No mismatch shaping is needed for $\mathrm{DAC_1}$, because it does not need to handle the blockers. For $\mathrm{DAC_{DIG}}$, the HPF is sufficient to filter distortion caused by DAC nonlinearity. Dither is not used in the DACs. The unit current for $\mathrm{DAC_1}$, $\mathrm{DAC_2}$, and $\mathrm{DAC_{DIG}}$ is 1.6, 1.4, and 7 μA respectively. $\mathrm{DAC_{DIG}}$ is clocked by $\mathrm{CLK_{DIG}}$, which is delayed from CLK by 0.7 period. The baseband full scale can be adjusted in 1 dB steps by increasing the unit current in $\mathrm{DAC_1}$, $\mathrm{DAC_2}$, and $\mathrm{DAC_{DIG}}$, and decreasing the VGA gain by the same amount.

A third-order feed-forward amplifier is used for the first operational amplifier [see Fig. 16(a)]. The first stage consumes 53% of the opamp power to reduce the input referred noise, whereas the output stage consumes only 20% of the opamp power, since the blocker power is mostly canceled by the digital path. A compensation capacitance C_C is placed at the output of the first stage to reduce the bandwidth of the third-order path. It is also possible to compensate the first stage with a Miller capacitor to reduce the compensation capacitor size. Three low-speed common mode feedback (CMFB) circuits are used to produce bias voltages V_{CM1}, V_{CM2}, and V_{CM3} for the three stages, with the schematic of the second stage CMFB shown in Fig. 16(b). To protect the amplifier from high-frequency common mode noise, mainly from the supply voltage ripples amplified by the PMOS pseudo differential pair, the CMFB circuit has a bandwidth of approximately 360 MHz. The differential output of the second stage V_{O2+} and V_{O2-} is averaged using a source follower, and common mode current is injected back into V_{O2+} and V_{O2-} with a

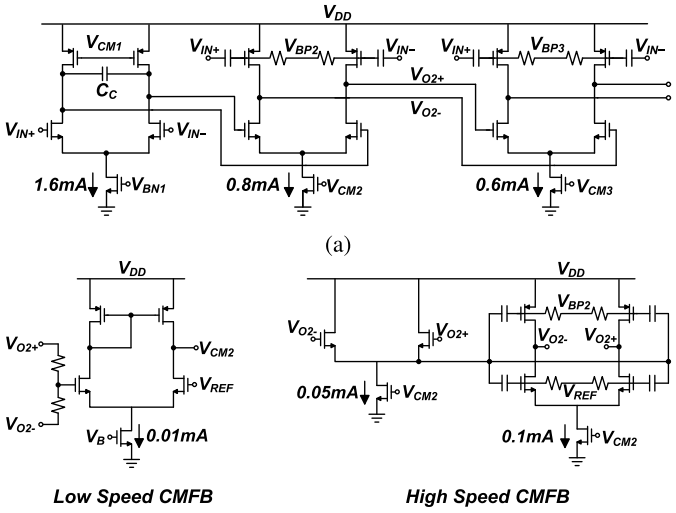

Fig. 16. Schematic of (a) third-order feedforward amplifier and (b) low-speed and high-speed CMFB circuit for the second stage.

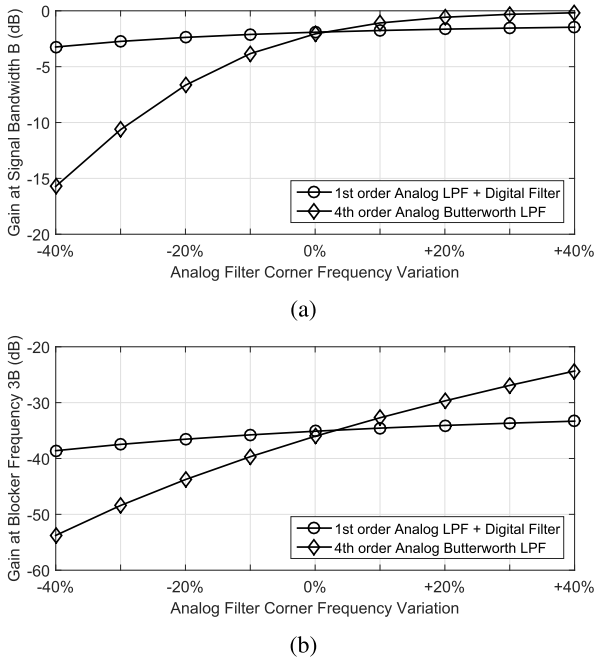

Fig. 17. Simulated gain variations at (a) signal bandwidth B and (b) blocker frequency 3B.

differential pair similar to the one used in the second stage. The high-speed CMFB circuit is only needed in one stage as it provides sufficient protection against high-frequency common mode noise.

The baseband transfer function is very accurate as it is determined mainly by the digital filter coefficients and clock frequency. On the other hand, a higher order analog filter (for example, the fourth-order Butterworth filter in [6]) requires accurate tuning of R and C. Even though the first-order passive analog LPF is used in this paper, it does not need tuning. Fig. 17 compared the simulated variations in baseband gain for the proposed digital filtering ADC and a fourth-order

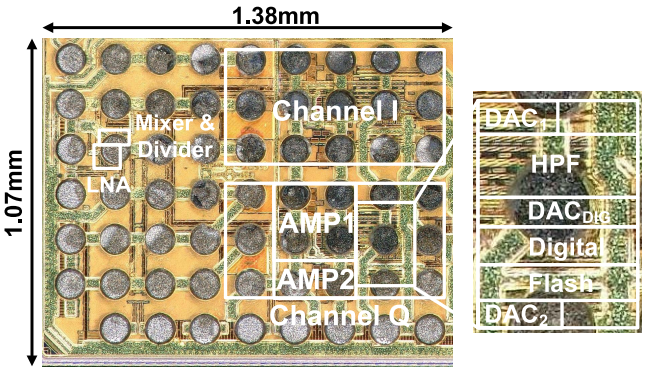

Fig. 18. Die photo.

analog Butterworth LPF. If the analog filter corner frequency varies ±40%, the gain at signal bandwidth B only changes by 2 dB for this paper compared with 16 dB if a fourth-order analog Butterworth LPF is used for blocker rejection [see Fig. 17(a)]. The gain at a blocker frequency of 3B changes by 5 dB for this paper compared with 30 dB for the fourth-order analog Butterworth LPF [see Fig. 17(b)]. With process and temperature variations, the metal–oxide–metal capacitor value in 28-nm CMOS can vary by ± 20%, and poly resistors vary by ±15%. Even excluding the switches, making R and C tunable presents at least 15%–20% area overhead, as well as increases complexity for calibration. A digital filter is also much easier to port into newer CMOS technologies and will benefit from scaling.

V. Measurement Results

The RF RX front-end prototype was fabricated in 28-nm CMOS technology. It occupies 1.07 mm × 1.38 mm with an active area of 0.64 mm^2 (see Fig. 18). In this prototype, part of the blocker detection digital circuitry was implemented off-chip in MATLAB, as shown previously in Fig. 7(b). If implemented on-chip, the total digital area will increase by 15% and the power consumption of these digital logic will be minimal as the blocker detection algorithm is only active for a maximum of 26 μs every 1 ms.

The measurement result is summarized and compared with other DSM-based RX designs in Table I. All measurements are performed with maximum gain setting (44 dB) controlled by the VGA unless otherwise specified. The RX front end operates at 0.9 and 1.8 GHz with a noise figure (NF) of 3.8 and 3.9 dB, respectively. The NF is measured by integrating the noise from 45 kHz to 9 MHz with the digital filter turned on. The RF front end (LNA+mixer) accounts for 82% of the total RX noise, and the baseband adds 18% which is dominated by the integrator. The RF front end in this paper was not optimized for this application and resulted in a poor NF but with a much smaller power consumption compared to [6]. It is worth noting that [6] has on-chip single-ended to differential conversion in the LNA, whereas the differential input RF front end used in this paper needs an external balun which further increases the NF by roughly 1.2 dB.

TABLE I
MEASUREMENT SUMMARY AND COMPARISON TABLE WITH OTHER DSM-BASED RXS

		[6]	[17]	[18]	[19]	This work	
Architecture		RX with ΔΣ-CSF	RX with filtering ADC	Direct ΔΣ RX	Direct ΔΣ RX	RX with ΔΣ-fb digital filter	
CMOS Technology (nm)		65	80	65	40	28	
RF Frequency (GHz)		0.6-3	0.04-1	0.4-4	0.7-2.7	0.9	1.8
NF(dB)		2.4-3.5	2.7-3.5	16	5.9-8.8	3.8	3.9
Power (mW)		35.5-53 43.4@1.8GHz[1]	221.4	17-70.5 37.8@1.8GHz[2]	90	19.5-36.6	20.4-37.5
Power Breakdown (mW)	RF[3]	23.5-36.7	113.4	-	48	4.4	5.3
	BB Analog	12-16.3	108	-	42	14.6	14.6
	BB Digital		-	-	-	0.5-17.6	0.5-17.6
Supply (V)		1.2	1.8/1	1.5/1.2	1.1	0.9	
IIP3 (dBm)		-6	-13	13.5	-2	-7	-5
SNDR (dB)		45-52		52-68	40-43	48	
RF Carrier BW (MHz)		10,20,40	5,6,7,8	4,10	1.4,15	18	
Area (mm^2)		0.7	5.6[4]	0.56	1	0.64	

1. LTE20 mode 2. Estimated 3. RF power includes LNA, mixer, LO gen and distribution
4. Incl. PLL and DSP

The baseband digital consumes as little as 0.5 mW with no blockers present, 11.7 mW with only TX leakage cancellation on, and 17.6 mW with both TX leakage and blocker cancellation enabled, and hence the total power consumption for 1.8-GHz input can vary between 20.4 and 37.5 mW. IIP3 is measured with two blockers at 17.5 and 35 MHz, in accordance with the LTE20 standard [10]. The programmable notch was placed at 17.5 MHz, thus canceling most of the intermodulation product. IIP3 is −5 dBm at 1.8 GHz. The baseband is very linear in the presence of blockers due to the digital blocker cancellation path; therefore, IIP3 is dominated by the RF front end.

Fig. 19 shows the measured output spectrum of channel I in four different scenarios for band 20 of the LTE20 standard. Note that the thermal noise is dominated by the RF front end. With the maximum gain setting, −48 dBm at the RX input translates to 0 dBFS at the ADC input. First, in Fig. 19(a), the desired signal (SIG) is at −3 dBFS. Since there are no blockers present, the digital filter can be turned off to provide a 45% power savings. Second, a +15 dBFS CW TX leakage is present at 41-MHz frequency offset from the input and the desired signal is −20 dBFS. The digital bandpass filter is turned on and placed exactly at 41 MHz to provide an attenuation of 34.9 dB [see Fig. 19(b)]. With the digital filter OFF, the ADC saturates as expected. Furthermore, in addition to the TX leakage, a +5 dBFS blocker is introduced at 22.5 MHz and is attenuated by 24.7 dB by the programmable filter, as shown in Fig. 19(c). Finally, Fig. 19(d) shows the ADC output spectrum with a −47 dBm modulated blocker at 22.5 MHz and a −34 dBm modulated TX leakage at 41 MHz as required by the LTE20 standard [10]. Both blockers are produced by PRBS9 data patterns modulated with 16QAM at a bandwidth of 5 MHz. The resulting input to the RX has a peak envelope power of −26 dBm. The modulated blocker at 22.5 MHz is attenuated by 17.3 dB and the modulated TX leakage is attenuated by 31.5 dB.

Fig. 20 shows the measured baseband frequency response with different settings for the programmable notch. It can be

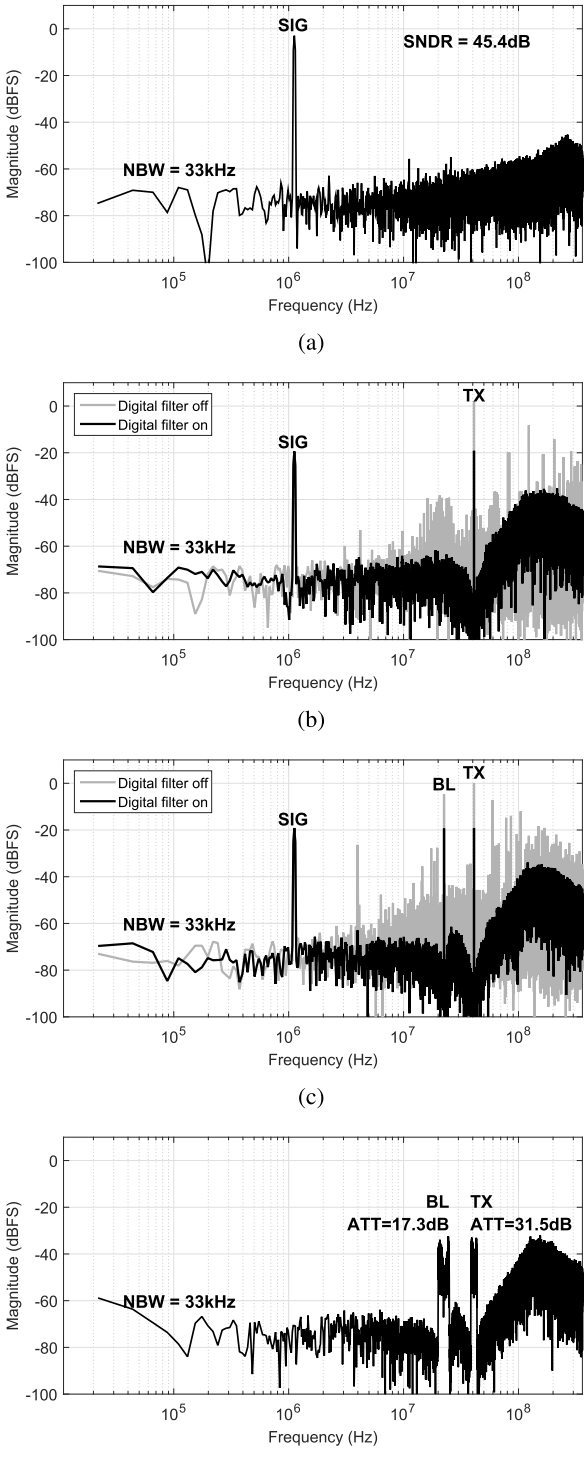

Fig. 19. Measured FFT spectrum for (a) no blocker, (b) CW TX leakage only, and (c) CW TX leakage and additional blocker, and (d) modulated TX leakage and additional blocker.

moved to any frequency in the range of 17.5–107.5 MHz, as shown in Fig. 20(a). The minimum frequency step size is 1 MHz. The amount of attenuation can be decreased in 6 dB steps to increase the loop phase margin [see Fig. 20(b)]. The Q factor of the notch can be adjusted depending on the modulated blocker bandwidth, as shown in Fig. 20(c). A low Q notch is undesirable near the signal band to prevent signal attenuation;

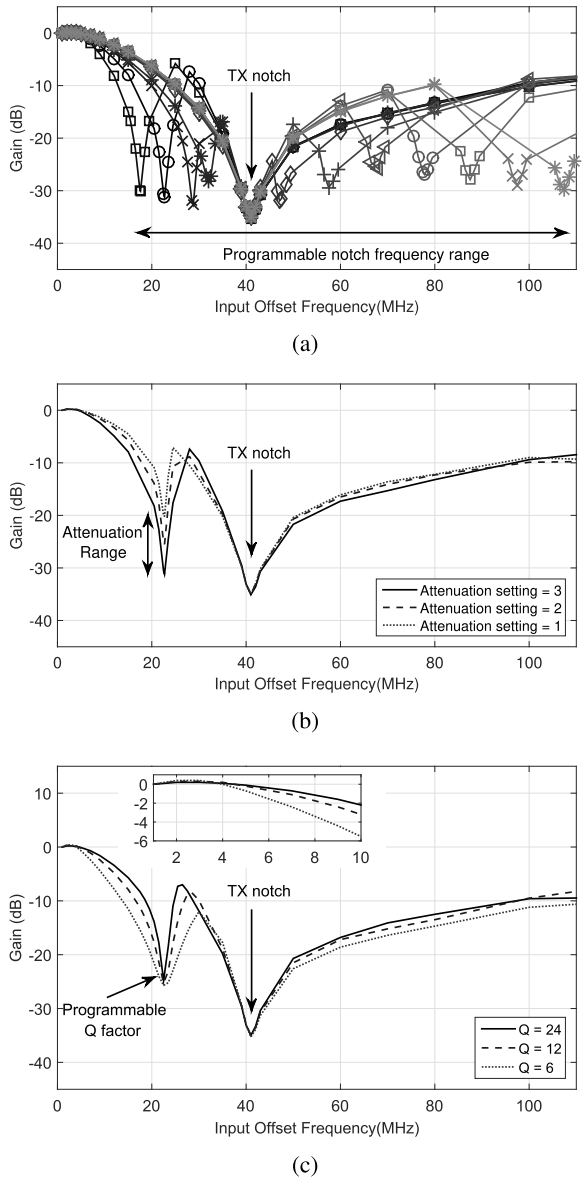

Fig. 20. Measured baseband frequency response for programmable notch at different (a) frequency, (b) attenuation, and (c) Q factor settings.

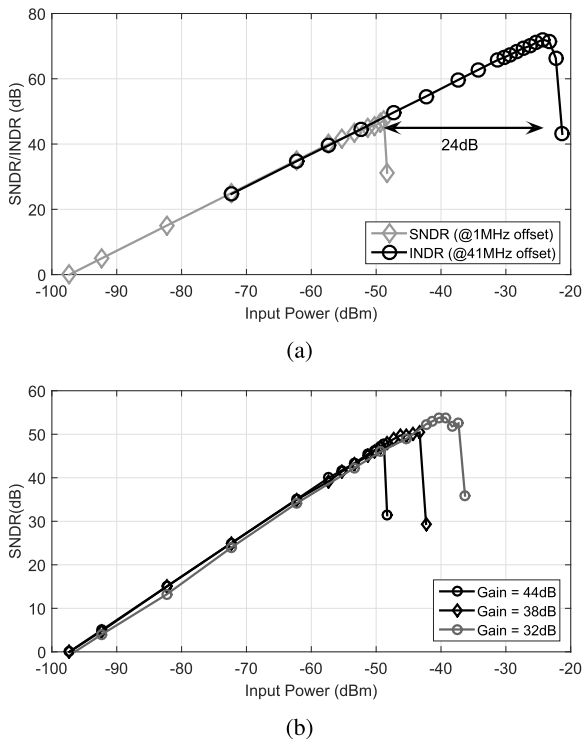

Fig. 21. (a) SNDR and INDR at maximum gain setting versus RF input power. (b) SNDR at different gain settings versus RF input power.

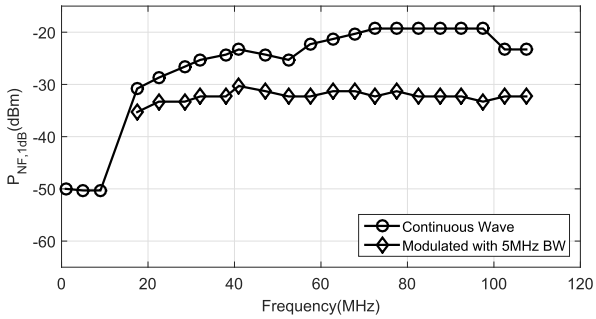

Fig. 22. $P_{\mathrm{NF,1\ dB}}$ versus frequency for a CW blocker and a modulated blocker with 5-MHz bandwidth.

however, that is not a problem as blockers close to the signal band have a maximum bandwidth of 5 MHz [10].

Signal-to-noise and distortion ratio (SNDR) is measured with a signal input offset 1 MHz from the carrier, and the interference-to-noise and distortion ratio (INDR) is measured at 41-MHz offset, as shown in Fig. 21(a). The INDR is defined as the power ratio between the interferer at the input and the in-band noise. It can be seen that the RX front end can handle a TX leakage 24 dB larger than the ADC full scale, while maintaining the same in-band noise. It is possible for the baseband to handle a blocker even larger than 24 dBFS by increasing the full-scale current of $\mathrm{DAC_{DIG}}$; however, the in-band noise and distortion from $\mathrm{DAC_{DIG}}$ will increase as well, which increases the RX overall NF. The SNDR is plotted with different gain settings in Fig. 21(b). The RX gain is digitally programmable in 1 dB steps via the VGA from 32 to 44 dB. The dynamic range improves at lower gain settings, whereas the NF remains the same at 44 and 38 dB gain settings, and degrades by 1 dB at 32 dB gain.

For CW and modulated blockers with 5-MHz bandwidth, $P_{\mathrm{NF,1\ dB}}$ is measured as the input blocker power when the NF increases by 1 dB (see Fig. 22). The modulated blocker used in this test has a peak-to-average power ratio of 9.5 dB, which is 6.5 dB higher than the CW blocker. The RX has great rejection for nearby blockers, just as expected. It can tolerate a -31 dBm ($+18$ dBFS) CW blocker at 17.5 MHz, which is less than twice the signal bandwidth.

Measured operation of the blocker detection algorithm is shown in Fig. 23. In the beginning, the blocker is at -12 dBFS and the RX is healthy with an SNDR of 30 dB at a signal amplitude of -20 dBFS. At iteration 7, a large blocker ($+7$ dBFS) appeared and the SNDR is reduced to 10 dB due to RX saturation. The algorithm first increases the ADC full scale and then initiates the blocker detection algorithm

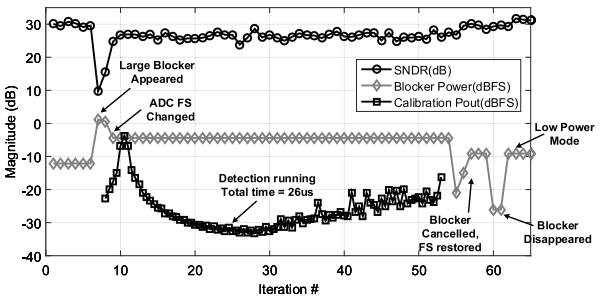

Fig. 23. Measured blocker detection algorithm.

that sweeps the programmable filter center frequency from 17.5 to 107.5 MHz in 1 MHz steps. The detection finishes at iteration 54 with a total time of 26 μs. With the blocker frequency known, it is canceled and the ADC full scale is restored. It can be seen that around iteration 58, the SNDR rises to 30 dB again. At iteration 60, the blocker disappeared and low power mode is activated, which turns off the digital filter to save power.

VI. Conclusion

An RF RX with a multi-blocker canceling baseband is introduced as a replacement for the conventional cascade of an analog filter and ADC. The digital bandpass filters produce two flexible notches in the baseband frequency response, canceling TX leakage and an additional blocker as required by the LTE20 standard. Compared with previous state-of-the-art designs, this paper achieves competitive IIP3 and NF, while consuming the lowest power and can dynamically scale its power depending on the number of blockers present.

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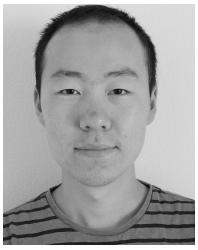

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