A Quantized Analog RF Front End

Javid Musayev and Antonio Liscidini, *Senior Member, IEEE*

***Abstract*— A surface acoustic wave (SAW)-less receiver with a quantized analog RF front end is presented. The front end is composed of 100 smaller unit front ends, each one dedicated to process only a portion of the input signal. This allows the compression point of the structure to be increased beyond the voltage supply and to reconfigure the dynamic range to fit different operative conditions. A prototype integrated in 65-nm CMOS is presented, where the 1-dB compression point can go up to 10.5 dBm under 0.8-V supply, while the noise figure can be lowered down to 1.5 dB. The RF front end and the baseband burn 14 mW, while clock generation and distribution burn 37.2 mW/GHz. Upon the configuration, IIP3 varies between 1 and 20.5 dBm, while IIP2 between 35 and 75 dBm with a single-ended structure. The third- and fifth-order harmonic rejections are over 40 and 47 dB, respectively. The active area is only 0.25 mm^2.**

***Index Terms*— Dynamic range, high linearity, low power, quantized analog (QA), receiver, surface acoustic wave (SAW)-less.**

I. Introduction

THE advantages of digital circuits hold over analog in signal storing, processing, and noise immunity, make it tempting to digitize the signal at the earliest stage possible in the signal processing chain. In case of wireless RF receivers, this idea started a pursuit of a software defined radio (SDR) a few decades ago [1]–[9]. Ultimately, an SDR would be a wideband analog-to-digital converter (ADC) directly following an antenna. However, stringent blocking requirements with a dynamic range (DR) up to 100 dB [10]–[12] and large carrier frequencies on the order of few gigahertz make ADC power requirements impractical. To cope with this challenge, an analog front end is used between the antenna and the ADC, which amplifies and down-converts the wanted signal, and filters unwanted blockers. Such front ends have challenging linearity and noise requirements as they need to amplify small signals accompanied by large blockers and transfer them to the baseband through down conversion, where filtering is ultimately performed [13], [14]. Therefore, what is called a modern day SDR is a digital reconfigurability in gain, noise, and filtering properties of the baseband [15]–[19]. However, filtering in the baseband is not sufficient to cope with large out-of-band (OOB) blockers, therefore most of the modern cellular receivers use external surface acoustic wave (SAW) filters. This opened up a new research path on SAW-less receivers, where the goal is to expand the dynamic range of the front end, eliminating the need for SAW filters [20]–[22].

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J. Musayev was with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering,University of Toronto, Toronto, ON M5S3G4, Canada. He is now with Rambus Inc., Toronto, ON M5J2M4, Canada (e-mail: javid.musayev@mail.utoronto.ca).

A. Liscidini is with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S3G4, Canada (e-mail: antonio.liscidini@ utoronto.ca).

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A. SAW-Less Receiver Architectures in the Literature

The main limitation in high-linearity front ends is the non-linear active devices. This is manifested as compression for large voltage swings, and weak distortion for small voltage swings. The mixer-first receivers deal with this problem by avoiding active elements in the front end [23]–[25]. In such receivers, antenna is directly interfaced to a passive down-conversion mixer, feeding the signal into baseband where it is eventually filtered. Although excellent linearity is achieved with such architectures (e.g., IIP3 = 44 dBm, P_{1dB} = 13 dBm [22]), matching with passive elements results in a noise figure (NF) greater than 3 dB [16], and the lack of amplification at the first stage leads to the excessive power demand in the baseband to maintain low noise (e.g., 30 mW in baseband and 36 mW/GHz in local oscillator (LO) for [22]).

The NF problem in mixer-first receivers can be alleviated by synthesizing impedances through feedback in the baseband (for high linearity) [25], or by using an auxiliary active path for noise canceling [7], [26]–[28], which ultimately becomes the linearity bottle-neck of the system. Both approaches require more power due to the active elements used. Therefore, for achieving low power, LNAs are still required. To deal with compression concerns, low-noise transconductance amplifiers (LNTAs) [21], [29], [30] are mainly used, which can even be accompanied by transformers [31], [32], to allow voltage swings larger than supply, and boost g_m [33]. The current signal produced by the LNTA is converted to voltage only after down-conversion and filtering. This helps with the output compression but necessitates the use of very large switches in the mixer for low LNTA output impedance, which increases the power in frequency generation. Blocker-filtering techniques [34]–[37] can help with this regard, which create sharp filtering profiles through the concept of impedance translation [12], [38]–[41]. This allows LNTAs to have lower output impedance at blocker frequencies, hence not develop much voltage for the large currents produced by the blockers. This idea can even allow the use of voltage-mode LNAs [42]–[44], but those have lower compression points than current mode. Creating such impedances is done through a non-linear switching process and, therefore, requires multi-phase LO signals to avoid harmonic generation and burns considerable LO power. Impedance translation with multiple LO phases is, in a way, equivalent to N-path filtering that is widely used in both active front ends [45]–[47] and mixer-first receivers [48]–[50] for achieving high linearity but also comes at the expense of power in frequency generation.

In almost all of the discussed topologies, harmonic rejecting multi-phase mixers [51] are used to reduce desensitization of the wanted signal due to the LO harmonics [26], [52]. These techniques are not mutually exclusive. Various combinations of all listed methods have been used in [31], [53], and [54]. However, due to the inherent tradeoff between noise and linearity, it is hard to improve the DR without burning excessive power in either LNA or mixer or baseband. In fact, the blocking scenarios defining the DR requirements of a wireless standard can be variant. Therefore, average power efficiency can be improved if DR of the receiver is made adaptive to these scenarios. There are some studies in the literature where receivers can operate in two modes (low noise/high linearity) [29] by switching on/off some component of the receiver (e.g., noise canceling auxiliary path [28]). In fact, a true SDR would ideally require a much more flexible adjustment in DR performance to maintain power efficiency in a variety of scenarios.

In this paper, we propose a receiver with an RF front end implemented using a quantized analog (QA) architecture [55], which addresses the issues outlined above. As highlighted in [56], the quantized-analog amplification increases the input range of an amplifier for a given power dissipation virtually above the nominal supply, improving the DR for a given power consumption and allowing voltage-mode operation even at very low-voltage supplies. In the context of the proposed receiver, the former property is exploited to obtained a SAW-less operation, while the latter to implement a novel harmonic rejection (HR) mixer architecture. The quantization of the analog signal path allows us to also exploit multi-tanh linearization [57] leading to an improvement of small signal distortions such as IP2 and IP3. Finally, we will show that the DR and spurious free dynamic range (SFDR) of the QA can be easily reconfigured, which makes it possible to adapt the receiver to blocking scenarios and minimize power consumption.

This paper is structured as follows. Section II revisits the QA concept and its main properties. Section III presents the QA receiver architecture and the novel HR mixer architecture. Section IV provides the prototype measurement results and Section V concludes this paper.

II. Quantized Analog Theory

In the quantized inverter amplifier proposed in [56], a CMOS amplifier is sliced into multiple elements, where each one is dedicated to amplify only a portion of the input signal. In [56], it has been demonstrated that such signal decomposition leads to several benefits, such as expansion of both input and output ranges of the amplifier, improvement of the SNR for a given power and minimization of the small-signal distortions. Such kind of signal decomposition is similar to the approach presented by Tsividis [58] on continuous-time digital signal processing. However, in the case of the quantized-analog amplification, the signal remains analog also after the decomposition in multiple paths.

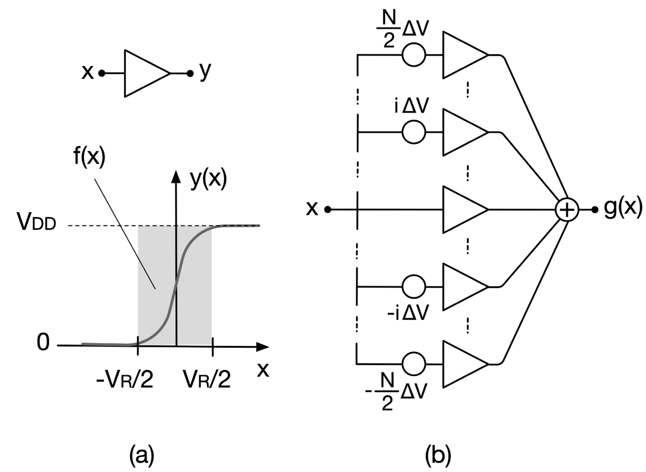

Fig. 1. (a) Single amplifier. (b) Quantized amplifier.

In addition to what was already presented in [56], the aim of this section is to provide an analytical description of the signal decomposition in order to highlight the main tradeoffs and the key elements which ultimately define the DR of the quantized radio. Although for simplicity, the analysis is based only on an amplifier, it can be extended to any linear operation occurring between the signal decomposition and its recombination [56].

A. Liquid Digital Signal Decomposition

Let us consider the amplifier shown in Fig. 1(a) with an input–output characteristic defined as follows:

$$y(x) = \begin{cases} 0 & x < -V_R/2 \\ f(x) & -V_R/2 \le x \le V_R/2 \\ V_{\mathrm{DD}} & x > V_R/2 \end{cases} \tag{1}$$

where $f(x)$ is a continuous function between the input and the output, V_R represents the maximum input range of the amplifier before saturation, and $[0, V_{\mathrm{DD}}]$ is the output range. When the amplifier is quantized in $N + 1$ slices (where N is an even number) [Fig. 1(b)], the overall transfer function becomes

$$g(x) = \sum_{i=-N/2}^{N/2} y(x - i\Delta V) \tag{2}$$

where ΔV is an offset applied at the input of each slice properly scaled upon the position i (which is limited between $-N/2$ and $N/2$). When $\Delta V \neq 0$, (2) can be rewritten as a function of the unit amplifier characteristic $f(x)$ as

$$g(x) = \sum_{i=-N/2}^{D_1(x)} V_{\mathrm{DD}} + \sum_{i=D_1(x)+1}^{D_0(x)-1} f(x - i\Delta V) + \sum_{i=D_0(x)}^{N/2} 0 \tag{3}$$

with

$$D_1(x) = \left\lfloor \frac{x - V_R/2}{\Delta V} \right\rfloor \tag{4}$$

$$D_0(x) = \left\lceil \frac{x + V_R/2}{\Delta V} \right\rceil \tag{5}$$

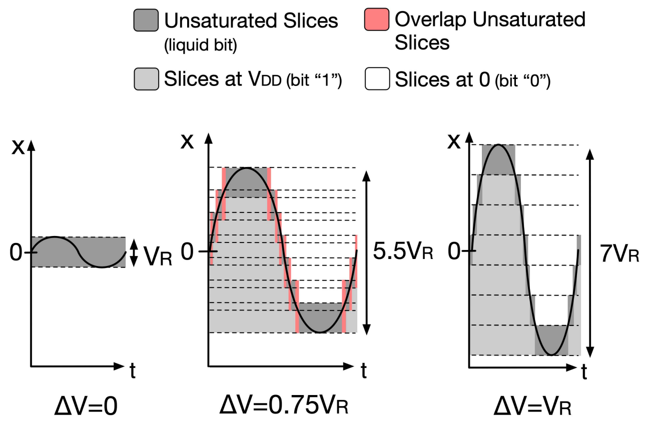

Fig. 2. Input range expansion for different ΔV $(N = 6)$.

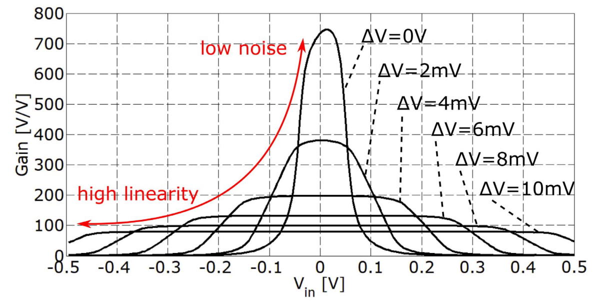

Fig. 3. LNA gain after the reconstruction (A_{QA}) as function of ΔV. $V_R = 80$ mV for the amplifier used in this simulation.

where $D_1(x)$ and $D_0(x)$ produce the two integer values obtained from floor and ceiling of functions of the input signal x, as shown in (4) and (5). The three series in (3) are representative of the status of different slices: the ones from $-N/2$ to $D_1(x)$ are saturated to V_{DD} (corresponding to an equivalent digital value "1"), the ones between $D_1(x) + 1$ and $D_0(x) - 1$ are working as analog amplifiers, and the ones from $D_0(x)$ to $N/2$ are saturated to ground (corresponding to an equivalent digital value "0").

Note that although some slices are saturated, the overall output $g(x)$ does not saturate if the input signal x is confined between $(-V_R - N\Delta V)/2$ and $(V_R + N\Delta V)/2$. Hence, compared to the original amplifier, the input range increases from V_R to $V_R + N\Delta V$.

To better understand this concept, Fig. 2 depicts a sinusoidal input signal with the maximum amplitude that does not saturate the QA amplifier. In Fig. 2, the status of different slices is highlighted: saturated to V_{DD} (light gray), unsaturated (dark gray), or saturated to ground (white). When $\Delta V = 0$, all the slices are completely overlapped and unsaturated, so the input range of the QA amplifier is equal to the original amplifier (i.e., V_R). When $\Delta V = 0.75\ V_R$, there is a partial overlap among the characteristics but thanks to some saturated slices the input range increases. The maximum input range is obtained for $\Delta V = V_R$ (third case) when at any x, only one slice is unsaturated.

All together the lines form a sort of thermometric code similar to the one produced by a flash ADC. Equation (3) can be rewritten in a more compact form as

$$g(x) = D(x) \times V_{\mathrm{DD}} + \sum_{i=D_1(x)+1}^{D_0(x)-1} f(x - i\Delta V) \tag{6}$$

where D(x) is an integer number corresponding to the digital thermometric code produced by the saturated lines given by

$$D(x) = D_1(x) + 1 + N/2. \tag{7}$$

Equation (6) is composed of two parts: a pure digital component, defined by D(x) (i.e., digital bits), and an analog residue produced by the unsaturated slices digitally undefined, which we named *liquid bits*. Note that while in a traditional mixed signals circuit analog and digital domains are separated by a fixed interface (i.e., ADC and digital-to-analog converter), in the case, here each slice swings between its analog and digital states upon the value of the input signal. Like in digital signals, the saturated slices do not introduce analog noise or distortion during the signal reconstruction [56]. On the other hand, the analog residue preserved in the *liquid bits* allows us to eliminate the quantization noise produced by the digital component but introduces analog noise and distortion during the signal reconstruction.

B. Gain of the Quantized Analog Amplifier

The expression of the gain of the QA amplifier can be obtained from the derivative of (3) that becomes

$$g'(x) = \begin{cases} N \times f'(x) & \Delta V = 0 \\ \displaystyle\sum_{i=D_1(x)+1}^{D_0(x)-1} f'(x - i\Delta V) & \Delta V \neq 0. \end{cases} \tag{8}$$

The above expression shows that the overall analog gain, as expected, depends only on the unsaturated slices and increases with the overlap (i.e., if ΔV decreases). The maximum gain, equal to N times the gain of the original amplifier $f'(x)$, is obtained for $\Delta V = 0$. On the other hand, the minimum gain [equal to $f'(x)$] is obtained for $\Delta V = V_R$ when there is only once unsaturated slice at the time. This behavior is confirmed by the simulation of the gain of the QA amplifier used as LNA in this design (A_{QA}) (Fig. 3).

When $\Delta V = 0$, the peak of the overall gain is equal to the peak of the gain of the single unit (i.e., 7) times the number of elements (i.e., 100). In this case, the overall input range is equal to the input range of the single unit V_R that is 80 mV for a minimum gain 3 dB below the peak. The gain rapidly decreases as the overlap among the slices diminishes, while the input range increases approximately to 1 V (i.e., $V_R + N\Delta V$).

C. Weak Distortion in a QA System

As it can be seen from Fig. 3, the gain of the single slice [i.e., $f'(x)$] defines the shape of the overall gain [i.e., $g'(x)$ and with both compression point and weak distortions (e.g., IP2 and IP3). The weak distortions can be studied through the series expansion of the characteristic around a given bias point, as done also in [57]. To do that, the higher order derivatives of $g(x)$ are needed. If $y(x)$ is C^∞, it is possible to verify that, starting from (8), the generic expression of the ith order derivative $g^{i\text{th}}(x)$ is equal to

$$g^{i\text{th}}(x) = \begin{cases} N \times f^{i\text{th}}(x) & \Delta V = 0 \\ \sum_{i=D_1(x)+1}^{D_0(x)-1} f^{i\text{th}}(x - i\Delta V) & \Delta V \neq 0. \end{cases} \tag{9}$$

The above equation suggests that small-signal linearity of $g(x)$ depends only on the *liquid* component of $g(x)$ and it can be improved by choosing properly ΔV to minimize $g^{i\text{th}}(x)$, as also done by Gilbert [57]. In the original multi-tanh analysis proposed by Gilbert, the linearization occurs in current where the voltage-to-current transfer characteristics of a bipolar differential pair resemble a tanh function. In this case, the linearization relies on the voltage-to-voltage transfer characteristics of a CMOS inverter that also resembles a tanh function as shown in [59] and [60].

The multi-tanh approach and the QA technique are similar since both rely on multiple shifted characteristics added up together. However, in the case of multi-tanh approach, the goal is only to minimize the small signal distortion (by averaging the non-linear gains of the paths) [57]. Therefore, the offsets and the number of slices are chosen so that for any input voltage, all the slices are unsaturated. The proposed QA amplification extends beyond the assumptions in [57] since it also adds saturated lines to improve the large signal distortion (e.g., compression point) and to lower the noise (at a given power) [56].

The difference between the two techniques is highlighted by the approach to choose the number of slices. In the multi-tanh approach, ΔV and N are chosen so that for each point of the characteristic, all the slices produce unsaturated currents that concur to minimize the high-order derivatives [see (9)]. For this reason, as explained in [57], for an optimum ΔV, N is typically small (e.g., 5) because due to the exponential characteristic of a bipolar device, the characteristic of each unit saturates very fast.

In the quantized-analog amplification, however, the main goal is to increase the DR of the amplifier. As shown in Fig. 2, the input range of the QA amplifier is maximized by maximizing the number of the saturated lines [i.e., the digital component of g(x)]. This can be done by increasing ΔV or alternatively by increasing N. A large number of saturated lines does not only lead to a larger input range but also to a larger DR for a given power, since the saturated lines (being "digital") do not introduce analog noise [56] and by operating in voltage mode, they do not consume additional static power. This explains why in the case of a QA amplifier, N is typically much larger than in the multi-tanh approach. In fact, ΔV is chosen as in [57] to minimize the weak distortions, while N is determined by the target input range, which is defined by $V_R + N\Delta V$.

D. Reconfigurability of NF and DR in a QA System

When the amplifier is sliced into N sub-units, the input-referred noise of each amplifier increases by a factor N [56] because each slice is biased with 1/N of the current to keep the same power dissipation of the original amplifier. However, as explained in [56], despite such increase in the input-referred noise, when ΔV is increased, the DR also increases. This happens because the allowable input–output signal swings increase, while the number of unsaturated lines, which are the only ones that produce noise at the output, decreases (e.g., Fig. 2).

Although the DR of an analog system is the main parameter that limits the bit-error-rate in demodulation of a signal, for a wireless RF front end, the input referred noise is also a crucial parameter, as it defines the NF and with it the sensitivity of the receiver.

In the absence of large signals (i.e., sensitivity test), the dependence of NF on ΔV can be described analytically by assuming an equal input-referred noise spectral density of v_n^2 for each slice. Since in the sensitivity case, the input signal is very small, a small-signal analysis can be performed. In this case, the overall noise at the output of the QA amplifier is given by the sum of the noises produced by the unsaturated slices as in (10)

$$v_{n,\text{out}}^2 = \sum_{i=D_1+1}^{D_0-1} v_n^2 |f'(i\Delta V)|^2 \tag{10}$$

where D_1 and D_0 are obtained from (4) and (5) with $x = 0$ and $f'(i\Delta V)$ is the gain of the ith unsaturated slice. To evaluate the expression of the NF (with respect to a source resistance of R_S), the noise spectral density produced at the output of the QA can be referred to the input through the small signal gain expressed by (8) as in (11)

$$\text{NF} = 1 + \frac{\sum_{i=D_1+1}^{D_0-1} v_n^2 |f'(i\Delta V)|^2}{4\text{kTR}_S |\sum_{i=D_1+1}^{D_0-1} f'(i\Delta V)|^2} \tag{11}$$

where the second term of the equation represent the noise produced by the unsaturated units divided by the noise produced by the source at the output. By acting on ΔV, it is possible to vary D_1 and D_0 [see (4) and (5)] and, therefore, the achievable NF. Although it is very difficult to get a simpler expression of (11) for a generic value ΔV, the NF range can be appreciated considering the cases when $\Delta V = 0$ and $\Delta V = V_R$.

The minimum NF (but also the smaller input range) is obtained for $\Delta V = 0$. In this case, all the slices are in parallel and (11) can be rewritten as

$$\text{NF} = 1 + \frac{v_n^2}{4\text{kTR}_s N} \tag{12}$$

This case represents the best configuration in terms of NF, but the worst in terms of DR. When $\Delta V = V_R$ (i.e., only one slice unsaturated), both the DR and NF reach their maximum and (11) becomes

$$\text{NF} = 1 + \frac{v_n^2}{4\text{kTR}_s} \tag{13}$$

The variation of ΔV is the main parameter of reconfigurability since it can control noise, weak distortion, and the compression point, which define DR and SFDR. This is the

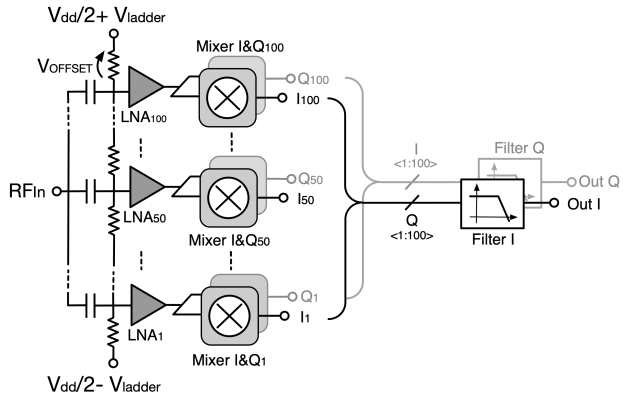

Fig. 4. QA receiver architecture.

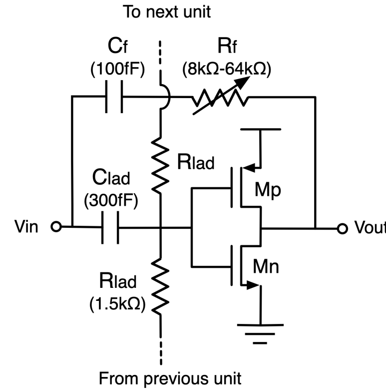

Fig. 5. LNA with a resistive feedback matching.

key idea of the proposed quantized RF front end that aims to increase the DR only in the presence of an interferer. Notice that, although this mechanism could resemble a variable gain control, there is a fundamental difference, since a mere variation of the gain in front of a stage cannot change its DR as both noise and compression point are scaled by the same factor [56].

E. Recombination in a QA System

A QA system requires a linear recombination to reconstruct the amplified signal. For systems that are ultimately terminated by ADC, this recombination can be performed in digital domain [56]. Another possibility is to recombine the signal in analog domain by adding them in such a way that the overall output swing does not exceed the nominal supply. This can be done by the use of a transimpedance amplifier (TIA) as proposed in the presented prototype, where for the lack of resources, an ADC could not be implemented. In this case, the benefit of the QA is lost for the parts of the system following the summation, since the recombined signal amplitude becomes limited by the supply.

III. Quantized Analog Receiver

The concept of signal decomposition applied to the QA amplifier can be extended to any linear signal processing as shown in the QA RF front end depicted in Fig. 4. An RF front end is split in 100-RF front-end units (i.e., the QA slices) that are recombined after the mixer by summing the current outputs using a TIA. In the proposed solution, tailored to SAW-less applications, each RF front-end unit is composed of an LNA, a harmonic-rejection mixer, and a frequency divider, while the baseband is implemented with two differential TIAs which provide I and Q outputs. Note that by having a mixer in a QA slice does not disrupt the operation, since ideally the down-conversion is a time-variant linear operation. Offsets between the QA slices are generated through a resistive ladder as in [56], and the input is ac-coupled. All the LNAs share the same supply (i.e., 0.8 V) while V_{ladder} is used to reconfigure the offsets ΔV, thereby making the front-end adaptive to various DR, noise, and compression requirements as previously discussed. Since the overall DR depends ultimately on the input-referred noise of the unit element, the choice of a granularity of 100 elements was motivated by having a fine-tuning of the NF and the DR.

A. Low-Noise Amplifier

Fig. 5 shows the schematic of the LNA. It is composed of an inverter-based voltage-mode amplifier, with a resistive feedback matching. The LNA is biased through the resistors R_{lad} that belong to the resistive ladder shown in Fig. 4. The RF input is ac-coupled by the capacitor C_{lad}.

The inverter is sized to have large enough g_m to meet the minimum NF requirement, which is obtained when all 100 slices are in parallel (zero dc-offset in the ladder). The bias points of nMOS and pMOS transistors in the inverter have been designed to achieve the highest current efficiency for the maximum g_m. This has been done by setting the inverter supply voltage to the sum of the two required V_{GS} values. In our design, this corresponded to a supply voltage of 800 mV for the g_m/I_d of 15 V^{-1}. Note that the supply of the LNA defines only the input range of the single slice (i.e., $V_R = 80$ mV), while overall input range of a QA structure (being equal to $V_R + N\Delta V$) can be customized by varying the dc-offset ΔV between 0 and 10 mV (i.e., V_{ladder} between 0 and 0.5 V).

A resistive feedback network is used to match to a 50-Ω antenna. Each slice draws a current proportional to the difference in its input and output voltages divided by RF. Then, the overall input current is equal to

$$i_{\text{in}} = \frac{N v_{\text{in}} - \sum_{i=1}^{N} v_{\text{out},i}}{R_f} = v_{\text{in}} \frac{N - \frac{\sum_{i=1}^{N} v_{\text{out},i}}{v_{\text{in}}}}{R_f}. \tag{14}$$

Defining the ratio of the total output voltage (i.e., sum of all slices) to the input voltage by A_{QA}, the input resistance can now be written as

$$R_{\text{in}} = \frac{v_{\text{in}}}{i_{\text{in}}} = \frac{R_f}{N + A_{\text{QA}}} = \frac{R_f}{100 + A_{\text{QA}}}. \tag{15}$$

The feedback resistor R_f is made 3-bit adjustable to accommodate matching under different gain conditions, considering that A_{QA} would change with the ladder offset (i.e., the overlap among the slices). Another condition on R_f is that it should be larger than the output resistance of the inverter, to not affect the gain, but it can be easily shown that this condition is automatically maintained when inverter size is increased to meet the NF requirement. The R_f is ac-coupled to the input through C_f, which is sized to have lower impedance than R_f at the operating frequency. This is done because in a QA system each inverter operates at a different bias point at a given time.

The last element in the LNA is the biasing RC network. The input is ac-coupled to the gate of the inverter with a capacitor much larger than the input capacitance to minimize attenuation and the effect of the gate capacitance non-linearity. The two ladder resistors connect each slice to the previous and the next one, providing a continuous biasing and offsets ΔV (between 0 and 10 mV) among RF front-end units. This configuration provides low-pass filtering for the noise of resistors and makes it negligible at RF frequency. In theory, increasing resistor size pushes the cutoff of the low pass to a lower frequency and reduces the noise, meanwhile reducing the ladder power consumption as well. However, care must be taken not to reduce the ladder current too much, as gate leakage of the inverters could move around the bias points and create non-linearity in the ladder.

The total NF of the LNA can be calculated as in (16), where γ is the transistor noise factor and G_M is the sum of all transconductances in the QA front end. The NF portion due to the matching can be easily found by referring the noises of N R_f resistors to the input through gain A_{QA}, and assuming a matched condition $R_s = R_{\text{in}}$, using the R_{in} expression of (15)

$$\text{NF}_{\text{LNA}} = 1 + \underbrace{\frac{\gamma}{G_M R_s}}_{\text{inverter}} + \underbrace{\frac{(N + A_{\text{QA}})N}{A_{\text{QA}}^2}}_{\text{matching}}. \tag{16}$$

B. Passive Harmonic Rejection Mixer

Current passive down-conversion mixers following an LNTA have been widely used in radio front ends in recent years, for the good compression properties of the current-mode architecture and linearity of passive switches [12], [38]–[41]. However, as higher order HR is required, such architectures use multiple TIAs because typically the required scaling of the signals in each phase is performed in the baseband, as scaling of the current coming from the LNTA in each phase is not possible.

In this paper, we propose a passive HR mixer (Fig. 6) following a voltage-mode LNA (Fig. 5). Voltage-mode architecture allows to scale the signals by terminating the LNA with different impedances in each phase. This allows having a different current flowing into the mixer in each phase, therefore only a single baseband is sufficient to recombine the down-converted currents. Fig. 6 shows the mixer architecture. C1 and C2 are the impedances converting the output voltage of the LNA to current signals that are directed to one of the low-impedance baseband terminals (I+, I−, Q+, or Q−) in each LO phase. In this way, the amount of current flowing to the baseband can be varied from phase to phase and an effective LO signal free of third and fifth harmonics can be

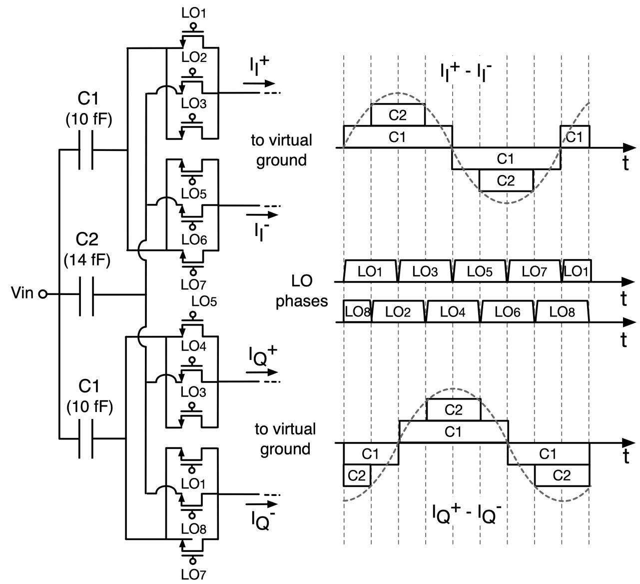

Fig. 6. Passive HR mixer following a voltage-mode LNA.

generated. In general, a sinusoidal signal uniformly sampled at any eight points would not have third and fifth harmonics. In addition, a specific choice of these sampling points can minimize the number of required levels, allowing to use a less number of impedances following the LNA. Fig. 6 also shows the sampling scheme used in this paper, which needs only two distinct amplitude levels, hence only two distinct capacitance values C1 and C2, where C2 is 1.41 times larger than C1. Capacitors were used instead of resistors to avoid the thermal noise. Note that the three capacitors act as a load for the LNA, and their impedance must be larger than the LNA output impedance to allow the LNA to work in the voltage mode.

The mixer transconductance with the given down-conversion scheme can be calculated as in (17)

$$G_{\text{mix}} = \frac{4}{\pi} \cdot \omega C1. \tag{17}$$

All of the QA outputs are shorted at the baseband low impedance terminals, therefore the overall RF gain is equal to $A_{\text{QA}} \cdot G_{\text{mix}}$.

C. Frequency Generation

The proposed HR scheme requires eight LO phases with 45° phase shift and 25% duty-cycle shown in Fig. 6. These waveforms are generated with a divide-by-four frequency divider composed of four flip-flops (eight master–slave dynamic latches). Initially, the flip-flops' bits are reset to the binary value of "1000," which is then circulated through the shift register. This makes the latch outputs circulate the binary value of "11000000," resulting in 25% duty cycle waveforms shifted by 45° as was intended.

Having a local frequency divider in each QA RF front-end slice allows simpler phase distribution in the layout. Instead of distributing eight 2-GHz LO phases across 600 μm, i.e., 100 slices with 6-μm pitch), a single 8-GHz clock is routed and the waveforms are generated locally.

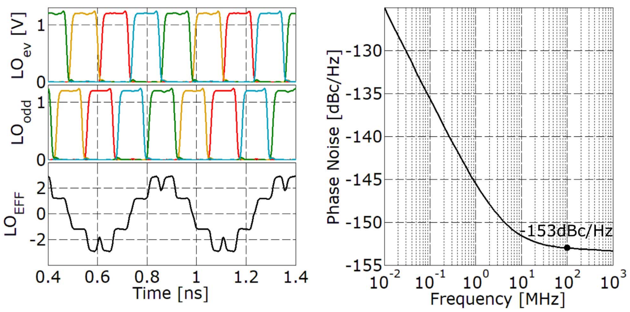

Fig. 7. Postlayout simulated phase noise of the divider in the single slice of QA RF-front end.

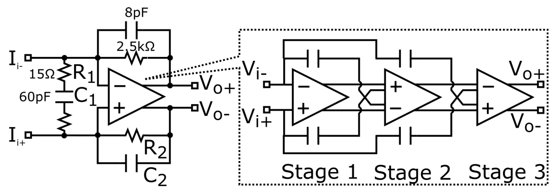

Fig. 8. Baseband TIA and opamp architecture.

The size and power consumption of the divider was defined based on the phase noise requirement, which can be calculated from the blocker NF (BNF) contribution due to the reciprocal mixing (4) [61]

$$\mathrm{BNF} = P_b + L(\Delta f) + 174_{[\mathrm{dBm/Hz}]} \tag{18}$$

where P_b is the blocker power, which is assumed to be 0 dBm based on the design specifications. Considering that the LNA NF would be around 7 dB in the high linearity mode (i.e., with the largest offset in ladder) and targeting an overall NF less than 10 dB, the BNF can be as large as 7 dB. This suggests that phase noise at the offset of the blocker (100 MHz in our case) should be less than −167 dBc/Hz. Fig. 7 shows the postlayout simulated phase noise of the effective LO waveform of the divider in a single slice of the QA RF front end, which was driven by an 8-GHz clock signal (for the LO frequency of 2 GHz). The phase noise at 100-MHz offset is −153 dBc/Hz suggesting that for the total of 100 slices, it is −173 dBc/Hz, which is 6 dB better than the requirement. The divider consumes 27.6 mW from a 1.2-V supply in this case. However, as will be shown in Section IV, the actual power consumption ended up being 2.7 times larger due to unestimated parasitics not captured in the postlayout simulation.

D. Baseband Trans-Impedance Amplifiers

The baseband consists of two differential TIAs which act as a summing and filtering element in the QA RX architecture. The low-impedance input terminals of the baseband TIAs collect the down-converted currents of all RF front-end units, while feedback impedance of the TIA amplifies the in-band signals and filters out the blockers. The architecture of the TIA is shown in Fig. 8.

The feedback $R_2 - C_2$ network places the cutoff frequency of the TIA at 8 MHz, and a larger input capacitance C_1 is used to provide a low-impedance node, at frequencies beyond opamps unity gain frequency. A small resistor R_1 is placed in series with C_1 for stability purposes. The opamp has a three-stage feed-forward topology as shown in Fig. 8 for achieving large gain, bandwidth, and the output swing. The first stage has a high gain, low bandwidth; the second stage has a moderate gain and moderate bandwidth; and the third stage has a low gain and a high bandwidth. The input is ac-coupled to every stage, so that when the gain of a former stage drops, the gain of the latter stage takes over, recovering the phase drop [62], [63]. In this way, even at high frequencies, when the first two stages have very low gain, but the last stage still is functional, the opamp can behave similar to a first-order system, hence maintaining stability. To achieve such a gain-bandwidth requirement, the first stage is designed with 800-nm length devices, the second stage with 120-nm length devices, and the last stage with 60-nm length devices. The three stages consume 1.6, 0.3, and 0.8 mA, respectively, while biasing and common-mode feedback circuitry consume 0.3 mA overall. This makes the total power consumption of the two opamps (I and Q) 6 mW (operated from 1-V supply) in idle condition and 8.5 mW in the presence of a large blocker (when the third stage sinks or sources additional blocker current).

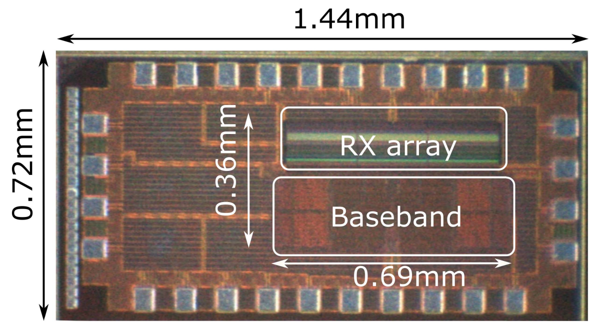

Fig. 9. Micrograph of the prototype. The active area is 0.25 mm^2.

IV. Prototype and Measurement Results

A prototype was fabricated in 65-nm CMOS technology and occupies an active area of 0.25 mm^2. The micrograph is shown in Fig. 9. The width of a single RF unit is 6 μm, therefore the overall front end is 600 μm wide. The baseband layout is implemented with a particular consideration given to matching the total width of the RF front end. The chip was wire-bonded to a daughterboard which had two SubMiniature Version A connectors for the LO clock and RF input. Both connections were impedance controlled and had a π-matching network to compensate for the parasitics.

A. Frequency of Operation

Despite the wideband nature of the RF front end, the RF frequency of the receiver was limited by the frequency divider to 1.4 GHz, even though the chip was intended to operate up to 2 GHz. The reason for this limitation was the parasitic elements associated with the capacitors used to ac-couple the

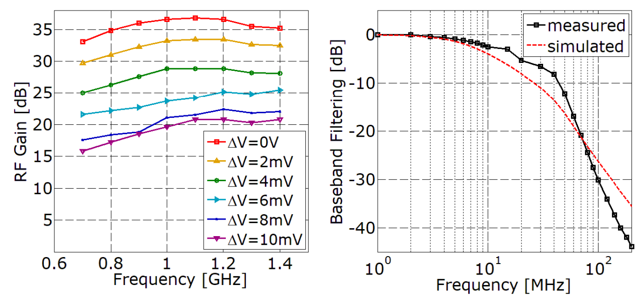

Fig. 10. RF gain and baseband filtering.

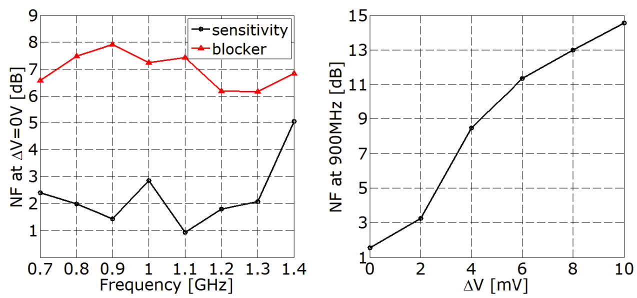

Fig. 11. NF measurement. Frequency and ladder offset dependence.

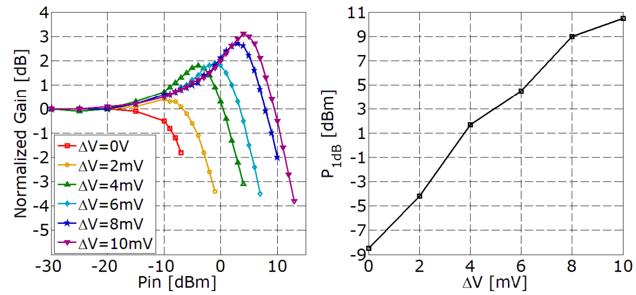

Fig. 12. $P_{1\text{ dB}}$ as a function of offset, extracted from input–output power curves. Measurements are performed at 900-MHz LO frequency and 100-MHz blocker offset.

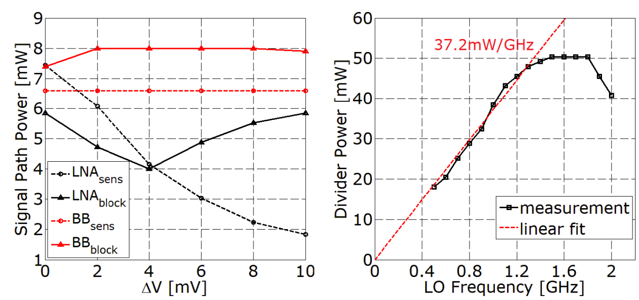

Fig. 13. Power consumption of the signal path (LNA and baseband) for different offsets, and the clock path (divider) across RF frequencies.

divider outputs to the gates of the mixer switches. It was required to fit eight such capacitors (i.e., for each phase of the divider) into the 6-μm pitch of RF unit. This was very challenging to do with the MIM capacitors due to their large minimum size. Metal–oxide–metal capacitors were not available in the process design kit (PDK). Therefore, we used high-density small nMOS capacitors for ac-coupling. However, their parasitic capacitance was not property modeled in the PDK. Our postlayout extraction results were inaccurate and the measured divider power consumption was 2.7 times larger.

B. Frequency Response of RF and Baseband Gains

Fig. 10 shows the measured RF gain of the front end at different offsets between the RF units. The gain has been measured between 0.7 and 1.4 GHz. The lower bound of frequency is defined by the high-pass nature of the ladder, while the upper bound is limited by the divider operation explained above. Upon the dc-offset between the slices, the gain of the front end can be reconfigured between 20 and 36 dB.

The baseband filtering profile is also shown. The 3-dB cutoff frequency is 10 MHz, and 30-dB attenuation is obtained at 100 MHz. Therefore, blockers are placed at this offset in the compression and linearity measurements to be described later. Some overshoot is observed in the gain characteristics, which is due to the deviation of the R and C values of the TIA from the intended design after fabrication.

C. Noise Figure and 1-dB Compression Point

Fig. 11 shows the NF measurements across the operating frequencies, for the low-noise configuration (i.e., $\Delta V = 0$ V) both in sensitivity and with a blocker at 100-MHz offset resulting in 1-dB compression ($P_{1\ dB}$). The NF remains within 1.0–2.8 dB until 1.3 GHz and starts increasing at 1.4 GHz because of the issues with the divider. The average NF from 0.7 to 1.3 GHz is 1.9 dB. In the presence of $P_{1\text{ dB}}$ blocker, the maximum NF increases to 7.9 dB. Fig. 11 also shows the increase in the NF for increasing ΔV. The NF increases by 13 dB from $\Delta V = 0$ V (i.e., $V_{\text{ladder}} = 0$) to $\Delta V = 10$ mV (i.e., $V_{\text{ladder}} = 0.5$ V). Fig. 12 shows the $P_{1\text{ dB}}$ for different offset configurations, extracted from the normalized gain curves, when the LO frequency is 900 MHz and the blocker is placed at a 100-MHz offset. The compression point increases from −8.5 to 10.5 dBm (by 19 dB) as ΔV is varied from 0 V to 10 mV. Note that with increasing ΔV, the $P_{1\text{ dB}}$ increases faster than the NF, therefore the DR also increases. At the maximum offset of $\Delta V = 10$ mV, the benefit in the DR becomes 6 dB, considering that the NF increases by only 13 dB while $P_{1\text{ dB}}$ improves by 19 dB. This is the measured proof of the QA concept. In fact, the baseband in the proposed system is not quantized and is still limited by the supply voltage; therefore, its noise prevents the system from taking a full advantage of the DR expansion of the quantized front end. However, even 6-dB improvement is equivalent to a four times power saving.

D. Power Consumption

Fig. 13 shows the current consumption for the LNA and baseband at different offsets in the ladder. In each case, currents are measured for two configurations; with no blocker (i.e., sensitivity) and in the presence of $P_{1\text{ dB}}$ blocker. LNA operating from a 0.8-V supply consumes a maximum power

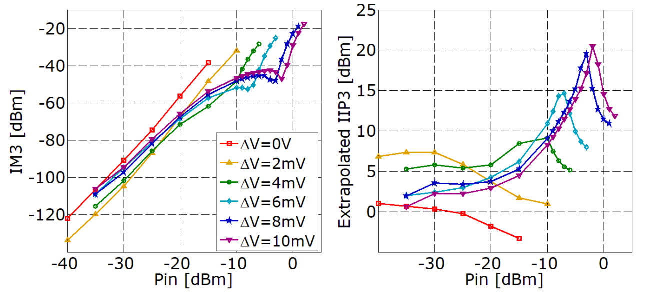

Fig. 14. IM3 measured at 2 MHz, with two input tones at 702 and 800 MHz, and LO frequency of 900 MHz, and IIP3 extrapolated from the given input power in each case.

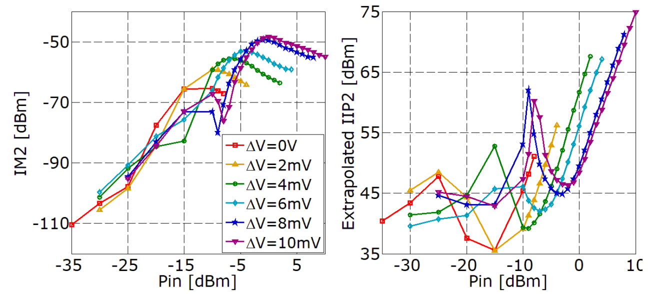

Fig. 15. IM2 measured at 2 MHz, with two input tones at 1002 and 1000 MHz, and LO frequency of 900 MHz, and IIP2 extrapolated from the given input power in each case.

of 7.4 mW in sensitivity for zero offset ($\Delta V = 0$ V), which drops to about 2 mW for the largest offset ($\Delta V = 10$ mV) as expected. In the presence of $P_{1\text{ dB}}$ blocker at larger offsets, the dynamic power burned in the mixer capacitances increases the LNA consumption to a maximum of 5.8 mW. The baseband power does not depend on the offset because it only depends on the current entering the TIAs. In the absence of blockers, the current signal downconverted and injected into the TIA is very small, hence the baseband operating from a 1-V supply consumes 6.6 mW. In the presence of $P_{1\text{ dB}}$ blockers, the current injected into the TIA increases and so the power rises to 8 mW. Then overall signal path consumes 14 mW in sensitivity and 13.8 mW in the presence of the largest blocker.

Divider current is also shown in Fig. 13 across RF frequencies. It increases linearly as expected with 37.2-mW/GHz slope (2.7 times larger than predicted by the postlayout simulations as explained before) and dropping after 1.4 GHz due to the dysfunctional divider.

E. Linearity, IIP3, and IIP2

Linearity of a QA system cannot really be characterized by measures such as IIP2 and IIP3, as due to the averaging of transfer characteristics, the distortion in such system is spread across multiple high-order terms rather than being accumulated around only the lower order ones [57]. However, just to illustrate this point and for the sake of providing a comparison with the literature, IIP2 and IIP3 measurements were performed by sweeping the input power. Fig. 14 shows the IM3 and IIP3 curves obtained from two-tone test, where blockers are placed at 702 and 800 MHz, creating an intermodulation product at 898 MHz, which down-converts to 2-MHz IF frequency with the 900-MHz LO. Note how even for small signal powers, $\Delta V = 2$ mV provides 6 dB better IIP3 than $\Delta V = 0$ V. This is due to the averaging of the transfer characteristics with QA architecture compared to a single inverter [56]. Increasing ΔV further reduces small signal IIP3 because of the gain ripple in transfer characteristics. However, as signal amplitude increases, ripples do not matter anymore, and IIP3 improves again. The power of peak IIP3 increases with increasing offset voltages. As power increases further, compression causes IIP3 to drop again. The overall IIP3 variation is from 1 to 20.5 dBm. A similar behavior can be observed for IIP2 and IM2 plots shown in Fig. 15, obtained from a two-tone test where blockers are placed at 1000 and 1002 MHz, creating a leakage intermodulation product at 2 MHz. Increasing ΔV improves IIP2 at higher signal powers. The overall IIP2 variation is from 35 to 75 dBm.

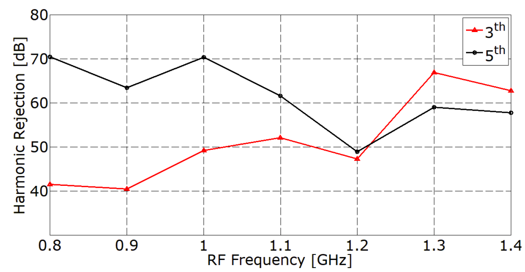

Fig. 16. Third- and fifth-order HRs.

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

	This work	[28]	[29]	[43]
Topology	Quantized RX	Noise Canceling	Transform.-LNTA	Voltage-mode[a]
Area [mm^2]	0.25	5	0.84, 0.74[a]	0.6
Freq. (GHz)	0.7-1.4	0.6-3	1.8, 2.4[a]	0.4-3
Gain [dB]	20.8[b], 36.8[c]	NA	44.5, 45.5[a]	70
NF [dB]	1.9[c]-14.6[b]	1.8[b]-3[b]	3.8, 1.9[a]	1.8-3.1
NF_{blk} [dB]	6.6[c]-7.9[c]	7-9	7.9	14, 10[d]
IIP3 [dBm]	1[b]-20.5[b]	10[a]-11.5[a]	18,16[a]	3,8[d]
IIP2 [dBm]	35[b]-75[b]	49.5[a]-55[a]	64,66[a]	55,80[e]
P_{1dB} [dBm]	-8.5[c], 10.5[b]	-6, -1	-1.5	-13
HR(3rd/5th) [dB]	40-68/50-70	52/54	54/65	40/50, 70/75[e]
Supply [V]	0.8, 1, 1.2	1	1.2, 1.8	0.9
P_{LO} [mW]	37.2/GHz	13/GHz	3.2/GHz	6.8/GHz +5.4
P_{LNA+BB} [mW]	13.7[b], 14[c]	30-46	23.4	14.3
Technology	65nm	28nm	40nm	28nm

[a]Differential., [b]High linearity (ΔV=10mV) [c]Low noise (ΔV=0V) [d]LNA optimized [e]Calibrated

F. Harmonic Rejection

The HR was measured with $\Delta V = 4$ mV and with the IF bandwidth of 2 MHz. Fig. 16 shows the third- and fifth-order HRs across operating frequencies, measured by applying signals to the input at frequencies three times and five times larger than LO frequency (plus 2-MHz IF bandwidth). In this case, 40-68-dB rejection is obtained for the third-harmonic and 50-70-dB rejection for the fifth harmonic.

G. Comparison with the State of the Art

Table I illustrates the comparison of the implemented receiver with the state of the art. The proposed prototype is compared to a mixer-first receiver with an auxiliary noise-canceling path and HR [28], to a receiver with a transformer-based LNTA [29] for achieving swings larger than supply, and to a receiver with a voltage-mode LNA with an impedance up-conversion to help with LNA output compression [43].

V. Conclusion

An RF receiver with a QA front end (QAFE) with a reconfigurable DR and a novel HR architecture is introduced. System reconfigurability allows having NF as low as 1.9 dB and compression point as high as 10.5 dB, while consuming only 14 mW in the signal path. Such high compression point is made possible with the QA architecture despite using voltage-mode LNAs. Voltage-mode operation also facilitates third- and fifth-order HRs in the mixer that is followed by only two baseband TIAs.

Appendix
Effect of the Random Mismatch in the Quantized Front End

To illustrate the effect of the random mismatches on the linearity of the QAFE, we have performed two different set of simulations: one to evaluate the impact on the total harmonic distortion (THD) generated by a large signal and one to evaluate the impact of a large interferer on a small wanted signal (i.e., desensitization test). Such simulations were performed at three different offsets ΔV, $\Delta V = 0$ V (no offset), $\Delta V = 4$ mV (moderate offset), $\Delta V = 10$ mV (largest offset).

Each test was performed twice, once in nominal condition (red curves) and once by using the mismatch models for transistors, mim-caps, and resistors (black curves). The mismatch simulations were performed at only one seed. Due to the complexity of the structure, a comprehensive Monte Carlo analysis over multiple seeds could not be performed. Thus, the main goal of this Appendix is to demonstrate the effect of gain and offset mismatches among the QAFE elements on the overall transfer characteristics rather than providing statistical analysis.

A. Impact on the Total Harmonic Distortion

To evaluate the impact of mismatches on the THD, the entire 100-element QAFE was simulated with the input power swept from -40 to 10 dBm, and the THD was calculated over 100 harmonics.

Fig. 17 shows the simulation results. At no offset (i.e., $\Delta V = 0$ V), the THD performance is identical in both cases (i.e., nominal and mismatch) because all slices operate in parallel at a single bias point. For $\Delta V = 4$ mV, at low input powers, the overall THD improves compared to $\Delta V = 0$ V and the impact of mismatches appears negligible (less than 1 dB variation). This behavior can be explain considering that at $\Delta V = 4$ mV, there is a considerable overlap among the characteristics that not only averages non-linearities but also the impact of mismatches. In fact, since the inverter's input range is around 80 mV, with $\Delta V = 4$ mV there are 20 unsaturated slices overlapped.

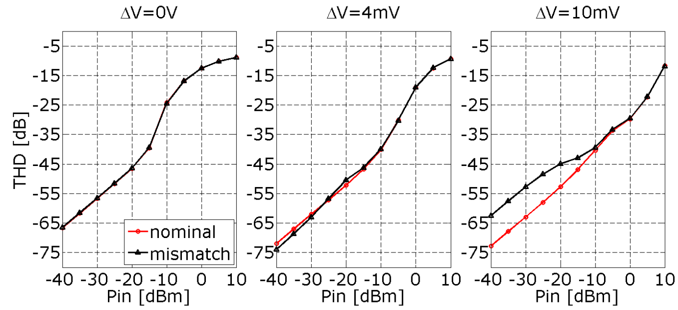

Fig. 17. Effect of mismatches on THD as a function of input power for different offsets among the QAFE elements.

For $\Delta V = 10$ mV and low input powers (lower than -10 dBm), there is a considerable difference in THD (around 10 dB) between nominal and mismatched cases, this is because the number of overlapped elements is smaller compared to the previous case (e.g., eight inverters, if the input range is 80 mV as considered before). The mismatches substantially nullify the averaging of small signal non-linearities and the THD tends to the case with no overlap. On the other end, at larger input powers, the impact of mismatches diminishes again, this time because larger signal explores more slices by shuffling multiple gain characteristics and so by averaging out the differences again. Despite the discrepancies at low powers, it is worth mentioning that the compression point for $\Delta V = 10$ mV is 10.5 dBm. This implies that if this mode is used, the signal power is probably already above -10 dBm and, hence, effect of the mismatches is negligible. Consequently, if system is used as intended (i.e., adapted to the input-signal power) mismatches should not impose a significant problem from this prospective.

B. Impact on the Desensitization

The impact of a large interferer on a small wanted signal can be characterized through the desensitization test as shown in [64]. Typically, in an amplifier, the presence of a large signal along with a small wanted signal leads to a sort of "swing" of the operating point by affecting the small-signal gain (eventually by reducing it). In the case of the QAFE, the presence of large blockers has a similar effect because the instantaneous value of the voltage signal at the input defines which amplifiers are active at a given time. In this case, the presence of mismatches can affect the overall signal gain. To characterize this effect, a desensitization simulation test was performed with and without mismatches among the lines. Fig. 18 shows the small signal gain as a function of blocker input power (for $\Delta V = 0$ V, $\Delta V = 4$ mV, and

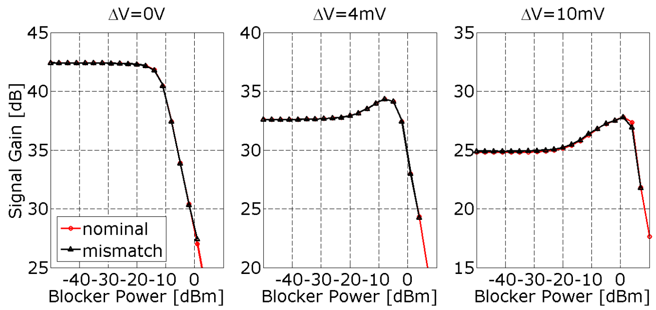

Fig. 18. Desensitization of the small signal gain as a function of the blocker input power for different offsets among the QAFE elements, with and without the effect of mismatch.

$\Delta V = 10$ mV). The small signal at −60 dBm signal at 1.8 GHz is applied to the input along with the blocker at 2 GHz, its power being swept from −50 to 10 dBm. In this case, mismatches do not have a significant impact on the small signal gain even at large offsets. This is because even in the case of the largest $\Delta V = 10$ mV, there is still an overlap of 8 units and mismatches among the lines are averaged by exploring several lines.

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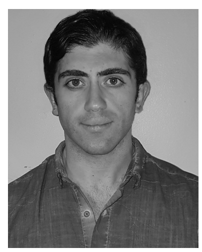

Javid Musayev was born in Baku, Azerbaijan, in 1988. He received the B.Sc. and M.Sc. degrees in electrical and electronics engineering from Middle East Technical University, Ankara, Turkey, in 2009 and 2011, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Toronto, Toronto, ON, Canada, in 2018.

From 2011 to 2013, he was an Integrated Circuit Design Engineer with Mikrosens, Ankara, Turkey. He is currently with Rambus Inc., Toronto, as an Analog Circuit Design Engineer.

Antonio Liscidini (SM'13) was born in Tirano, Italy, in 1977. He received the Laurea *(summa cum laude)* and Ph.D. degrees in electrical engineering from the University of Pavia, Pavia, Italy, in 2002 and 2006, respectively.

He was an Intern with National Semiconductors, Santa Clara, CA, USA, in 2003, where he was studying poly-phase filters and CMOS low-noise amplifiers. From 2008 to 2012, he was an Assistant Professor with the University of Pavia and a Consultant with Marvell Semiconductors, Pavia, in integrated circuit design. In 2012, he was with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada, where he is currently an Associate Professor. His research interests are focused on analog mixed signal interfaces with particular emphasis on the implementations of wireless transceivers and frequency synthesizers for cellular and ultralow power applications.

Dr. Liscidini was a member of the International Solid-State Circuit TPC from 2012 to 2017 and has been the European Solid-State Circuit Conference TPC since 2010 and Custom Integrated Circuit Conference TPC since 2018. He was a recipient of the Best Student Paper Award at the IEEE 2005 Symposium on VLSI Circuits and a co-recipient of the Best Invited Paper Award at the 2011 IEEE Custom Integrated Circuit Conference. He has served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS from 2008 to 2011 and from 2017 to 2018 and as a Guest Editor for the IEEE JOURNAL OF SOLID-STATE CIRCUITS in 2013 and 2016, and the *IEEE RFIC Virtual Journal* Issue dedicated to frequency synthesizers. From 2016 to 2018, he was a Distinguished Lecturer of the IEEE Solid-State Circuits Society.