A Reconfigurable Passive Switched-Capacitor TX RF Front End With −57 dB ACLR2

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***Abstract*—This letter presents a wireless transmitter (TX) front end in which the functionalities of digital-to-analog conversion, baseband filtering, and signal upconversion are implemented by a passive switched-capacitor (PSC) network. The result is a versatile architecture that fully benefits from CMOS scaling. The front end was integrated in a 65-nm CMOS technology and can support various channel bandwidths simply by adjusting the switching frequency for the PSC network. Thanks to its third-order reconfigurable filter, it maintains a thermal noise floor better than −156 dBc/Hz at a power dissipation of 45 mW. The measured prototype achieves an ACLR2 of −57 dB and an EVM of −31 dB for a 20-MHz 64-QAM OFDM and a 20-MHz 16-QAM signal, respectively.**

***Index Terms*—ACLR, CMOS, DAC, discrete time, EVM, filter, low-power, out-of-band noise, passive-switched-capacitor (PSC), SAW-less, transmitter (TX), wireless transmitter.**

I. Introduction

The allocation of new frequency bands in the already congested sub-6-GHz spectrum calls for transmitters (TX) with tighter spurious and noise emission requirements. On the one hand, analog TX [1] have demonstrated superior performance in terms of out-of-band emissions, but lack in reconfigurability and do not fully take advantage of technology scaling. On the other hand, digital TX architectures are more flexible, but need high-resolution DACs (at least 12 bits) and high sampling rates (at least 500 MHz) [2] or long FIR filter taps (greater than 100) to meet the strict out-of-band emission requirements [3]. However, digital approaches have demonstrated some promising results, such as the switched-capacitor power amplifier with harmonic rejection (HR SCPA) proposed in [4] and the 1-bit $\Delta\Sigma$-FIR DAC TX demonstrated in [3].

The work of [5] introduced the idea of the rotating sampling capacitor to implement a first order IIR filter for a wireless receiver. Later, the concept of incremental charge signalling using a charge-based DAC (QDAC) [6] opened a new path toward a more passive and scalable solution. Our work follows the same path, adding more features in terms of bandwidth flexibility and filter performance. In particular, the DAC is merged with a higher order passive switched-capacitor filter (PSC-DAC) resulting in three times better noise suppression without suffering from the limiting tradeoff between signal amplitude and bandwidth inherent in the QDAC architecture [6]. Compared to the HR SCPA [4] and $\Delta\Sigma$ implementations [3], the digital baseband operates at a much lower rate without the need for long FIR taps. Hence, the proposed front end aims to address the above-mentioned issues of digital TX by taking advantage of PSC techniques in order to relax the number of required DAC bits, lower the baseband sampling rate, and offer a high degree of bandwidth flexibility without compromising the output noise performance.

This letter is structured as follows. Section II compares various digital TX frequency responses to the proposed PSC-DAC scheme. Section III elaborates on the system architecture while Section IV discusses the experimental results. Finally, the conclusion of this letter is presented in Section V.

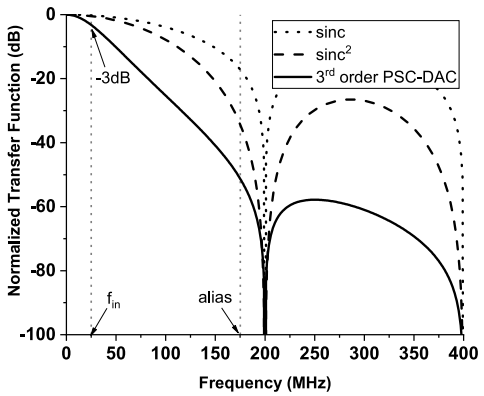

Fig. 1. Filtering profiles for $f_{clk} = 200$ MHz and $f_{\text{in}} = 25$ MHz.

II. Filter Profile Investigation

The poor out-of-band performance of digital TX originates from the absence of analog filtering in the transmit path. Fig. 1 plots the sinc response of a typical radio-frequency DAC (RFDAC), the sinc^2 of a QDAC [6], and the proposed PSC-DAC response in the frequency domain. The PSC-DAC combines the responses of a sinc and a third-order low-pass filter with real poles resulting in almost 20 dB more alias suppression than the sinc^2. Higher oversampling ratios (f_{clk}/f_{in}) improve the effectiveness of the proposed filtering arrangement. In fact, more than 10-dB improvement can be obtained for oversampling ratios of 6 and above.

The observed 3-dB drop at the edge of the passband in Fig. 1 may be undesirable and can be mitigated by a more elaborate PSC network allowing for a maximally flat (Butterworth) response or by increasing the filter cutoff frequency at the expense of alias and noise attenuation. Alternatively, this drop can be corrected by applying digital predistortion (DPD) on the TX.

III. System Architecture

The architecture of the proposed TX front end is illustrated in Fig. 2. The chip consists of a synthesized custom SRAM with SPI controller, four time-interleaved 11-bit PSC-DACs, an IQ voltage passive mixer with 25% duty-cycle clocks, and an open-drain driver amplifier (DA) providing 18 dB of power control. The existence of two separate clock generators allows the center frequency, f_{LO}, to

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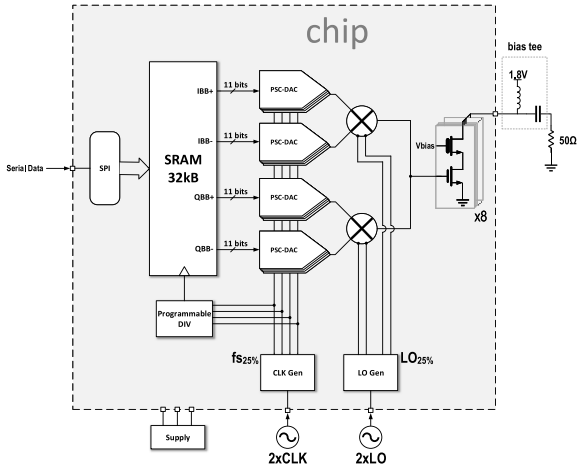

Fig. 2. Proposed TX system block diagram.

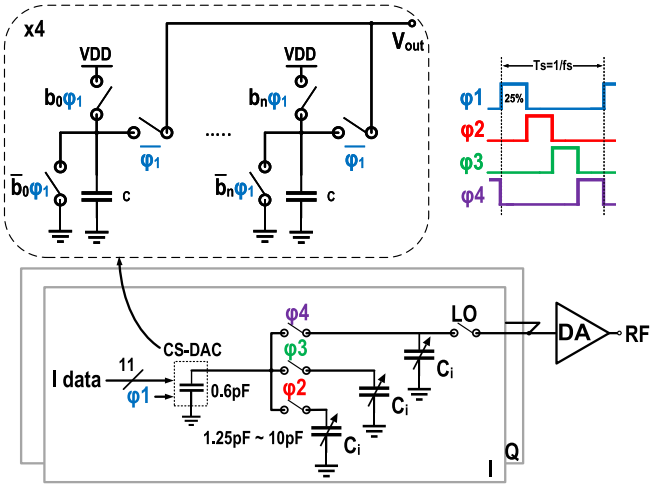

Fig. 3. PSC-DAC circuit schematic with 4× time-interleaving.

be chosen independently from the channel bandwidth, which is an advantage over other implementations (e.g., [6]).

Fig. 3 shows the schematic of the PSC-DAC. It consists of a four-phase PSC network encompassing a charge-sharing DAC (CS-DAC). For filtering purposes, the CS-DAC acts as a capacitor, C_s, whose charge is shared among the programmable integrating capacitors, C_i, during each of the phases ϕ_2–ϕ_4 in a similar fashion to [5]. The operation of the CS-DAC is as follows: during ϕ_1 each of the capacitors is either charged to V_{DD} or ground depending on the value of the corresponding bit. At the end of ϕ_1, all capacitors are connected in parallel forming a total capacitor C_s which holds the analog voltage equivalent of the supplied digital code. Despite the simplicity of the graph in Fig. 3, the CS-DAC was designed with 5 thermometer-coded MSB to guarantee monotonicity against glitches and a series bridge capacitor was inserted to minimize the total capacitance of the DAC. Care was taken in the sizing of the switches in order to maintain the bandwidth while being mindful of charge injection.

Under the same conditions as in [7], the entire PSC-DAC can be represented by the continuous-time equivalent circuit shown in Fig. 4. It is straightforward to prove that the PSC-DAC operates as a third-order filter with three real poles at: $f_o = (f_s C_s / 2\pi C_i)$. When upconverted, this frequency determines the RF channel bandwidth, which can be precisely adjusted by changing either f_s or C_i. Please note that the input capacitance of the DA has a negligible effect on the

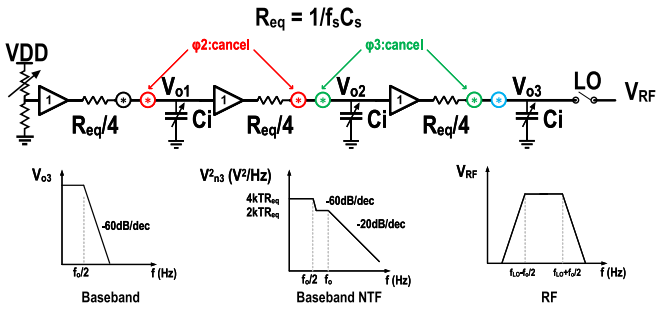

Fig. 4. Continuous-time model capturing noise, baseband, and RF transfer functions.

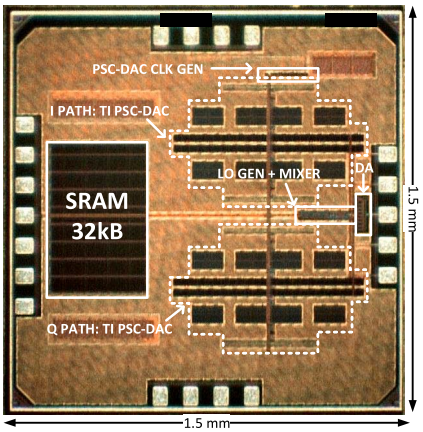

Fig. 5. Chip micrograph.

channel bandwidth since C_i is typically orders of magnitude larger. Achieving wider bandwidths requires a higher f_s which translates to tight settling requirements for the switches of the PSC-DAC. An elegant solution to this problem is time interleaving [7] which effectively reduces the equivalent resistance and boosts the bandwidth, as illustrated in Fig. 4, without any changes in the switch size.

What is even more interesting is that the model reveals that the switch thermal noise associated with phases ϕ_2 and ϕ_3 is fully correlated and cancels out, leaving only the noise of the last switch to dominate, which is filtered by −20 dB/dec (the noise due to ϕ_1 is filtered by −60 dB/dec). This information allows the designer to choose the optimal $R_{\mathrm{eq}} = (1/f_s C_s)$ to meet the thermal noise requirements of the TX. System simulations including both quantization and thermal noise predict less than −160 dBc/Hz output noise at 45-MHz offset from the carrier with 11 bits, $f_{clk} = 250$ MHz, $f_s = 1$ GHz, and a capacitor ratio C_i/C_s of 16. In the fabricated prototype C_s is 0.6 pF including parasitics and C_i can be set to a maximum value of 10 pF.

IV. Experimental Results

Fig. 5 shows the micrograph of the fabricated TX. The chip was fabricated in TSMC 65-nm CMOS process and occupies 1.5×1.5 mm^2 including the pads. The active area excluding the SRAM and SPI blocks is 0.5 mm^2 dominated by the time-interleaved baseband cores. By maintaining the same target frequency and bandwidth, time interleaving could be avoided in a 28-nm CMOS process similar to the one used by [6], thus reducing the area below 0.2 mm^2.

Fig. 6 plots the measured normalized transfer function of the PSC-DAC and confirms the bandwidth reconfigurability of the front end. The transfer function follows a −18 dB/oct slope, as expected from a third-order filter. The maximum achievable 3-dB cutoff frequency is 24 MHz (not depicted in Fig. 6), which corresponds to a 48-MHz RF

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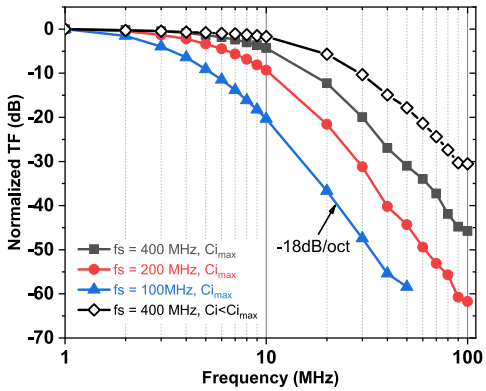

Fig. 6. Measured transfer functions for various f_s and C_i values.

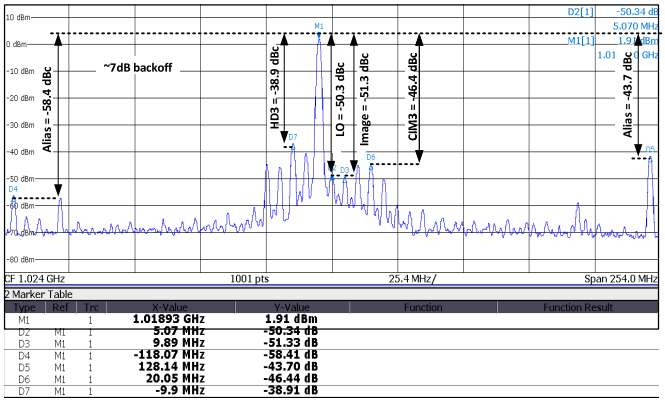

Fig. 7. Measured output spectrum for a 5-MHz tone: $f_{\mathrm{LO}} = 1.024$ GHz, $f_s = 4 \times 256$ MHz, and $f_{clk} = 128$ MHz.

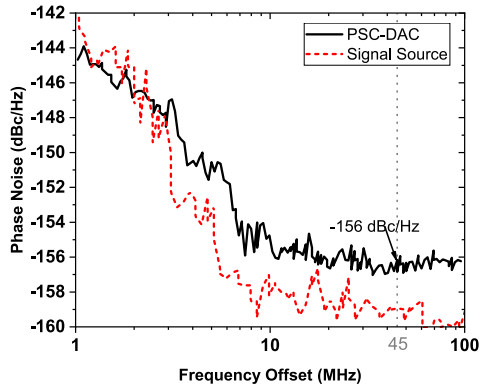

Fig. 8. Measured output noise for 0-dBFS static input ($P_{\mathrm{out}} = 9.5$ dBm, $f_{\mathrm{LO}} = 1$ GHz, and $f_s = 4 \times 320$ MHz).

channel and is limited by the external signal source and the on-chip frequency divider.

Spectrum measurements of a 5-MHz tone in Fig. 7 reveal an LO leakage and image better than −50 dBc after LO and IQ calibration. The apparent third-order distortion quantified by HD3 and CIM3, is attributed to a malfunctioning bit in the thermometer decoder used in the MSB part of the PSC-DAC, which can be reduced by dithering or DPD. The observed upper sideband alias attenuation of −43.7 dB is approximately 17 dB worse than expected. This was the result of a wrong estimation of switch parasitics which led to poor switch isolation in the baseband. Please note that the above observations do

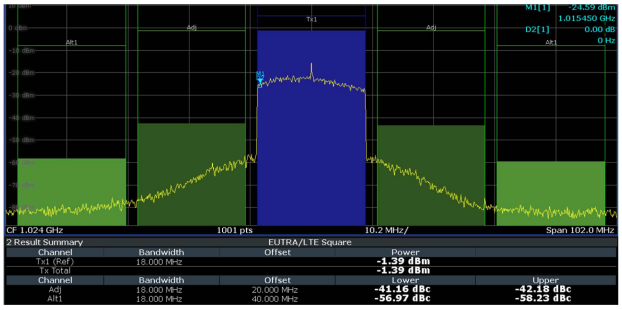

Fig. 9. Measured ACLR for 64-QAM OFDM. Measurement conducted at $f_{\mathrm{LO}} = 1$ GHz, $f_{clk} = 160$ MHz, and $f_s = 4 \times 320$ MHz (test setup losses not de-embedded).

TABLE I
COMPARISON WITH STATE-OF-THE-ART

	[1]	[3]	[4]	[6]	This Work
Topology	Analog	ΔΣ-FIR DAC	HR SCPA	QDAC	**PSC-DAC**
Bandwidth [MHz]	20	20	20	20	**20**
f_{LO} [GHz]	0.85[a]	0.9	0.9	1	**1**
Peak Power [dBm]	6	4.6	25.6	6[b]	**9.5**
Average Power [dBm]	2.8	-1.5	18.6[c]	1	**2.5**
CIM3 [dBc]	N/A	-49	-42[d]	-52	**-46**[e]
LO feedthrough [dBc]	N/A	-59	N/A	-46	**-50**
Image [dBc]	N/A	-60	N/A	-44	**-51**
Signal	LTE10	LTE20	16-QAM	OFDM[f]	**64-QAM OFDM**[g]
EVM [dB]	-37	-36.5	-26.1	N/A[h]	**-31**[e,i]
ACLR1/ ACLR2	-43.4/-54.4	-34/-43	N/A	-42/-47	**-41/-57**
PN @ offset [dBc/Hz]	-159 @45MHz	-125 @200MHz[c]	-137 @40MHz	-155 @45MHz[j]	**-156 @45MHz**[k]
P_{DC} [mW]	98	38.3	2250[l]	41.3	**45**
Active area [mm^2]	1.15[m]	0.047	3[m]	0.25	**0.5**[n]
Technology	55LP	28nm FD-SOI	65nm	28nm	**65nm**

[a] Band 5. [b] Limited by maximum DAC capacitance. [c] Estimated from reported data. [d] HD3. [e] Limited by decoder error. [f] PAPR = 7 dB. [g] PAPR = 9 dB. [h] Insufficient memory. [i] 16-QAM. [j] CW test. [k] Static test. [l] Based on reported system efficiency. [m] Estimated without on-chip baluns. [n] Limited by time-interleaving.

not represent fundamental limitations of the PSC-DAC concept, but rather implementation errors in the fabricated prototype.

In order to characterize the out-of-band performance of the TX, phase noise and ACLR tests were performed. The former aimed to capture the noise produced by the filter and the RF blocks (excluding quantization noise). The latter aimed to verify the effectiveness of the proposed filtering approach on a modulated signal which also includes distortion and quantization noise. For phase noise measurements, the PSC-DAC was configured with a dc input of 0 dBFS achieving −156 dBc/Hz at a 45-MHz offset, which was close to the measured phase noise of the external signal source, as shown in Fig. 8. At −6 dBFS, the phase noise degradation was found to be less than 1 dB.

Fig. 9 shows the ACLR measurement for a 20-MHz 64-QAM OFDM channel with setup losses included. The measurement was conducted without DPD, offset or IQ gain/phase compensation, which is reflected in the asymmetry of the main channel and the existence of a center peak due to LO leakage. However, the excellent filtering performance of the PSC-DAC is confirmed by the −57 dB ACLR2 in the alternate channel.

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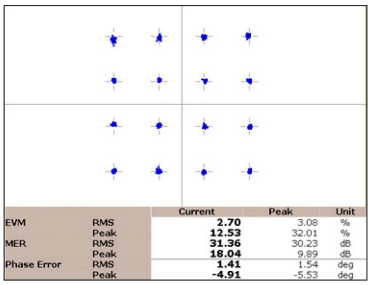
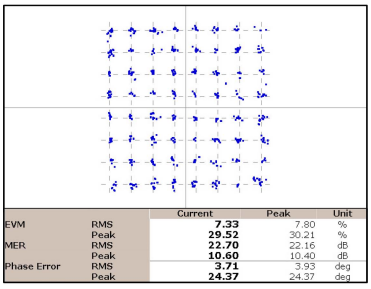


(a)



(b)

Fig. 10. Measured constellations without DPD at 2.5 dBm average power after compensating for setup losses ($f_{clk} = 160$ MHz and $f_s = 4 \times 320$ MHz). (a) 16-QAM: EVM $= -31$ dB at 1.024 GHz. (b) 64-QAM: EVM $= -22.7$ dB at 960 MHz.

Finally, in-band performance is shown in Fig. 10 at 2.5-dBm average output power (after loss de-embedding). Measured error vector magnitude (EVM) for a 16-QAM signal at 16 MSym/s is −31 dB without DPD. The poor EVM performance of a 64-QAM signal (measured at −22.7 dB) is attributed to distortion and quantization noise introduced by a malfunctioning bit in the binary-to-thermometer decoder in the CS-DAC.

Table I summarizes the measured performance of the proposed TX front end. At approximately 50% less power and a third of the silicon area, it achieves out-of-band performance comparable to [1]. Despite the technology node adopted, which required an increase in power and area due to time interleaving, the proposed solution achieves the best ACLR2 at total power dissipation comparable to [6]. It also outperforms the HR SCPA [4] and the $\Delta\Sigma$-FIR DAC [3] in terms of EVM and ACLR, respectively.

V. Conclusion

A 45-mW reconfigurable wireless TX front end in 65-nm CMOS was presented. Employing PSC filtering techniques, it achieved −57 dB of ACLR2, −41 dB of ACLR1, and −31 dB of EVM. The measured thermal noise floor was −156 dBc/Hz limited primarily by the testing equipment. Embedding the filter inside the PSC-DAC allows for easy reconfigurability of the channel bandwidth by adjusting the sampling frequency, f_s. Finally, the filter order can be extended further simply by adopting an extra clock phase and integrating capacitor, C_i.

Acknowledgment

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