A Low-Power Sub-GHz RF Receiver Front-end with Enhanced Blocker Tolerance

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***Abstract*—This paper presents a class-AB sub-GHz RF receiver front-end suitable for ultra-low power application. By exploiting transistors' class-AB operation in both the RF and baseband sections, the receiver front-end achieves a very low sensitivity and an elevated blocker tolerance while keeping a low power consumption. Such performance makes the receiver suitable for both short-range (e.g. 802.15.4) and long-range (e.g. LoRa) applications. The proposed RF front-end has been implemented in 0.13um CMOS technology, operates in the 868/915MHz ISM bands, and exhibits an in-band gain of 50dB, noise figure of 2.7dB, out-of-band IIP3 of +2dBm, out-of-band IIP2 of +37dBm, out-of-band P1dB of -10.5dBm, while draining 2.1mA from a 1.2V supply.**

I. Introduction

The emerging development of Internet of Things (IoT) has opened up a huge market for sub-GHz applications in areas such as sensor networks, smart cities and personal health monitoring systems. Sub-GHz wireless systems have several advantages over their 2.4GHz counterparts including longer operation range and lower power consumption, which make them a popular choice for IoT applications. The trend in recent works [1], [2] for IoT receiver design is to primarily target ultra-low power consumption (sub-mW) while sacrificing the performance in sensitivity and linearity (i.e. the radio spurious free dynamic range SFDR). Though a low power consumption is important for battery-powered systems, worse sensitivity reduces the operative range by making such solutions not compliant with low power wide area networks (LP-WAN) [3]. Moreover, a reduction in linearity compromises the co-existence with other devices, especially in the presence of large interferers.

To address the above issues, we designed a sub-GHz RF receiver front-end which deeply relies on class-AB operation to enhance its sensitivity and blocker resilience. Such approach allows the design to have the best in-class sensitivity and SFDR while keeping the overall current consumption around 2mA from a 1.2V supply. The paper is structured as follows: In section II the receiver architecture is presented. In section III detailed circuit implementations are reported with particular emphasis on the low-noise amplifier (LNA) and the class-AB filtering trans-impedance amplifier (TIA). The paper ends with the measurement results and a comparison with the state-of-the-art.

II. Receiver Front-end Architecture

Recently, RF receivers exploiting class-AB LNA have shown to achieve a promising performance in power usage efficiency and blocker tolerance [4], [5]. The goal of the proposed solution is to extend the use of class-AB operation to the entire RF front-end. The structure of the proposed receiver is shown in Fig. 1. The LNA is followed by a pair of passive current mixers to implement a low-IF quadrature down conversion scheme. As typically happens in ultra-low power RF front-end, the LNA is single-ended. This choice reduces the power consumption of the RF section and avoids the use of an external balun, which would degrade the RX sensitivity with its insertion loss. The passive mixers, driven by a 25% duty-cycle clock, perform also a single-ended to differential conversion by making the remaining part of the receiver fully differential. An on-chip divider is designed to generate non-overlapping phases from an external LO. The receiver is completed by the analog baseband section where the down-converted current is sensed by a class-AB filtering TIA ac-coupled with a further filtering stage which makes the receiver fully compliant with the 802.15.4 blocker profile.

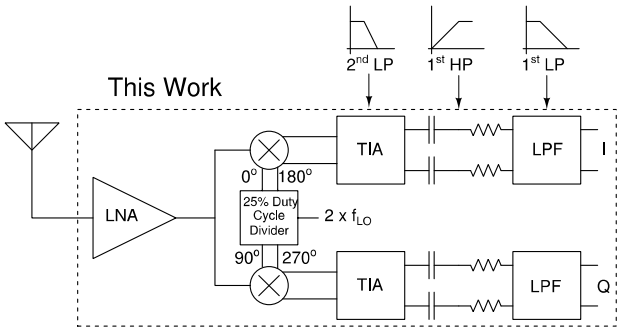

Fig. 1. RX Front-end Block Diagram

In the absence of large interferers, both the LNA and TIA will work in class-A drawing minimum current from the power supply. When large signals show up at the input of the receiver, both the LNA and TIA will operate in class-AB by handling the blockers without saturating the system. The LNA output and the TIA input are biased at the same dc value to ensure that nominally zero dc current flows through the mixer switches [6]. This eliminates the need for large decoupling capacitors at the input of the passive mixers to minimize the impedance seen by the LNA. As a result, the LNA experiences a low output voltage swing even in the presence of large blockers since its load is dominated by the low input impedance provided by the TIA, which is up-converted to the LNA output via the mixer [6]. This strategy avoids gain compression at the output of the LNA and improves linearity.

The TIA, with a 2^{nd} order filtering capability, is able to attenuate large out-of-band blockers at an early stage which greatly improves out-of-band linearity. The TIA together with the channel selection filter create an overall 3^{rd} order

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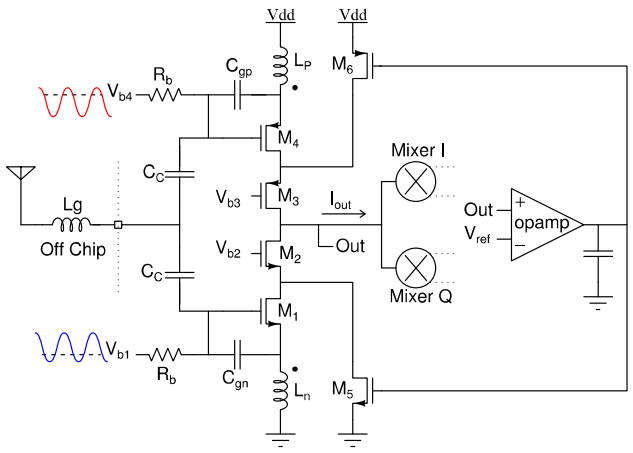

Fig. 2. Class-AB PN Complementary LNA

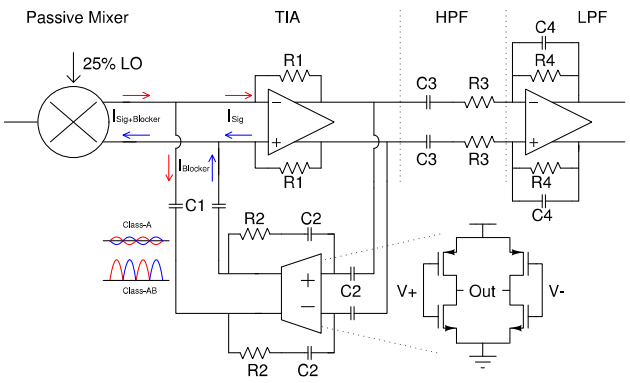

Fig. 3. Class-AB Baseband Circuit

Butterworth filtering profile for the receiver front-end. Image rejection will be performed in the digital domain through IQ recombination. With an IF of 800KHz, the baseband signal spans between 200KHz and 1.4MHz. A high-pass filter with a cut-off frequency of as high as 200KHz is sufficient to filter the dc-offset and 1/f noise. The high-pass filter is realized with a passive RC circuit between the TIA and channel selection filter.

III. Circuit Implementations

A. Class-AB PN Complementary LNA

The classical inductive-degenerated cascode LNA has been widely used for narrow band applications because of its high gain and low noise performance. Several techniques have been proposed to modify this classical topology to reduce its power consumption and increase its linearity. One of them is the current re-use technique where an n-MOS stage and a p-MOS stage share the bias current thereby increasing the effective g_m for a given bias current [7]. In the design proposed in [7] the structure was biased to operate only in class-A with a limited blocker tolerance. Increasing the gate-source overdrive voltage can improve the linearity, but the bias current should be increased as well. To enhance blocker tolerance without sacrificing power consumption, the LNA can be biased in class-AB [4], [5].

The proposed LNA in Fig. 2 uses the PN complementary structure which simultaneously achieves current re-use and class-AB biasing. The complementary transistors M1 and M4 operate in the weak inversion region to maximize the g_m/I_d ratio. p-MOS transistors are sized two times larger than n-MOS transistors to compensate for their smaller mobility. In order to reduce the area of the design, Ln and Lp inductors are realized through an integrated transformer and coupled each other. The g_{mn}/C_{gn} and g_{mp}/C_{gp} ratios have been designed to be approximately the same so that a 1:1 transformer could be used thereby simplifying the layout and having a full symmetric structure. At sub-GHz frequencies, an off-chip inductor (L_g) is required to resonate the input network and provide the required input impedance matching. The LNA's dc output voltage is set through a current-mode feedback injecting into the source of M3 and M2. The current-mode approach simplifies the compensation of the feedback loop and reduces the parasitic capacitance introduced by the biasing network.

B. Baseband TIA and LPF

Fig. 3 shows the detailed baseband circuit design, which consists of a 2^{nd} order active TIA, a 1^{st} order passive high-pass filter, and a 1^{st} order active low-pass filter. Since the TIA is the first baseband stage, its input impedance, noise and linearity can critically affect the performance of the overall chain. A low input impedance is necessary to ensure the theoretical conversion gain of the mixer by maximizing the signal transfer between the RF and BB. It also limits the voltage swing at the output of the mixer to reduce the modulation on the switch resistance when large blockers are present. The goal of the TIA design is to achieve a high gain in the signal band to suppress the noise coming from the following stages, and to provide a high attenuation in the stop band to reject large interferers.

The TIA in Fig. 3 was originally introduced in [8] and has been shown to exhibit an excellent self-adaptive blocker cancellation capability. This TIA has a 2^{nd} order low-pass filter response. In the filter pass-band, the feedback path is open (since it's ac-coupled through capacitor C_1) and the current signal goes through the feed-forward operational amplifier (Op-Amp) with a trans-impedance gain of R_1. On the other hand, in the filter stop-band, the interferers are absorbed by the feedback path through the capacitor C_1. The two real zeros in the feedback network (created by C_1 and R_2C_2) become complex conjugate poles in the close-loop transfer function. Therefore, the TIA can be configured as a 2^{nd} order Butterworth filter. As proposed in [8], the OTA in the TIA's feedback path has been implemented with a complementary topology operating in class-AB. As a result, the TIA can achieve a low power consumption and low noise during the sensitivity test and a high blocker tolerance in the presence of large blockers [8]. Notice that, the particular low in-band noise of this topology allows the trans-conductance gain of the LNA to be limited to less than 40mS. This approach not only saves power in the LNA itself but also scales up the impedance level of the filter without saturating the receiver chain. A larger impedance reduces both the area of the baseband section and the power consumption in the output stage of the feed-forward Op-Amp.

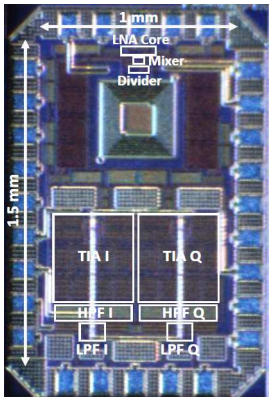

Fig. 4. Die Photo

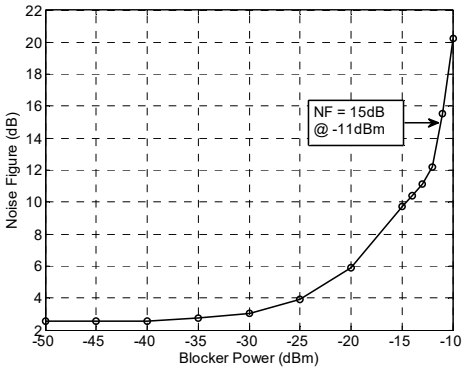

Fig. 7. Noise Figure vs. Blocker Power at [LO+50MHz]

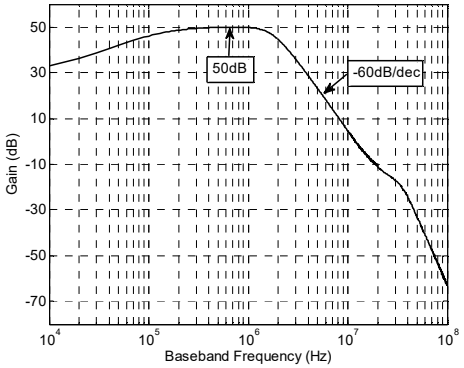

Fig. 5. Transfer Function

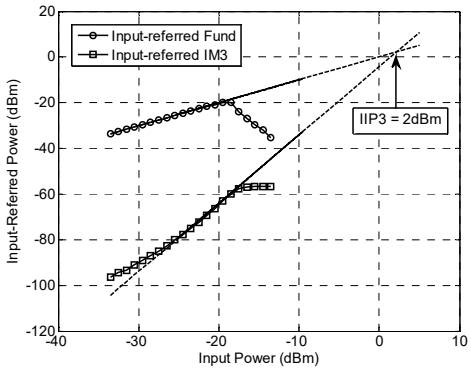

Fig. 8. IIP3 – Two Tones at [LO+50MHz, LO+99MHz]

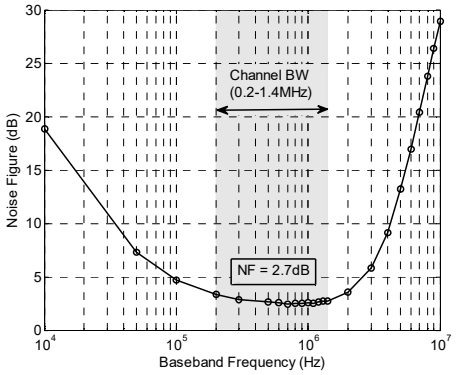

Fig. 6. Noise Figure

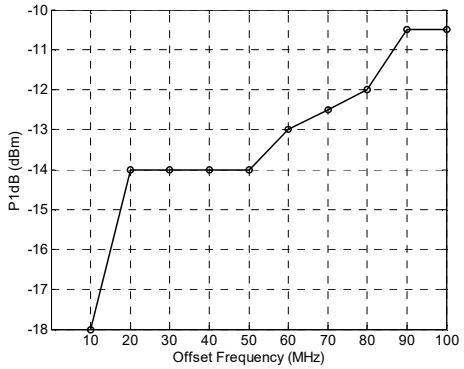

Fig. 9. P1dB vs. Blocker Offset Frequency from LO

The 1^{st} order passive high-pass filter created by R_3C_3 is responsible for eliminating the dc-offset and 1/f noise in the baseband. The 1^{st} order active low-pass filter introduces another real pole to the baseband filtering so that the baseband circuits achieve an overall 3^{rd} order Butterworth filtering capability.

IV. Measurement Results

The RF receiver front-end prototype was fabricated in 0.13um CMOS technology. It occupies $1\text{mm} \times 1.5\text{mm}$ with an active area of $0.5\ \text{mm}^2$ (Fig. 4). The receiver front-end operates at the 868/915MHz ISM band (S_{11}<-10dB) and consumes 2.46mW in total (0.66mW for LNA, 0.42mW for 25% duty-cycle divider, and 1.38mW for IQ baseband circuits).

The measured transfer function (Fig. 5) shows that the receiver front-end achieves a 50 dB gain in the signal band and a 3^{rd} order Butterworth filtering profile in the stop band.

The integrated noise figure (NF) over the signal band is 2.7 dB (Fig. 6). To test the NF in the presence of a blocker, the NF was measured with an out-of-band blocker at [LO+50MHz] and its power swept from -50dBm to -10dBm (Fig. 7). The NF is almost unchanged for blocker <-30dBm, and the NF is below the specification's maximum allowable value (<15dB) for blocker <-11dBm.

All linearity tests were performed at maximum gain. An out-of-band IIP3 (OB-IIP3) of 2dBm was measured by placing two tones at [LO+50MHz, LO+99MHz] (Fig. 8). The measurement was repeated by placing two near-band tones at

Table I. Performance comparison with the state-of-the-art works

	This Work	JSSC 2014 [1]	MTT 2006 [9]	CICC 2012 [10]	RFIC 2014 [11]
Technology (nm)	130	65	180	180	130
Active Area (mm^2)	0.5	0.2	1	0.4	0.12
Architecture	Low IF Single-ended LNA	Low IF Single-ended LNA	DCR Single-ended LNA	DCR/Low IF Differential LNA	Low IF Differential LNA
Frequency (MHz)	868/915[1]	433/860/915/960[1]	915[1]	170/433/868/915/950	960
BW (MHz)	1.2	1.2	1.2	0.01	1.2[4]
Gain (dB)	50	50	30	39	59.6
NF (dB)	2.7	8.1	3	6.5	8.2
OB-IIP3 (dBm)	+2/-2	-20.5	-5[2]	-8[2]	-19
OB-IIP2 (dBm)	+37/+35	-	+45[2]	-	-
OB-P1dB (dBm)	-10.5	-23	-15[2]	-	-
SFDR (dB)[3]	69/66	50	64[2]	74[2]	51[4]
Supply (V)	1.2	0.5	1.8	1.8	1.2
Current (mA)	2.1[5]	1[5]	2	2.3	2.6[5]

1. IEEE 801.15.4 standard 2. In-band linearity test with minimum gain setting 3. $SFDR = \frac{2}{3}(\text{IIP3} - \text{Noise Floor} - \text{NF}) - \text{SNR}_{\text{min}}$ 4. Standard unspecified, number derived based on IEEE 801.15.4 standard 5. Including a clock divider

[LO+10MHz, LO+19MHz] and an OB-IIP3 of -2dBm was measured in this case. The out-of-band IIP2 (OB-IIP2) test was performed for two scenarios. The first one is the beat frequency leakage due to two closely-spaced tones at [LO+10MHz, LO+11MHz] and an OB-IIP2 of +37dBm is measured. The second one is the IM2 product falling in band due to two farther-spaced tones at [LO+10MHz, 2LO+11MHz], and an OB-IIP2 of +35dBm is measured in this case. Such IIP2 value allows the receiver to handle a -6dBm out-of-band blocker (which is above the compression point of the system) without a significant in-band SNR degradation. The out-of-band P1dB (OB-P1dB) was measured by sweeping the power of an out-of-band blocker until the in-band gain was compressed by 1dB. This test was repeated by placing the blocker at different offset frequencies from the LO and the result is shown in Fig. 9. The receiver front-end exhibits a high blocker tolerance. The P1dB is as high as -18dBm even at a near-band offset frequency (10MHz), and it further increases to -10.5dBm as the blocker offset frequency increases to 100MHz.

Due to the limited number of existing works in sub-GHz receiver design and the lack of description in their measurement setups (especially for linearity tests), it is challenging to present a comprehensive comparison of this work with the state-of-the-art. To the best of the author's knowledge, previous works with the most comprehensive measurement results are reported in Table I. Compared to [1], this work consumes more power but achieves a much better performance in both noise and linearity. A similar noise figure was reported in [9], however, its out-of-band linearity tests were not provided, and its in-band linearity tests were performed with minimum gain setting. In [10], comparable power consumption leads to a much higher noise figure in a channel bandwidth 100 times smaller. Such small bandwidth significantly enhances the sensitivity resulting in a high SFDR. Finally the solution presented in [11] did not provide the information regarding the specification, therefore its SFDR was derived based on the IEEE 802.15.4 specification for a fair comparison. Overall, the benefits of the proposed class-AB receiver show the best noise figure and a much higher blocker tolerance compared to the state-of-the-art with a competitive power dissipation.

V. Conclusion

A low power high SFDR sub-GHz RF receiver front-end is discussed. The design exploited the class-AB biasing in both the RF and baseband sections, resulting in the best in-class sensitivity (required for the emerging long-range applications) and an excellent blocker tolerance.

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