A 150-μW 3rd-Order Butterworth Passive-Switched-Capacitor Filter with 92 dB SFDR

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Abstract

For the first time, complex conjugate poles are integrated on silicon by using only switches and capacitors. A general design methodology is proposed to implement low-pass transfer functions with sharper frequency profile compared to the passive-switched-capacitor topologies present in the literature. Theory and simulation results are validated through the measurements of a 0.13μm prototype filter. The 3rd-order filter has a cut-off frequency of 540 kHz, an integrated input referred noise of 17μV and out-of-band IIP3 of 55dBm, while consuming 150μW in the phase clock generator. **Keywords:** passive-switched-capacitor, complex conjugate poles, low-pass filter, CMOS, discrete-time, IIR, high linearity, low noise.

Introduction

While digital designs directly benefit from the technology scaling, their analog counterparts have to face new challenges related to a lower voltage supply and poor intrinsic transistor gains. In this scenario, passive-switched-capacitor filters (PSCF) can be an attractive solution for the implementation of channel selection filters in wireless receivers [1-6]. These filters inherit the advantages of switched-capacitor filters but avoid the use of active components, which sets severe constraints in the creation of an arbitrary filtering profile. For example, the 7th-order PSCF shown in Fig. 1(a) can only realize real poles resulting in smooth band-edge transition [1].

Recently PSCF with complex conjugate poles have been published in literature [2], [3] both providing only simulation results. However, approach proposed in [2] lacks of a general methodology for the filter design, while [3] proposes a straightforward way to realize a pair of complex conjugate poles only with a maximum quality factor (Q) of $1/\sqrt{2}$. In this work, the limitation of the Q achievable will be addressed and for the first time, a comparison between theory, simulation and measurements will be provided, by validating the model introduced in [3]. The proposed approach is used for the design of a 3rd-order PSCF that not only validate the theory but also shows performance beyond the state of the art.

Synthesis of Complex Conjugate Poles with Arbitrary Q

Complex conjugate poles with an arbitrary Q can be realized starting from the all real pole low-pass filter shown in Fig. 1(a). This circuit is formed by two kinds of capacitors C_I (integrating capacitors) and C_S (sampling capacitor). The formers act as elements of memory, while the latter play the roles of a resistor. The number of real poles created is equal to the number of C_I's.

The location of the poles synthesized by the filter can be easily found by applying the model proposed in [3], which transforms Fig. 1(a) into its continuous-time model shown in Fig. 1(b) by replacing the switching parts (C_S and the switches) with ideal voltage buffers and equivalent resistances, $R_{eqv}=1/f_S C_S$ (for $C_I/C_S>>1$) [3].

It is known that complex conjugate poles can be generated by closing a feedback around a cascade of real poles. In this case, it is done by connecting the output of the cascade to the input through an inverting buffer and R_{eqv}, as in Fig. 2. It is possible to show that the poles generated have the same Q as the ones generated by the same order Butterworth filters. However, the pole frequencies deviate from each other, leading to in-band peaking for higher order filters. By considering this behavior, a 3rd-order filter is chosen to be designed having complex conjugate pole pair with Q=1. An example of a 3rd-order implementation is shown in Fig. 3, where C_S shares charge with C_{I1}, C_{I2}, and C_{I3}, respectively, creating a unilateral signal flow. During the phase change from Φ_3 to Φ_1, C_S is flipped to create the negative feedback behavior.

Prototype

To validate the proposed approach, a fully differential 3rd-order PSCF was designed and integrated. The charge inversion of C_S is realized by cross-coupling positive and negative nodes in the fully differential structure. The filter implementation is shown in Fig. 4. A g_m-cell was not included in the design in order not to dominate the linearity and noise responses of the PSCF itself. The filter uses six phases: Three non-inversion phases (Φ_1, Φ_2, and Φ_3), when one C_S (on the left) is connected to the top C_I's sequentially, while the other C_S (on the right) is connected to the C_I's on the bottom differential side. During the consecutive three inversion phases (Φ_{1N}, Φ_{2N}, and Φ_{3N}), the C_S's are connected to the C_I's, on the opposite sides. In order to increase the sampling rate, three time-interleaved blocks are employed.

For a sampling frequency of 160MHz, the filter 3dB bandwidth was designed to be 540 kHz. C_I's are chosen to be equal for maximum Q. All capacitors, C_I's and C_S's, are used as MIM capacitors with values 11.8pF and 225fF, respectively, together with the added parasitic capacitances. The switches are implemented using transmission gates and sized for 1.5kΩ maximum on resistances. A phase clock generator is designed using a Johnson counter structure to create the six non-overlapping clock phases from an external clock signal. For measurement purposes an open drain output buffer is designed to avoid loading the filter.

Measurements

The measurement setup consists of a voltage source fed into the filter through 200kΩ external resistors in series (R_{ext}) which acts as the Thévenin equivalent of a g_m-cell with a finite output resistance (Fig. 4). The PSCF consumes 125μA from 1.2V power supply, which is the power consumed by the phase clock generator. The active area of the chip is 0.06 mm^2 mainly dominated by the integrating capacitors (Fig. 4).

Fig. 5 shows the normalized measured transfer function of the prototype within the simulation of a post-layout schematic and the CT model proposed in [3]. A good agreement has been obtained between measurements, simulation and theory. In addition to that also the filter response of the 7th-order PSCF proposed in [1] has been added (designed to have the same DC gain and 1 dB droop frequency). It can be observed that 7th-order filter transfer function has a much smoother roll-off around the cut-off frequency compared to other filtering profiles, and this causes more than 10 dB attenuation loss around the band-edge. Almost one decade after the cut-off frequency, the measured filter response shows a flattening caused only by leakage on the PCB used for testing. The inset in Fig. 5 shows that PSCF in-band deviation both for the simulation and measurements is less than 0.5dB.

Output noise measurement (referred to the filter output) are

shown in Fig. 6(a) with a resolution bandwidth of 1 Hz. At low frequencies, noise is equal to the noise of the R_{eqv} ($4kT/f_SC_S$). The black solid line shows the simulation result of the PSCF, whereas the dashed line shows the continuous-time model simulation result. It can be seen that measured noise spectral density closely follow the simulations and theory. From the simulation it is also possible to see that leakage generated by the non-idealities present in the on-chip phase clock generator. This leakage however is negligible since it does not exceed -135dBm. The measured input referred noise is 17.0μV integrated between 10 kHz and 540 kHz. Out-of-band IIP3 is measured with two blockers at 3.4MHz and 6.7MHz creating an intermodulation product at 100 kHz. Fig. 6(b) shows the input signal power and the third-order intermodulation distortion referred to the chip input (V_{in} in Fig. 4). The out-of-band IIP3 extrapolated is 55.1dBm leading to 91.7dB SFDR.

Table I summarizes the measurement results and compares them with the 7th-order PSCF [1]. The SFDR obtained is more than 25 dB better with a much lower power consumption thanks to the presence of complex conjugate poles which allowed to reduce the order of the filter without compromising the filter selectivity close to the cut-off frequency. This once again represent a remarkable result since for the first time switched-capacitor complex conjugate poles have been integrated on silicon without the need of any amplifier.

References

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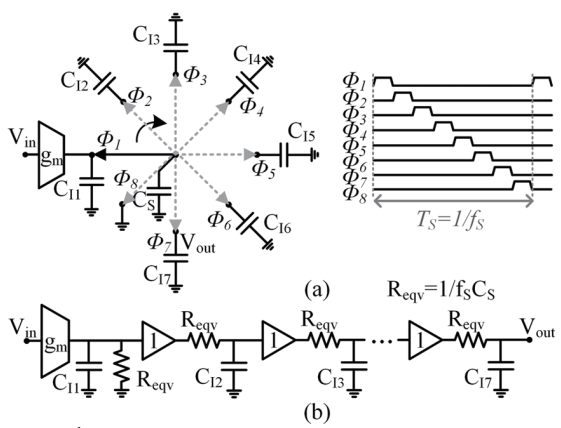

Fig. 1. (a) 7th-order all real pole low-pass PSCF, and (b) its continuous-time simplified model.

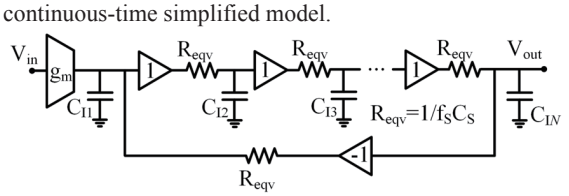

Fig. 2. Proposed low-pass filter model.

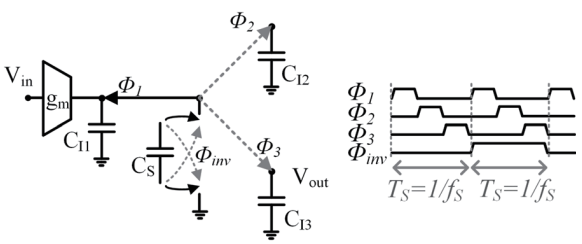

Fig. 3. Proposed 3rd-order low-pass PSCF.

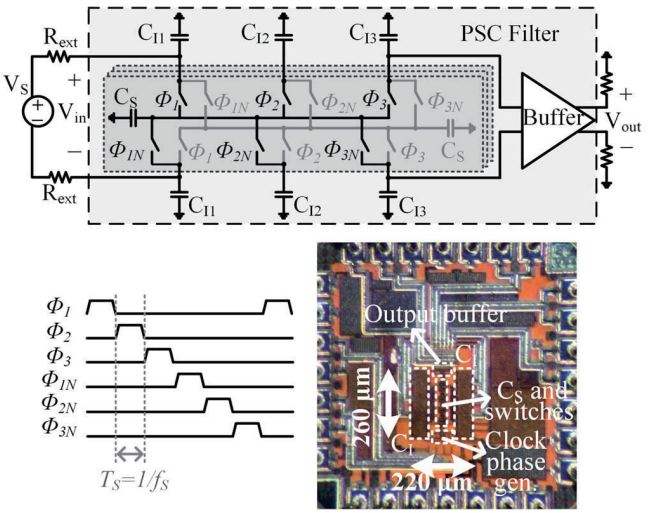

Fig. 4. Fabricated 3rd-order low-pass PSCF schematic and chip photo.

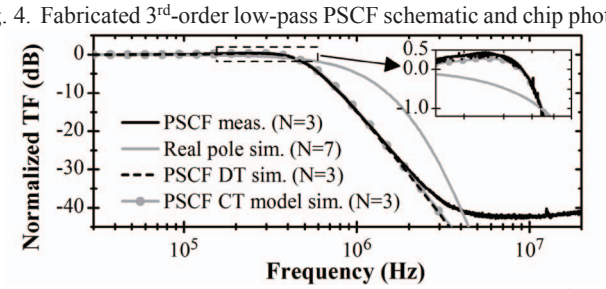

Fig. 5. Transfer function of the simulated and measured 3rd-order low-pass PSCF and the simulated 7th-order all real pole filter.

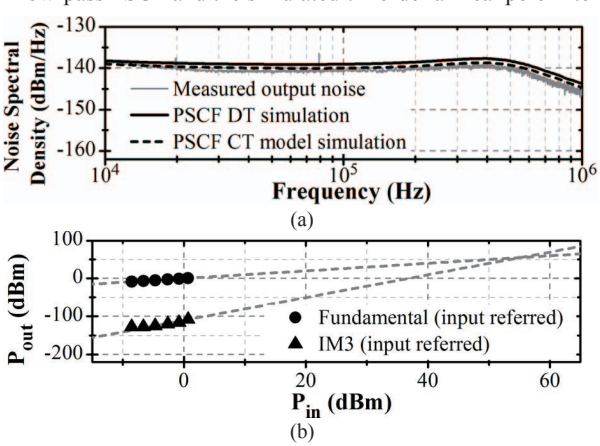

Fig. 6. (a) Measured output noise spectral density over the filter bandwidth, (b) Out-of-band IIP3 measurements of the PSCF with two tones.

TABLE I.
SUMMARY RESULTS AND COMPARISON TABLE

	This Work	[1]
Technology (nm)	130	65
Order	3rd	7th
Poles	1 real + 2 complex conj.	7 all real
Power (mW)	0.15	1.98
Voltage supply (V)	1.2	1.2
3dB cut-off (MHz)	0.54	0.4-30
Sampling Rate (MHz)	160	800
OB IIP3 (dBm)	55.1	11.7
Int. Noise (μV)	17.0*	13.7**
IRN (nV/√Hz)	23.3	4.57
SFDR (dB)* **	91.7	64
Active area (mm²)	0.06	0.42

Integrated over *10 kHz – 540 kHz, ** 50 kHz – 9 MHz bandwidth.
*** $SFDR = 2/3 \cdot (IIP3 - Int.Noise)$