# A LTE RX Front-end with Digitally Programmable Multi-Band Blocker Cancellation in 28nm CMOS

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***Abstract*—This paper presents a LTE receiver front-end with a feedback digital filter in the baseband to perform multi-band blocker cancellation. The programmable filter provides 34.9dB attenuation of TX leakage and variable attenuation of an additional blocker anywhere in the frequency range 17.5MHz–107.5MHz. The receiver front-end operates at 1.8GHz with a noise figure of 3.9dB, IIP3 of -5dBm, and consumes only 20.4–37.5mW, the lowest among state-of-the-art designs.**

## I. Introduction

Low supply voltages and analog gain in nanoscale CMOS make the design of a RF receiver (RX) very challenging. One of the most difficult requirements is to reject signals in adjacent bands (blockers) whose amplitude is much larger than the inband signal.

Traditionally, an analog channel select filter (CSF) is used before the ADC to provide blocker filtering. To improve noise shaping and power efficiency a feedback loop can be built around the cascade of a CSF and ADC thus creating a filtering ADC [1], [2]. Although this approach gives the impression of a more digital and flexible implementation, the filter transfer function still relies on the poles of the analog feed-forward path hence limiting filter selectivity and requiring accurate calibration and PVT correction. This paper replaces the feed-forward analog CSF with a digital filter in feedback around the ADC. Doing so provides a digitally defined transfer function that is highly reconfigurable and completely insensitive to PVT variations. Noise and distortion introduced in the feedback path is highpass filtered with a trivial uncalibrated 1st-order passive network. As a result, the analog baseband circuitry consists only of a 1st-order continuous-time $\Delta\Sigma$ modulator, a feedback DAC with relaxed specifications, plus a few passive components that do not require tuning. The resulting receiver is low-power and well-suited to implementation in CMOS technologies at 28nm and beyond.

## II. Baseband Blocker Cancellation

Typically, the biggest blocker comes from the local transmitter (TX). For example, in the LTE standard TX leakage can be as high as -30dBm at the receiver front-end assuming a TX-RX isolation of 57dB and TX-antenna insertion loss of 2dB [3]. Fortunately, TX leakage appears at a known frequency offset – a minimum of 41 MHz in band 20. Additionally, one other blocker (or two in an IMD test) may be present as shown in Fig. 1. In [4], a digital feedback loop was introduced to cancel one blocker, however the ADC still required enough

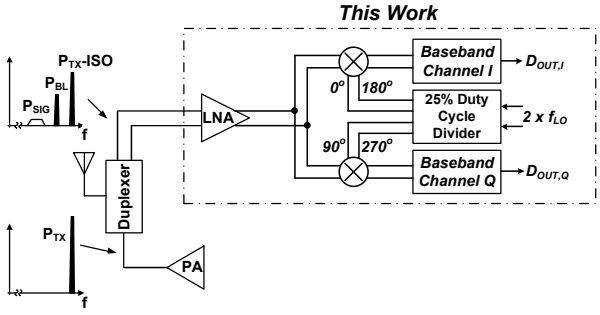


Fig. 1: RF RX front-end block diagram, with power amplifier and duplexer to illustrate the blocker profile

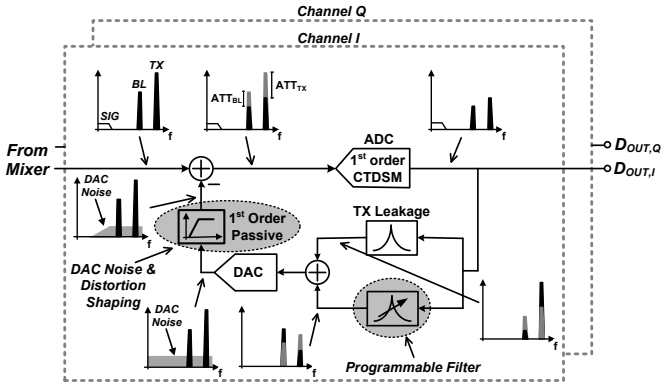


Fig. 2: Baseband signal flow with digital multi-band blocker cancellation

dynamic range (DR) to handle additional blockers; thus a 3rd order continuous-time delta sigma modulator (CTDSM) was used. To ensure stability of the digital feedback loop around the 3rd-order modulator, the maximum cancellation frequency offset was limited to only 40MHz, insufficient for LTE.

The baseband architecture operation with digital multi-band blocker cancellation is shown in Fig. 2. The baseband circuitry receives a current-mode signal comprised of the inband signal (SIG), TX leakage and an additional blocker (BL). A digital bandpass filter extracts the TX leakage at its known frequency offset, while a programmable digital bandpass filter can be

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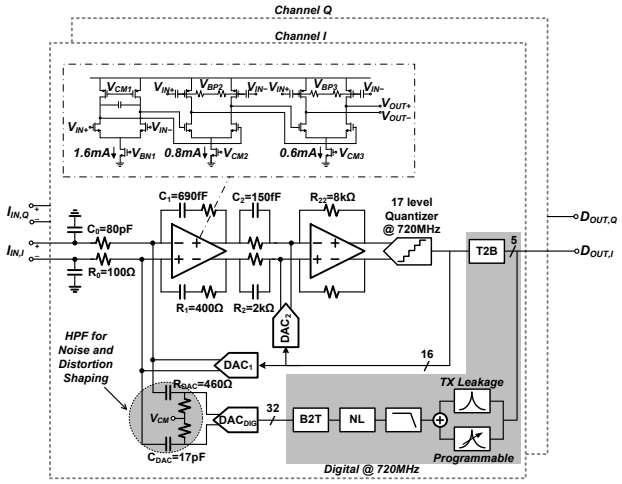
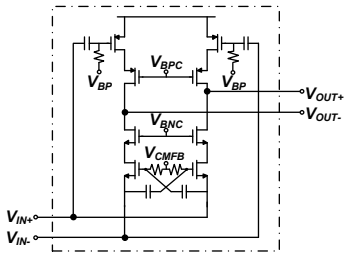
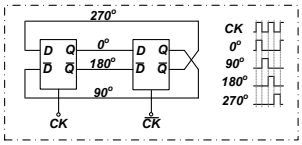



Fig. 3: Baseband circuit design with digital and HPF highlighted




(a) LNA implementation




(b) 25% duty cycle divider

Fig. 4: RF front-end building blocks

used to track another blocker. The programmable filter can be set to reject blockers at any frequency offset in the range 17.5MHz–107.5MHz under the control of an adaptive algorithm (not discussed here). The DAC converts the summed digital filter outputs to an analog current.

The DAC requires sufficient DR to cancel full-scale TX leakage and blockers while contributing minimal noise in the signal band. In [4], DAC noise made it necessary to use an accurate reconstruction filter off-chip which in turn re-amplified the blocker so that it was attenuated by only 6dB after reconstruction. Here, recognizing that the DAC is used to replicate blockers and does not have any signal content in the band of interest, a 1st order passive highpass filter (HPF) is placed at the DAC output to reduce in-band thermal noise, quantization noise and distortion from the DAC. Hence, in this work a 5-bit DAC provides 34.9dB blocker attenuation and its DR is not a limiting factor. Only a 1st order CTDSM ADC is needed in the main signal path because most of the blocker power is already absorbed by the digital path and DAC.

## III. Circuit Implementations

Fig. 3 shows the detailed baseband circuit design. A 1st order passive filter with 20MHz cutoff frequency is placed at the input to act as a lowpass anti-aliasing filter and also provides some attenuation of out-of-band blockers. The voltage swing at the mixer output $I_{IN,I}$ and $I_{IN,Q}$ is minimized with a small $R_0$ of 100Ω. The first operational amplifier is the integrator while the second operational amplifier provides additional gain and performs excess loop delay (ELD) compensation with $DAC_2$. A zero is added by introducing $C_2$ to provide some positive phase shift for compensation. The baseband has an input bandwidth of 9MHz (LTE20) with a 17-level quantizer is clocked at 720MHz yielding an oversampling ratio (OSR) of 40.

Two digital 2nd order IIR filters with 9-bit coefficient resolution detect and cancel TX leakage and one additional blocker. Note that an intermodulation test, where TX leakage plus two additional blockers are present, cancelling the TX leakage and the blocker at lower offset frequency is sufficient to reduce the intermodulation product significantly. The fully programmable coefficients allow accurate adjustment of the filter centre frequency, gain, and Q factor to effectively cancel blockers with different frequency, power level, and modulated bandwidth. The DAC quantization noise is shaped by a 1st order delay-less digital noise loop filter (NL). The output noise and distortion from $DAC_{DIG}$ is shaped furthermore by the 1st order passive highpass filter created by $R_{DAC}$ and $C_{DAC}$. A 1st order digital lowpass filter is added to cancel the effect of the passive highpass filter.

The baseband transfer function is very accurate as it is determined completely by the digital filter coefficients and clock frequency. On the other hand, an analog filter (for example, the 4th order Butterworth filter in [2]) requires accurate tuning of R and C. With process and temperature variations, the metal-oxide-metal (MOM) capacitor value in 28nm CMOS can vary by $\pm 20\%$, and poly resistors vary by $\pm 15\%$. Even excluding the switches, making R and C tunable presents at least 15-20% area overhead, as well as increasing complexity for calibration. A digital filter is also much easier to port into newer CMOS technologies and will benefit from scaling.

The three DACs are designed using a high-speed current-steering architecture [5]. A 3rd order feed-forward amplifier is used for the 1st operational amplifier. The 1st stage consumes 53% of the opamp power to reduce input referred noise, whereas the output stage consumes only 20% of the opamp power since the blocker power is mostly cancelled by the digital path.

A RF front-end is designed and included in the prototype to

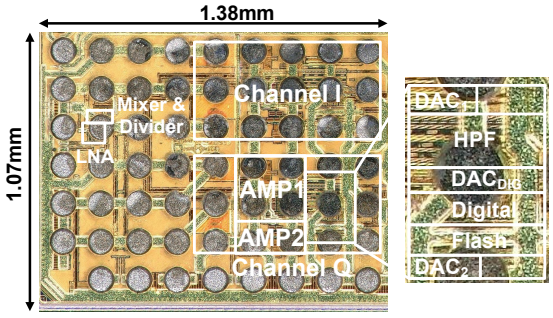



Fig. 5: Die photo.

TABLE I: Measurement summary and comparison table with other DSM-based receivers.

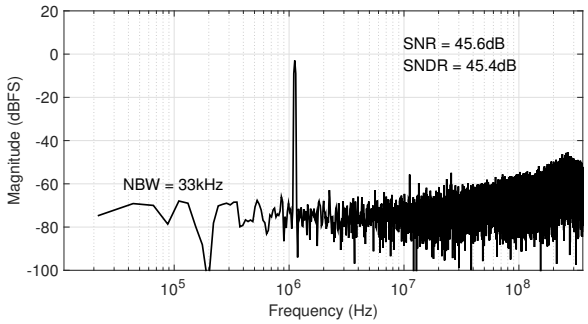
| | | [2] | [7] | [8] | [9] | This work | |
|---|---|---|---|---|---|---|---|
| Architecture | | RX with ΔΣ-CSF | RX with filtering ADC | Direct ΔΣ RX | Direct ΔΣ RX | RX with ΔΣ-fb digital filter | |
| CMOS Technology (nm) | | 65 | 80 | 65 | 40 | 28 | |
| RF Frequency (GHz) | | 0.6-3 | 0.04-1 | 0.4-4 | 0.7-2.7 | **0.9** | **1.8** |
| NF(dB) | | 2.4-3.5 | 2.7-3.5 | 16 | 5.9-8.8 | **3.8** | **3.9** |
| Power (mW) | | 35.5-53<br>43.4@1.8GHz[1] | 221.4 | 17-70.5<br>37.8@1.8GHz[2] | 90 | **19.5-36.6** | **20.4-37.5** |
| Power Breakdown (mW) | RF[3] | 23.5-36.7 | 113.4 | - | 48 | **4.4** | **5.3** |
| | BB Analog | 12-16.3 | 108 | - | 42 | **14.6** | **14.6** |
| | BB Digital | | - | - | - | **0.5-17.6** | **0.5-17.6** |
| Supply (V) | | 1.2 | 1.8/1 | 1.5/1.2 | 1.1 | **0.9** | |
| IIP3 (dBm) | | -6 | -13 | 13.5 | -2 | **-7** | **-5** |
| SNDR (dB) | | 45-52 | | 52-68 | 40-43 | **48** | |
| RF Carrier BW (MHz) | | 10,20,40 | 5,6,7,8 | 4,10 | 1.4,15 | **18** | |
| Area (mm$^2$) | | 0.7 | 5.6[4] | 0.56 | 1 | **0.64** | |

1. LTE20 mode 2. Estimated 3. RF power includes LNA, mixer, LO gen and distribution
4. Incl. PLL and DSP

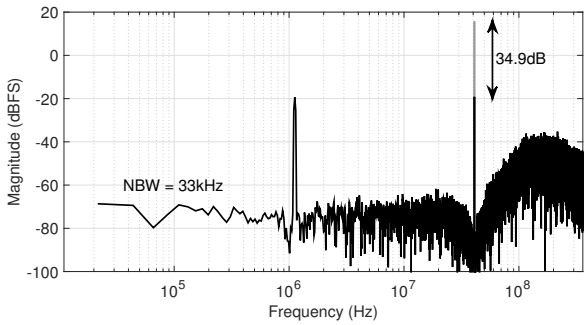
test the blocker cancellation baseband in a realistic scenario. The low input-referred noise of this baseband permits a simplified and low-power low-noise amplifier (LNA) design. A common-gate LNA is used, shown in Fig. 4a. To improve its transconductance, the NMOS input pair is capacitively cross-coupled [6], and the input is also fed into the PMOS input pair. The LNA output impedance is improved with the cascode. The I and Q current-mode passive mixers are driven by a 25% duty cycle divider that consists of two latches as shown in Fig. 4b. A 50% duty cycle clock at twice the LO frequency is provided to the divider from off-chip.

## IV. Measurement Results

The RF receiver front-end prototype was fabricated in 28nm CMOS technology. It occupies 1.07mm×1.38mm with an active area of 0.64mm$^2$ (Fig. 5). The measurement result is summarized and compared with other DSM-based RX designs in Table I. The receiver front-end operates at 0.9GHz and 1.8GHz with a noise figure of 3.8dB and 3.9dB respectively, which is dominated by the RF front-end. The baseband digital consumes as little as 0.5mW with no blockers present, 11.7mW with only TX leakage cancellation on and 17.6mW with both TX leakage and blocker cancellation enabled, hence




(a)

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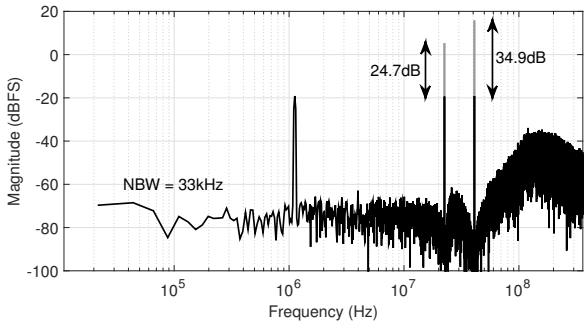
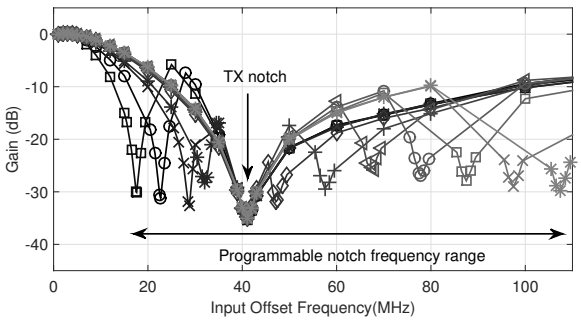



(c)

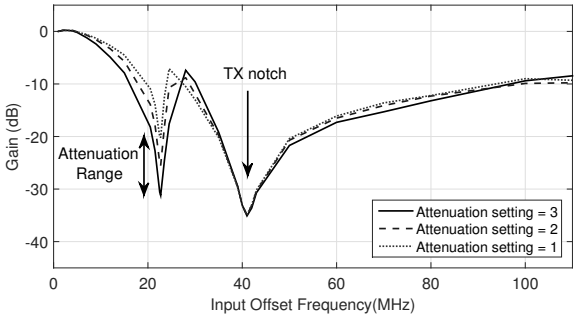
Fig. 6: measured FFT spectrum for (a) digital filter off, (b) TX leakage cancellation, and (c) TX leakage and additional blocker cancellation

the total power consumption for 1.8GHz input can vary between 20.4mW and 37.5mW. IIP3 is measured with two blockers at 17.5MHz and 35MHz, in accordance with the LTE20 standard [3]. The programmable notch was placed at 17.5MHz, thus cancelling most of the intermodulation product. IIP3 is -5dBm at 1.8GHz, and is limited by the RF front-end.

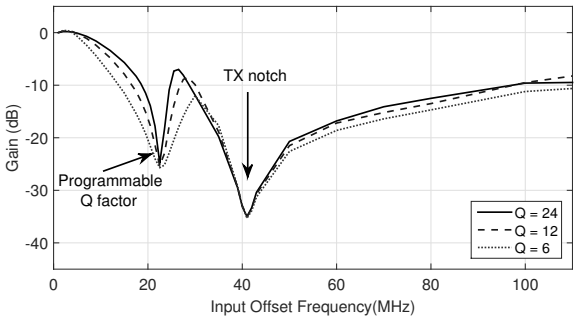
Fig. 6 shows the measured output spectrum of channel I in three different scenarios for band 20 of the LTE20 standard. First, if there are no blockers present, the digital filter can be turned off to provide a 45% power savings. Second, TX leakage is present at 41MHz frequency offset from the input, and the digital bandpass filter is placed exactly at 41MHz to provide an attenuation of 34.9dB. The attenuation is reduced to 31.7dB for a 5MHz-bandwidth modulated blocker centered at 41MHz [3]. Finally, an additional blocker is introduced at




(a)




(b)




(c)

Fig. 7: Measured baseband frequency response for programmable notch at different (a) frequency, (b) attenuation, and (c) Q factor settings

22.5MHz and is attenuated by 24.7dB by the programmable filter. The grey lines in the FFT spectrum are only used to illustrate the amount of attenuation.

Fig. 7 shows the measured baseband frequency response with different settings for the programmable notch. It can be moved to any precise frequency in the range of 17.5MHz–107.5MHz. The amount of attenuation can be decreased to increase the loop phase margin. In addition, the Q factor of the notch can be adjusted depending on the modulated blocker bandwidth. A low Q notch is undesirable near the signal band to prevent signal attenuation, however that's not a problem as blockers close to the signal band have a maximum bandwidth of 5MHz [3].

Signal to noise and distortion ratio (SNDR) is measured with a signal input offset 1MHz from the carrier, and the

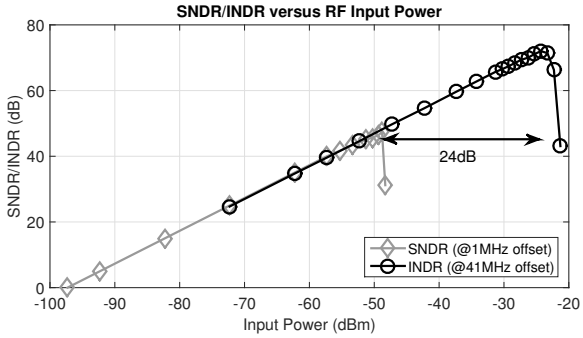



Fig. 8: SNDR and INDR versus RF input power.

interference-to-noise and distortion ratio (INDR) is measured at 41MHz offset, as shown in Fig. 8. It can be seen that the receiver front-end can handle a TX leakage 24dB larger than the ADC fullscale, while maintaining the same in-band noise.

## V. Conclusion

A RF receiver with a multi-blocker cancelling baseband is introduced as a replacement for the conventional cascade of analog filter and ADC. The digital bandpass filters produce two flexible notches in the baseband frequency response, cancelling TX leakage and an additional blocker as required by the LTE20 standard. Compared with previous state-of-the-art designs, this work achieves competitive IIP3 and noise figure, while consuming the lowest power and can dynamically scale its power depending on the number of blockers present.

## Acknowledgment

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