# Thermal noise limit for time-domain analogue signal processing in CMOS technologies

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The impact of thermal noise in voltage- and time-domain analogue signal processing is discussed. Despite the technology scaling allows to resolve smaller time differences, it will be shown that in CMOS technologies voltage signal processing have a better fundamental limit compared with its time counterpart.

*Introduction:* With the scaling down of the channel length and increasing bandwidth in CMOS technologies, the performance improvement in analogue circuits has been subpar compared with their digital counterpart. Analogue circuits are penalised by the lowering of the voltage supply, reduced to minimise the power consumption of the digital section. To overcome the limitations coming from a low-voltage supply, the research activity has recently started to look towards solution based on time-domain signal processing [1, 2]. In time-domain signal-processing, the information is extracted measuring time difference between two events instead of a voltage drop. The elaboration of the signal relies on the capability to create accurate delayed replicas of the input waveform and on the possibility to digitalise them by the use of time comparators, implemented with flip-flops or latches [2]. Eventually, the amount of information that can be digitalised is limited by the maximum delay generated by the circuit [1]. The key idea beyond this approach is that the time resolution improves with the technology scaling, being related to the unitary gain bandwidth of the transistor (i.e. $f_T$) [1].

The aim of this Letter is to analyse and compare the performance of the CMOS inverter used in both voltage- and time-domain approaches. As done for an analogue circuit operating in voltage mode by Castello and Gray [3] and Enz and Vittoz [4], a straightforward relationship between power consumption and dynamic range will be provided for time-domain operation, showing that in deep-scaled CMOS technologies both approaches are limited in similar ways.

The comparison between voltage and time domain will be realised starting from the CMOS amplifier in Fig. 1. This structure can be used both in voltage and time domain, in the first case by acting as a voltage amplifier [5], in the latter as a delay stage. In the first case, the information is contained in the amplitude of the sinusoid, whereas in the second case in the period.

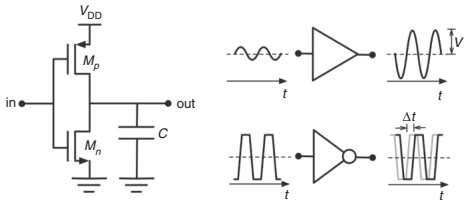


**Fig. 1** *CMOS stage used as amplifier or as delay element*

In voltage domain, the maximum signal that can be processed by this circuit is limited by the voltage supply, whereas the minimum signal by the thermal noise produced by the transistor. These boundaries define the signal-to-noise ratio (SNR) of the amplifier, and with it its performance [4]. In time domain, the jitter noise added by the inverter sets a lower bound in the time difference detectable, whereas the upper bound is set by the maximum delay generated by the circuit. Also for the time domain it is possible to define an SNR that is the parameter used for the comparison. To simplify the analysis, the transistors will be assumed linear (when operating as an amplifier) and with only thermal noise [4].

*SNR against power in voltage domain:* The SNR achievable by the inverter used as an integrator has been already evaluated by Enz and Vittoz in [4]. As shown in [4], the minimum signal detectable is limited by the noise integrated in the output capacitor equal to $V_{n,\mathrm{rms}}^2 = \mathrm{kT}/C$, where the $k$ is the Boltzmann constant and $T$ is the temperature of the circuit. On the other side, the maximum sinusoidal output is set by the voltage supply ($V_{DD}$) by having an amplitude equal to $V_{s,\mathrm{rms}} = V_{DD}/2\sqrt{2}$ [4]. These two constraints lead to a maximum achievable SNR given by

$$\mathrm{SNR} = \frac{V_s^2}{V_n^2} = \frac{C}{8\,\mathrm{kT}} V_{DD}^2 = \frac{C}{4\,\mathrm{kT}\alpha_V} V_{DD}^2 \tag{1}$$

with $\alpha_V = 2$. Enz and Vittoz relate the SNR also to the power consumption of the stage that in this case is equal to

$$\mathrm{power} = V_{DD} \times fCV_{DD} \tag{2}$$

where $f$ is the frequency of the sinusoidal input [4]. From (1) and (2) the minimum power required to achieve a given SNR and bandwidth for a voltage-domain-based circuit was obtained

$$\mathrm{power} = 8\,\mathrm{kT}f\ \mathrm{SNR} = 4\,\mathrm{kT}f\ \mathrm{SNR}\ \alpha_V \tag{3}$$

Although (3) was derived from a particular case, it sets a fundamental limitation for any analogue circuit operating in voltage domain [4]. In fact, the same results were found a few years earlier by Castello and Gray for switch capacitor circuits [3] and it is the base on the well-known ADC figure of merit (FoM) proposed by Schreier [5].

*SNR against power in time domain:* The approach adopted by Enz and Vittoz is used in this Letter for time-domain operation. In this case, the jitter noise produced by the inverter and the maximum delay achievable will be used to achieve an expression of power against SNR.

The expression of the jitter added by a CMOS inverter as a function of the generated delay was evaluated by Abidi in [6] and is given by

$$\sigma^2 = \frac{8\gamma\,\mathrm{kT}t_d^2}{CV_{DD}(V_{DD} - V_t)} + \frac{4\,\mathrm{kT}t_d^2}{CV_{DD}^2} \tag{4}$$

where $\sigma$ is the jitter, $t_d$ is the delay of the inverter, $\gamma$ is the thermal noise coefficient for the transistor and $V_t$ is the transistor voltage threshold. Equation (4) can be used for both transitions (i.e. from $V_{DD}$ to 0 and vice versa) assuming the same $V_t$ for both n-channel MOS (n-MOS) and p-channel MOS (p-MOS) transistors. The jitter expression found by Abidi is constituted by two terms, the first one takes in account of the noise injected by the transistor during the switching phase, whereas the second derives from the initial noise charge stored in the capacitance $C$ before the commutation [6]. Starting from (4) it is possible to define the SNR of the inverter working as a delay stage as

$$\mathrm{SNR} = \frac{t_d^2}{\sigma^2} = \frac{1}{\left(8\gamma\,\mathrm{kT}/(CV_{DD}(V_{DD} - V_t))\right) + (4\,\mathrm{kT}/CV_{DD}^2)} \tag{5}$$

Note that, the SNR of the inverter in time domain is independent of the delay generated, being a function of the capacitive load $C$, the voltage supply and the transistor threshold. For an easier comparison with (1), (5) can be rewritten as

$$\mathrm{SNR} = \frac{C}{4\,\mathrm{kT}\alpha_T} V_{DD}^2 \tag{6}$$

with

$$\alpha_T = \frac{2\gamma V_{DD}}{V_{DD} - V_t} + 1 \tag{7}$$

Equation (6) looks very similar to (1) except for the factor $\alpha_T$. In fact, while in voltage domain $\alpha_V = 2$, in time domain $\alpha_T$ is technology dependent because it is a function of the ratio between the voltage threshold and the voltage supply. Since the power consumption of the stage in both cases is the same, the relationship between power and SNR in time-domain results

$$\mathrm{power} = 4\,\mathrm{kT}f\ \mathrm{SNR}\ \alpha_T \tag{8}$$

*Limitations and comparison:* Equations (6) and (8) show that the ultimate performance in time domain is a function of the technology used. However, from the point of view of the maximum SNR achievable, this dependency is function of the voltage supply adopted rather than the transistor cut-off frequency. An increment of $f_T$ allows to resolve a smaller time difference (lowering, for example, the quantisation noise in a TDC), but it cannot improve the ultimate limit set by the thermal noise.

Another important observation coming from (7) is that $\alpha_T$ is always >2, which means that in principle the SNR achievable in time domain

cannot be better than the one obtained in voltage domain (assuming the same power and bandwidth). An intuitive explanation for this can be found considering that the generation of a delay through a CMOS inverter requires two elements: a threshold to trigger a transition and a capacitor to store the digital value before the commutation. Since a signal lower than the threshold cannot trigger the CMOS inverter, the dynamic range of the stage is intrinsically reduced by a factor ($V_{DD}-V_t$). This explains the first term in (7) that tends to 2 when $V_t$ tends to 0. On the other side, since the noise associated with the previous transition is stored in the capacitor, it is transferred to the output during the generation of the delayed replica of the input signal by leading to the term +1 in (7). This last penalty is not present in voltage domain because the amplifier works as a continuous time circuit where the capacitor integrates only the thermal noise injected in one period.

The result obtained by (8) should not surprise too much, since after all inverter-based time-domain circuits generate the delay by sensing a voltage signal. For this reason, the ultimate time-domain limit should not overcome the voltage-domain one. However, it is important to recall that (8) cannot be considered a fundamental limit such as (3) since the expression of $\alpha_T$ depends on (4), which was obtained by Abidi under several assumptions and approximations (although in [6] a good agreement has been demonstrated through experimental results and in this Letter through simulations performed with different technologies).

Expression (3) offers a straightforward relationship between the SNR, the bandwidth and the power achievable by a circuit which operate in voltage domain. Such expression has been used as FoM in different forms. The most trivial expression is given by

$$\mathrm{FoM} = \frac{\mathrm{SNR} \cdot f}{\mathrm{power}} \tag{9}$$

that differs from the one used by Murmann in [7] only by a factor 2 (which derives by the fact that in Nyquist ADCs the signal bandwidth is half of the clock rate). From (3) it is possible to verify that (9) cannot exceed 1/8 kT (i.e. 195 dB $J^{-1}$). If for voltage-domain circuits, the maximum value for the FoM expressed by (9) is fixed, in time domain such limit is technology dependent being equal to 1/(4 kT $\alpha_T$). This limit, coming from (8) cannot exceed its voltage counterpart.

*Simulation results:* Simulations have been performed in different technology nodes (IBM 130 nm, TSMC 65 nm and ST 28 nm SOI) to quantify the performance of the inverter used as a delay stage. For each technology, different transistor types were used to verify the impact of the ratio between voltage supply and the voltage threshold. For 130 and 65 nm technologies, low-/standard-/high-voltage threshold transistors were used (lvt, std and hvt, respectively). In the case of the 28 nm SOI, the threshold was changed by varying the voltage applied to the body of n-MOS and p-MOS transistors: std case (0 V, 0 V), lvt case (1.5 V, −1.5 V) and hvt case (−1 V, 1 V).

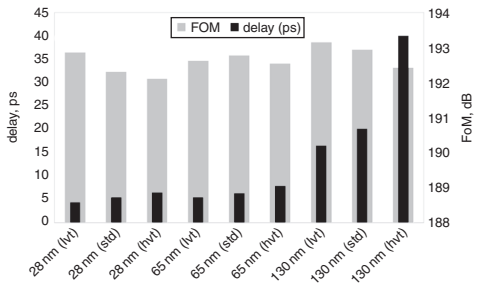


**Fig. 2** *Simulated delay and FoM for different CMOS technologies*

The jitter and the delay for the inverter were derived by simulating a three-stage ring oscillator under the same assumption provided by Abidi in [6]. Since the developed theory is based only on thermal noise, other noise sources were neglected. Since the minimum delay achievable scales with the technology node (and with it the power consumption), the best way to provide a clear comparison was to use the FoM defined by (9). As shown in Fig. 2, although the time resolution achievable improved significantly with the technology scaling, the FoM remains almost constant. The FoM behaviour can be better explained by plotting it against $V_{DD}/V_t$ (Fig. 3). When $V_{DD}/V_t$ is large, $\alpha_T$ is small and so the performance of the inverter used as delay stage improves. In Fig. 3, the voltage-domain fundamental limit (1/8 kT) and also the time-domain limit 1/(4 kT $\alpha_T$) are reported. For the latter, variations of ±10% have been also added since, as previously stated, the developed theory is based on some simplifications.

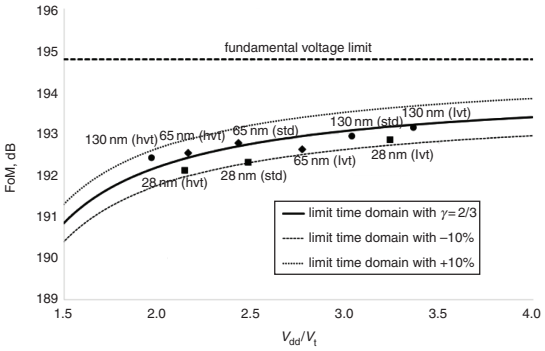


**Fig. 3** *Simulated FoM for CMOS delay stage against $V_{DD}/V_t$*

*Conclusion:* The impact of the thermal noise in voltage- and time-domain signal processing for CMOS technologies have been discussed. A fundamental limitation in the SNR achievable in time domain was derived, by showing that the performances are related to the ratio between the threshold and the supply adopted rather than the technology node used.


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## References

1 Staszewski, R.B., and Balsara, P.T.: 'All-digital frequency synthesizer in deep-submicron CMOS' (Wiley, Hoboken, New Jersey)
2 Chen, P., Chen, C., *et al.*: 'A time-to-digital-converter-based CMOS smart temperature sensor', *J. Solid-State Circuits*, 2005, **40**, (8), pp. 1642–1648
3 Castello, R., and Gray, P.: 'Performance limitations in switched-capacitor filters', *Trans. Circuits Syst.*, 1985, **CAS-32**, (9), pp. 865–876
4 Enz, C., and Vittoz, E.: 'CMOS low-power analog circuit design'. Proc. of IEEE Int. Symp. on Circuits and Systems (ISCAS), Ch. 1.2, Tutorials, Atlanta, May 1996, pp. 79–133
5 Schreier, R., and Temes, G.C.: 'Understanding delta–sigma data converters' (Wiley-IEEE Press, Hoboken, New Jersey, 2005)
6 Abidi, A.: 'Phase noise and jitter in CMOS ring oscillators', *J. Solid-State Circuits*, 2006, **41**, (8), pp. 1803–1816
7 Murmann, B.: 'The race for the extra decibel: a brief review of current ADC performance trajectories', *Solid-State Circuits Mag., Summer*, 2015, **7**, (3), pp. 58–66